P19401

128x64 YELLOW OLED

Application Notes

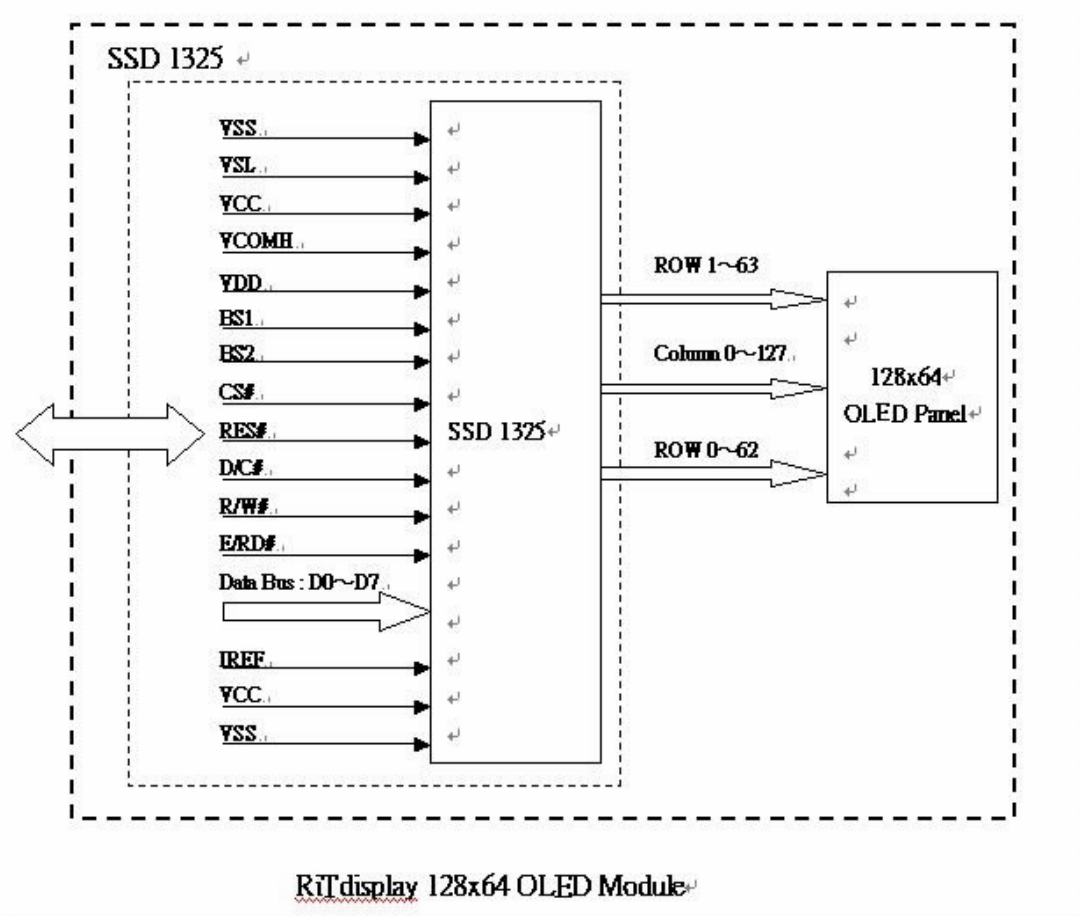
DESCRIPTION

P19401 is a 128X64 dot matrix 16 grayscale OLED module with controller for many compact portable applications.

FEATURE

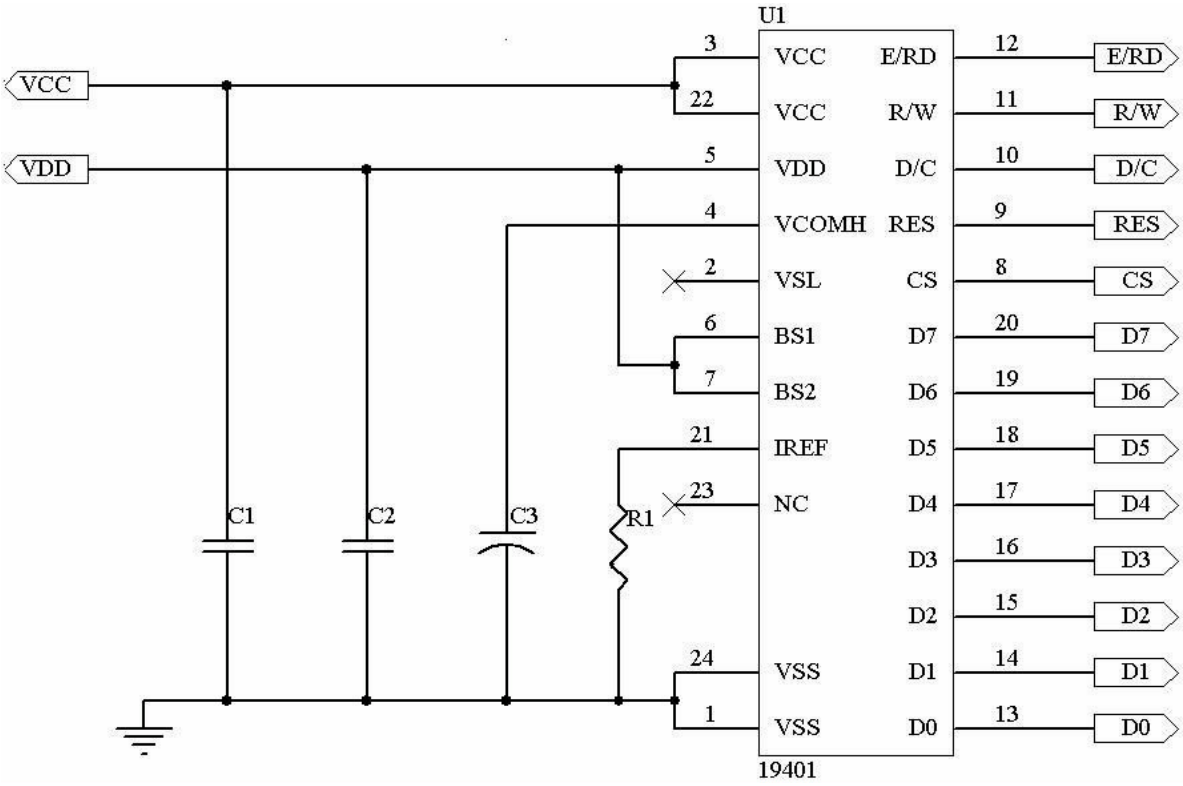
- Panel matrix 128x64.
- Driver IC: SSD1325.
- VCC=14V
- VDD=2.4~3.5V.
- 8-bit 6800-series parallel interface,8-bit 8080-series Parallel Interface, serial peripheral interface.
- Display data RAM: 128x80x4 = 40960 bits.
- Adjustable frame frequency and pre-charge Voltage.
- Row re-mapping and Column re-mapping.

FUNCTION BLOCK DIAGRAM



RiTdisplay 128x64 OLED Module

APPLICATION CIRCUIT



Recommend components:

C1: 2.2uF/25V (0805)

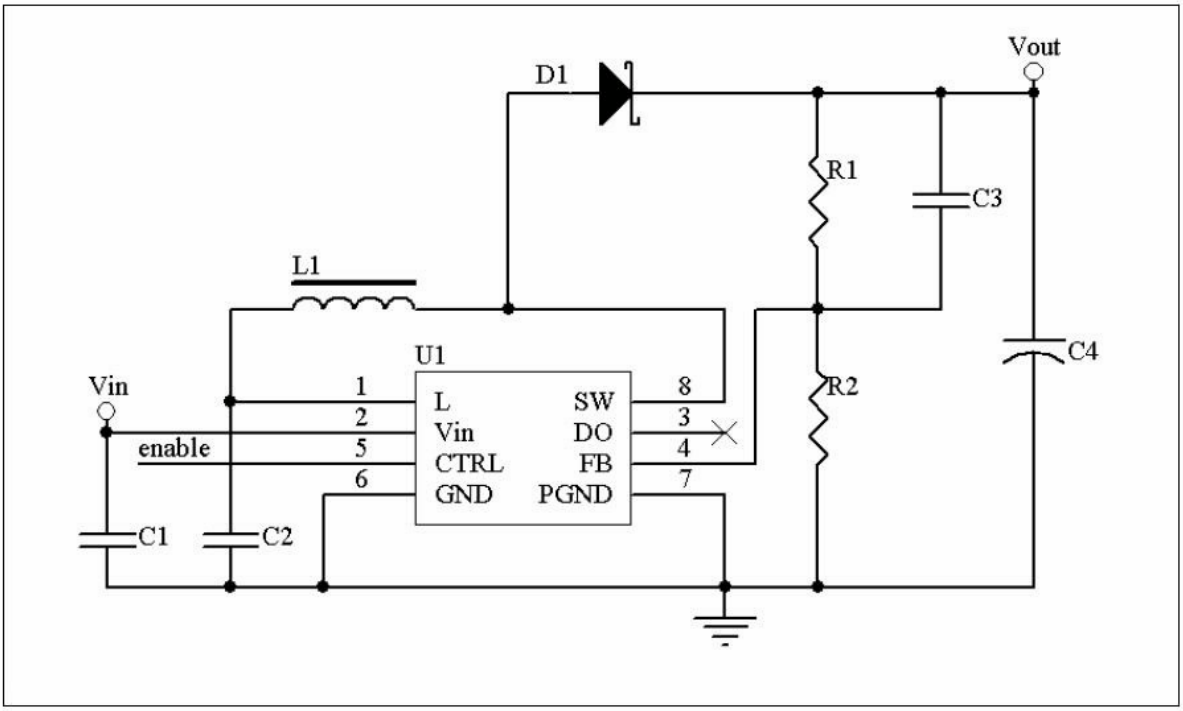
C2: 1uF/16V (0603)

C3: 4.7uF/25V (TANTALUM or Solid Tantalum 4.7uF/ 25V/ A Case (Vishay 572D))

R1: 1M ohm/1% (0603)

Notes: This circuit is for 8080 interface.

External DC-DC application circuit



Recommend components:

The C1: 0.1uF/6.3V.

The C2: 4.7 uF/6.3V.

The C3: 22pF/16V.

The C4: 4.7 uF/25V Tantalum type capacitor.

The R1: 1.2M ohm/ 1%

The R2: 115K ohm/ 1%

The D1: SCHOTTY DIODE.

The L1: 10uH.

The U1: TPS61045DRB

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

Pin No.	Pin Name	TYPE	Description
1	VSS	I	This is a ground pin.
2	VSL	O	This pin is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to VSS for stability.
3	VCC	I	Positive OLED high voltage power supply
4	VCOMH	O	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
5	VDD	I	Voltage power supply for logic
6	BS1	-	Interface select pin
7	BS2	-	Interface select pin
8	CS#	I	Chip select pin. The driver IC will be selected When CS pin is active low.
9	RES#	I	Hardware reset signal
10	D/C#	I	Data/Command control pin. When it pulled high, the input at D0-D7 is treated as display data. When it pulled low, the input at D0-D7 is transferred to command register
11	R/W#	I	Write strobe signal and reads data at the low level
12	E(RD#)	I	Read strobe signal and reads data at the low level
13	D0	I/O	8-bit data bus
14	D1	I/O	8-bit data bus
15	D2	I/O	8-bit data bus
16	D3	I/O	8-bit data bus
17	D4	I/O	8-bit data bus
18	D5	I/O	8-bit data bus
19	D6	I/O	8-bit data bus
20	D7	I/O	8-bit data bus
21	IREF	I	The current reference input pin, this pin should be connected to ground through a resistor.
22	VCC	I	Positive OLED high voltage power supply It is supplied by external high voltage source
23	NC	I	No connection.
24	VSS	I	This is a ground pin.

Application Software

```
/* 128 x 64 OLED driver program */
void init_oled(void)
{
comm_out(0xad);//set muster configuration
comm_out(0x02);//Disable DC-DC converter
comm_out(0xae);//set display off
comm_out(0xa8);//set multiplex ratio
comm_out(0x3f);//second byte
comm_out(0xa1);//set display start line
comm_out(0x00);//second byte
comm_out(0xa2);//set display offset
comm_out(0x00);//second byte
comm_out(0xa0);//set re-map
comm_out(0x41);//second byte
comm_out(0x85);//half current range
comm_out(0x81);//set contrast
comm_out(0x4f);//second byte
comm_out(0xbc);//set pre-charge voltage
comm_out(0x00);//second byte
comm_out(0xbe);//set VCOMH voltage
comm_out(0x1f);//second byte
comm_out(0xbf);//set Segment Low Voltage (VSL)
comm_out(0x02);//second byte
comm_out(0xb1);//pre-charge/discharge
comm_out(0x33);//second byte
comm_out(0xb2);//set row period
comm_out(0x22);//second byte
comm_out(0xb3);//set display clock divide ratio/oscillator frequency
comm_out(0xc3);//second byte
comm_out(0xaf);//display on
}
```

After initial the driver IC, user must clear the whole DDRAM.

```
void cleanDDR(void)
{
char i,j;
comm_out(0x15);//set column address
comm_out(0x00);//Column Start Address
comm_out(0x3f);//Column End Address
comm_out(0x75);//set row address
comm_out(0x00);//Row Start Address
comm_out(0x4f);//Row End Address
for(i=0;i<80;i++)
{
for(j=0;j<64;j++)
{
data_out(0x00);//clean DDRAM
}
}
}
```

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|									
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs Column Address (HEX)

COM Outputs / Row Address (HEX)

(Display Startline=0)

Table 3– GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]
|	|									
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs Column Address (HEX)

COM Outputs / Row Address (HEX)

(Display Startline=0)

Table 4–GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	(HEX)
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
|	|									
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 5–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=10H)

Table 6–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00										(HEX)
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
|	|									
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										
COM Outputs	Row Address (HEX)										

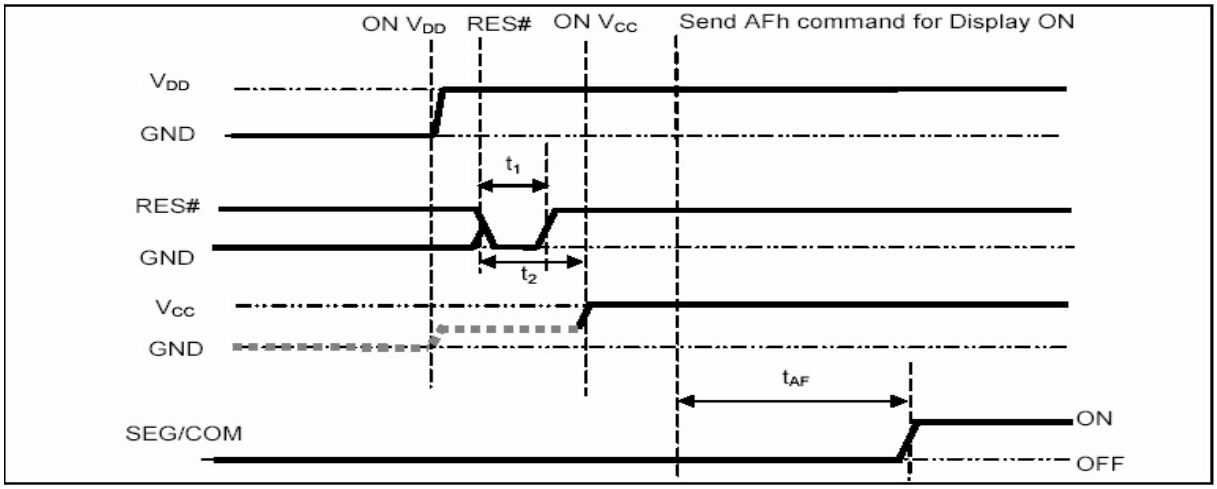
(Display Startline=0)

Table 7–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, … , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

Power On/Off Sequence

***Power ON sequence**:*

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



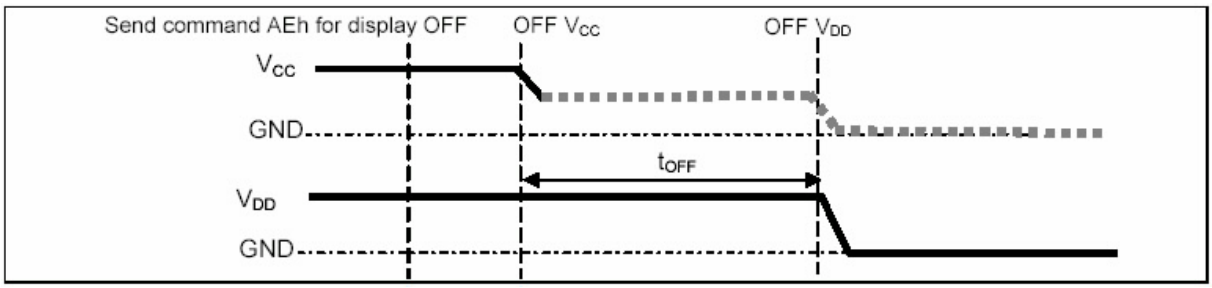
Power OFF sequence:

1.Send command AEh for display OFF.

2.Wait until panel discharges completely.

3.Power OFF V_{CC}. (1), (2)

4.Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

THANK YOU