ZTW622 (Preliminary Specification 0.0.2)

8x8 channels
Capacitive Touch Screen Controller

PRODUCT FEATURES

- 6th Generation Capacitive touch screen controller
  - 8 x 8 channels, 1 independent Wakeup Self Key
  - Up to 10 fingers
  - No scan rate degradation in multi touch
- Benefits
  - Hybrid Touch
    - Self + Mutual capacitance sensing
    - Enhanced Water Proof
    - Enhanced Glove Touch
    - Enhanced Stylus Pen
  - HW Touch Detection
    - Touch Gesture Wakeup
    - Ultra Low Power Touch Detection
  - CDMS (SF)
    - Enhanced SF Technology
    - Higher SNR
    - Higher Scan Rate
    - Lower Power Consumption
- Fast response time (NOTE1)
  - Point detection latency : Down to 10msec
  - Point report rate : Down to 10msec
- High screen resolution
  - Up to 2048x2560
- Supporting LCD size
  - Up to 3.0 inch with 8x8 channel
- TSP sensor type
  - On-cell touch
  - GF1 with/without shield layer
  - G2(SITO) with/without shield layer
  - G1F without shield layer
  - GFF without shield layer
  - Metal Mesh sensor
- Sensor pattern :
  - Best performance for stylus pen, finger nail
  - 1 layer pattern for GF1,GF2,G1,G2(SITO),GG(SITO)
  - 2 layer pattern for G1F, GFF, GG(DITO), GFd
- Minimum gap between TSP and LCD (NOTE2)
  - Down to 0.1mm UV resin gap
  - Down to 0.1mm AIR gap
- Window thickness
  - 0.5 ~ 3.0mm glass
  - 0.5 ~ 2.5mm plastic
- High SNR
  - Stylus pen : down to 1.0phi tip (NOTE3)
- Supporting COB(Chip On Board)
  - Tested up to 150mm FFC/FPC
  - FFC or B2B connector
- I2C interface options
  - I2C : Supporting BYTE/DMA mode
  - I2C : Up to 400KHz/1MHz
  - I2C: Open drain I/O with 1.62V ~ 3.6V
- DSP technology for the noise reduction
  - Minimizing the cheek/grab noise
  - Minimizing the charger noise
  - Minimizing the LCD noise
  - Various digital filters
- No TSP calibration
  - Real time compensation
  - Fast/Easy mass production
- No RFI issue (NOTE4)
  - No interference to FM, NFC, GSM
  - Immune to 2G/3G/4G, WiFi, Bluetooth RF
- Windows software (ZTouchDebugger)
  - Demonstration, Evaluation, Debugging
  - Firmware downloading, data monitoring
  - Built in Test Mode for Mass production
- Manufacturing support
  - TSP drawing, FPC schematic, FPC gerber
  - Design guide for Test Machine
- Single power supply
  - 2.7V ~ 3.6V
  - VBUS needed to ultra-power saving operation
- Wide operating temperature
  - Operating : -20°C ~ 85°C
  - Storage : -40°C ~ 125°C
- Small package
  - 25-ball WLCSP : 1.97mm x 1.97mm x 0.47T (0.4mm ball pitch)
- Hazardous Substance
  - Pb-free/Halogen-free, RoHS/REACH compliant

[NOTE]

1. Response time is related to the channel counts, Cm, charger noise and LCD noise. Suggested value can be changed according to the system properties.
2. The gap thickness is heavily affected by LCD types, glass thickness and TSP structure
3. Point diameter is affected by TSP performance
4. Need further discussion with the customer about RF interference such as antenna location for touch performance optimization.

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REVISION HISTORY

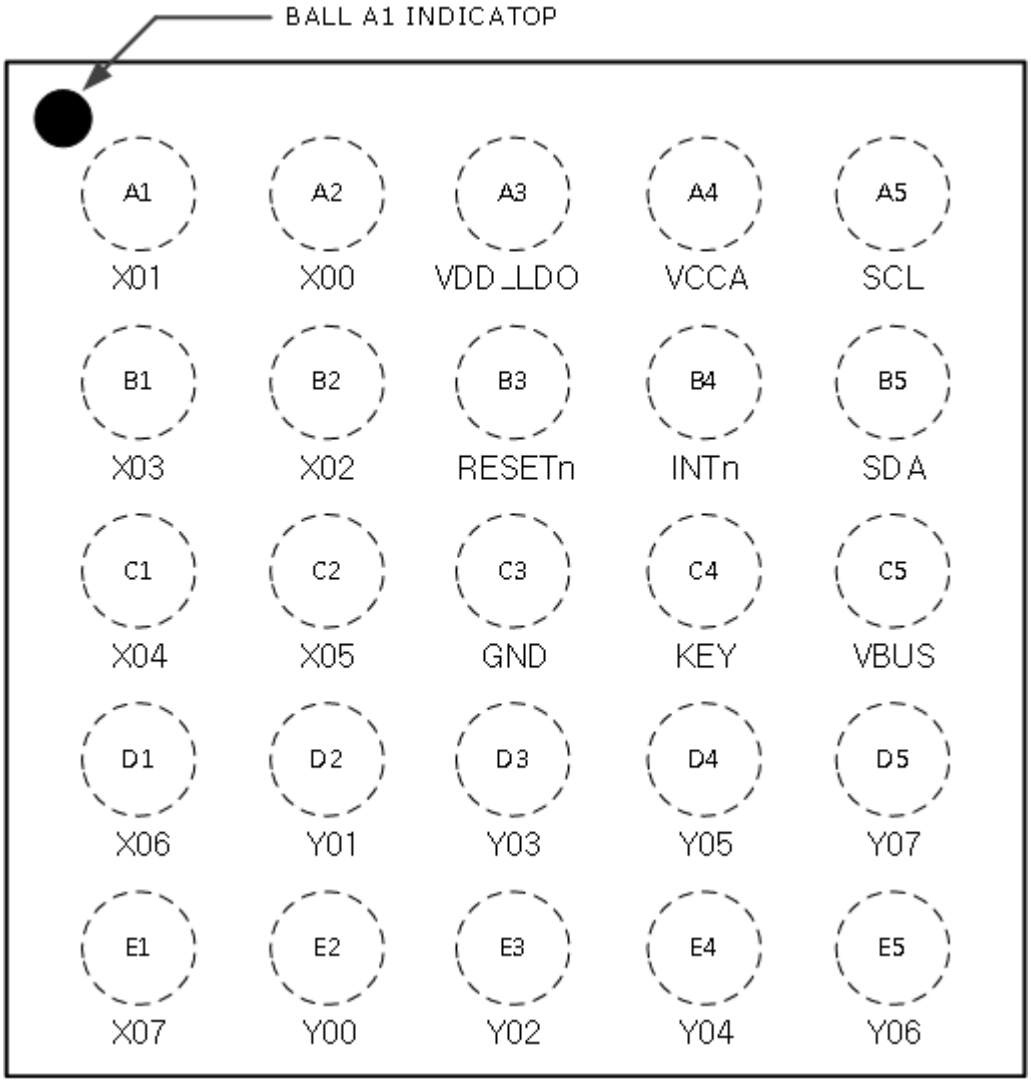
REV	DATE	AUTHOR	DESCRIPTION
0.0.1	2019/08/08	Leonard Kim	First release
0.0.2	2019/08/21	Leonard Kim	Correct Channel Information Typo. Update Block Diagram

1. GENERAL DESCRIPTION

The ZTW622 is a 6th generation capacitive touch screen controller vitalizing the transparent capacitive touch screen panel. New hybrid AFE engine utilizing both mutual and self-driving provides better wet touch, glove touch and stylus pen performance. In addition, the embedded hardwired touch-detection engine is able to minimize power consumption in idle mode during the system is suspended. The system can be revoked by user-defined gestures which can be programmed on the user space NVM embedded on this controller. It also includes all signal processing algorithms to provide the versatile filters to cope with various LCD types, noises and user-defined scenarios.

It supports wide I/O voltage level which can accept the various voltage level of I/O in HOST CPU so that it can be compatible with almost all HOST CPU for the mobile applications. For HOST CPU communication, it provides I2C interface with up to 1MHz of I2C clock speed which is the fastest in I2C specification.

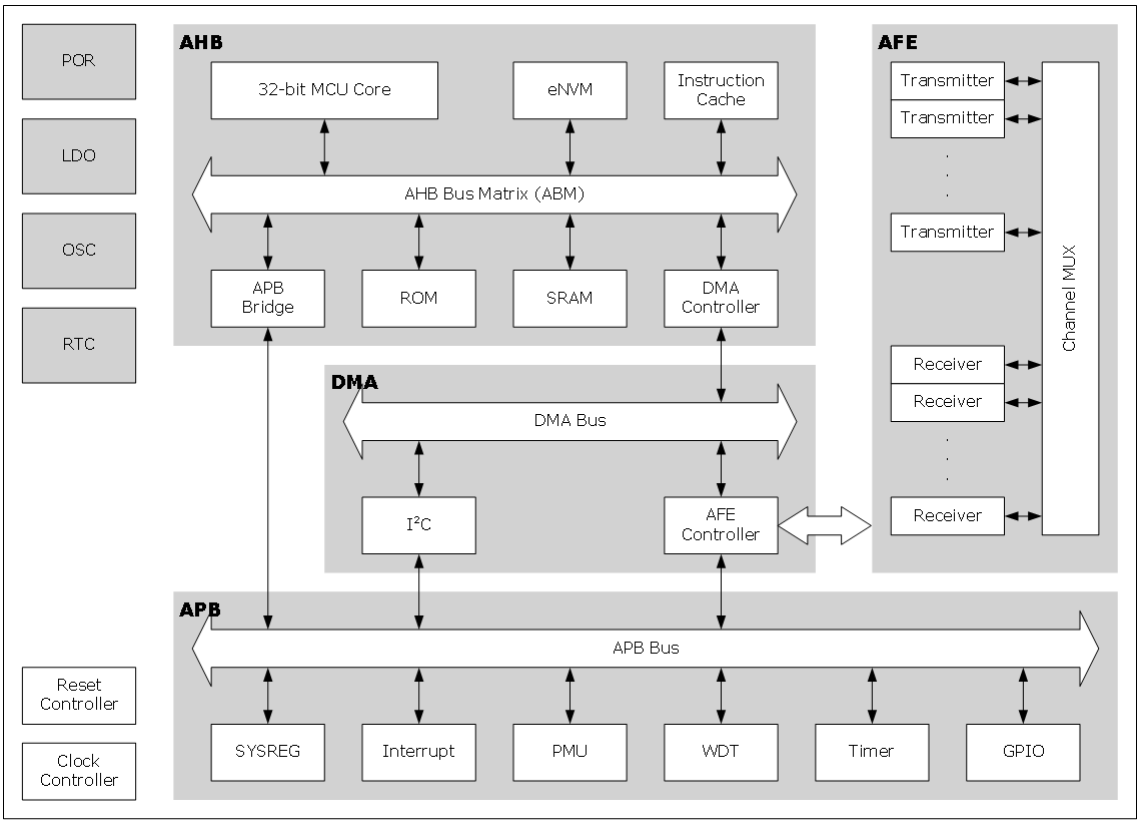
No external components except bypass filter capacitors for the power supply are needed.



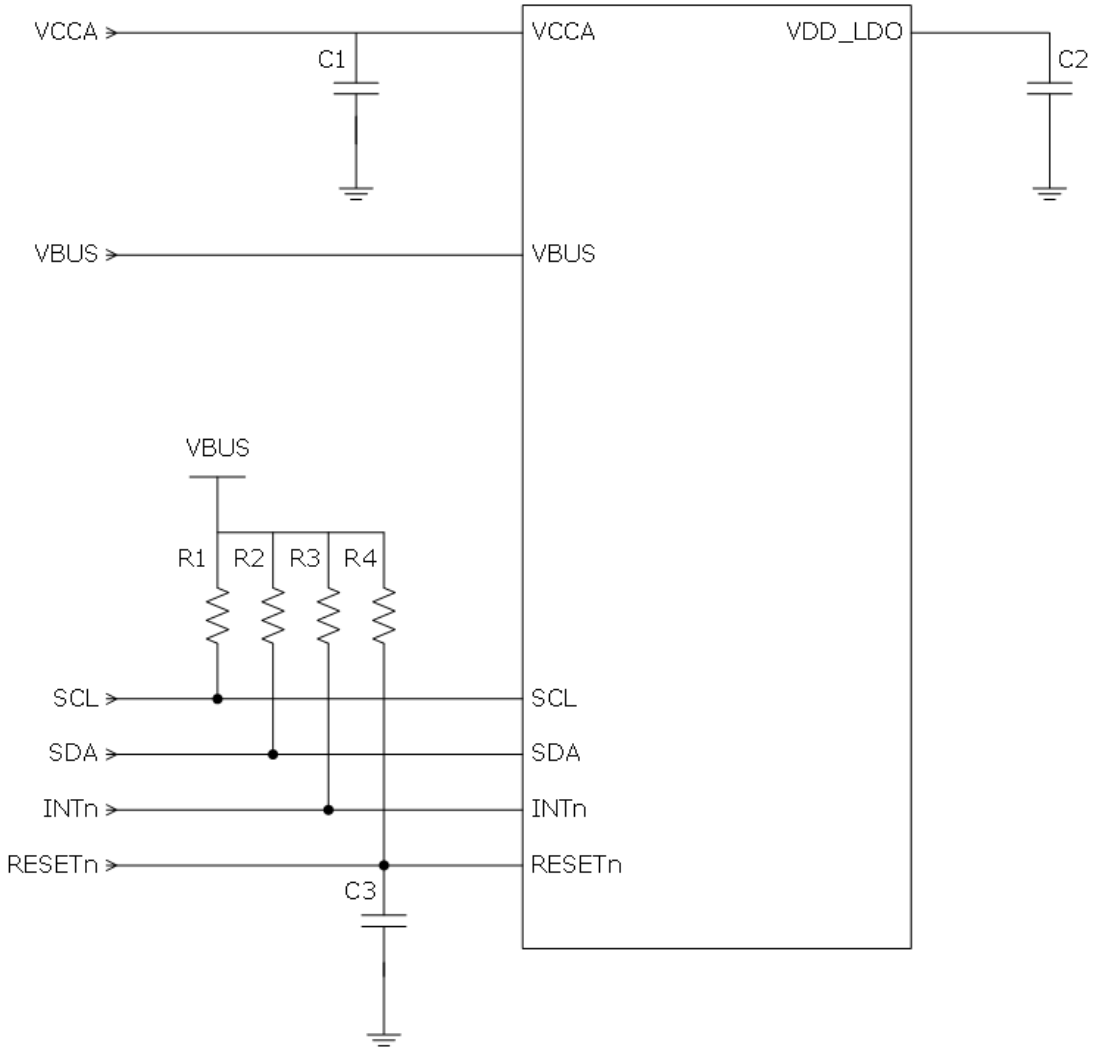
25 Ball WLCSP (TOP VIEW) assignments

2. HARDWARE DESCRIPTIONS

2.1 BLOCK DIAGRAM



2.1.1 I2C HOST INTERFACE



C1	C2	C3 (NOTE1)	R1	R2	R3	R4 (NOTE1)
1uF/6.3V	0.1uF/6.3V	0.1uF/6.3V	2.2KΩ	2.2KΩ	2.2KΩ	10KΩ

[NOTE]
1. R4 and C3 are optional components. RESET pin can be tied to VCCA directly.

2.2 PIN ASSIGNMENT

(NOTES)
Suffix 'n' in "XXXn" means the low level assertion. Negation value for suffix 'n' signals shall be the logic 'HIGH'.

25	PIN NAME	TYPE	FUNCTION
A1	X01	O	X forcing 01
A2	X00	O	X forcing 00
A3	VDD_LDO	PWR	LDO Output
A4	VCCA	PWR	Analog power supply
A5	SCL	OD	I^2C clock
B1	X03	O	X forcing 03
B2	X02	O	X forcing 02
B3	RESETn	OD	Reset
B4	INTn	OD	Interrupt to Host
B5	SDA	OD	I^2C data
C1	X04	O	X forcing 04
C2	X05	O	X forcing 05
C3	GND	PWR	Ground
C4	KEY	I	Wake up Key
C5	VBUS	PWR	Interface power
D1	X06	O	X forcing 06
D2	Y01	I	Y sensing 01
D3	Y03	I	Y sensing 03
D4	Y05	I	Y sensing 05
D5	Y07	I	Y sensing 07
E1	X07	O	X forcing 07
E2	Y00	I	Y sensing 00
E3	Y02	I	Y sensing 02
E4	Y04	I	Y sensing 04
E5	Y06	I	Y sensing 06

3. ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VCCA	Analog power supply voltage (1)	-0.5	-	4.0	V
V_{IN}	Input voltage for I/O bus (1)	-0.5	-	4.0	V
I_{IN}	DC input current (1)	-	-	50	mA
I_{OUT}	Output short circuit current (1)	-	-	50	mA
T_{STG}	Storage temperature (6)	-65	-	+150	°C
V_{ESD1}	Electrostatic handling HBM (3)	-4000	-	+4000	V
V_{ESD2}	Electrostatic handling MM (4)	-250	-	+250	V

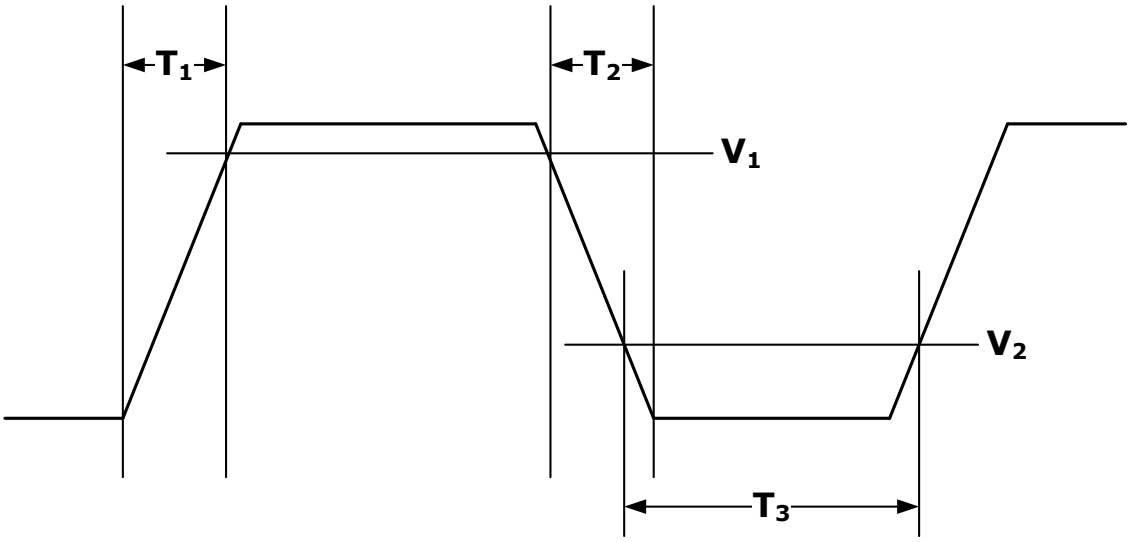
(NOTES)

1. Either voltage limit or current limit is sufficient to protect inputs.
2. Maximum ratings are defined based on the wide voltage
3. Equivalent to discharging a 100pF capacitor through a 1.5 kΩ series resistor.
4. Equivalent to discharging a 200pF capacitor through a 0 kΩ series resistor.
5. Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the recommended conditions
6. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

3.2 RECOMMENDED OPERATING CONDITIONS

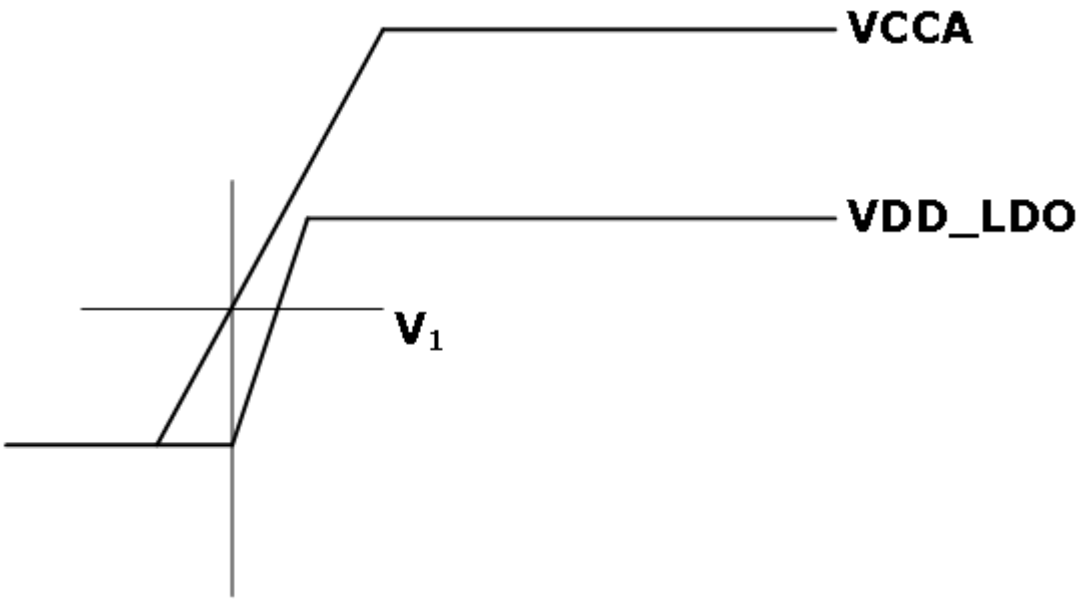
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VCCA	Analog power supply voltage	2.7	3.3	3.6	V
T_{OPT}	Operation environment temperature	-20	-	85	°C
T_J	Junction temperature	-40		125	°C

3.3 POWER UP CONDITION



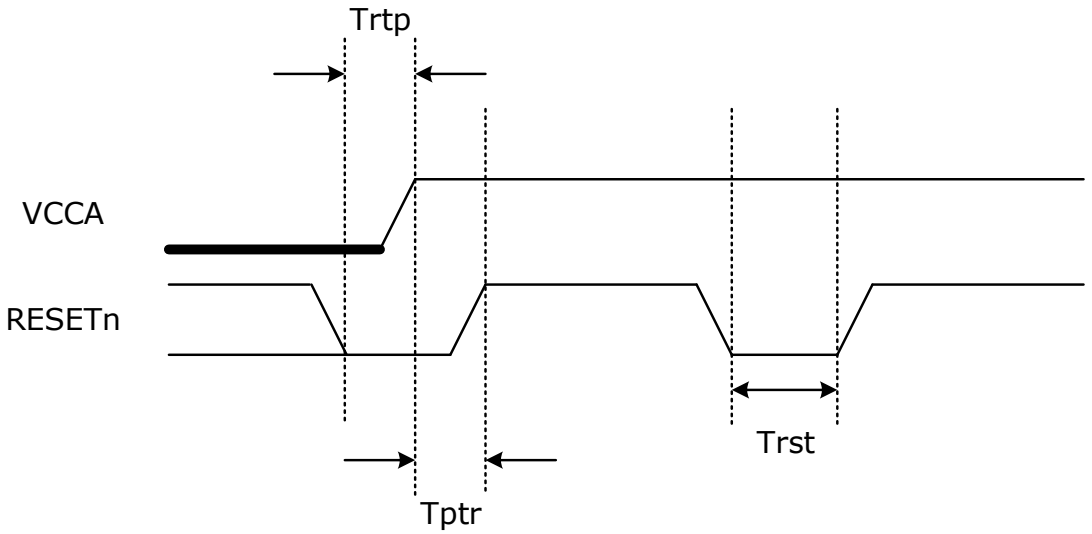
SYMBOL	PARAMETER	MIN	MAX	UNIT
T_1	Power-on time	-	10ms@V_1=2.7V	ms
T_2	Power-off time	-	10ms@V_2=0.3V	ms
T_3	From power-off to power-on time	20	-	ms

3.4 LDO



SYMBOL	PARAMETER	MIN	MAX	UNIT
V_1	LDO start-up threshold	0.7	1.0	V

3.5 Reset Sequence



SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{rtp}	Reset to low time before power-on	0	-	us
T_{ptr}	Reset time after power-on	1	-	ms
T_{rst}	Reset time	1	-	ms

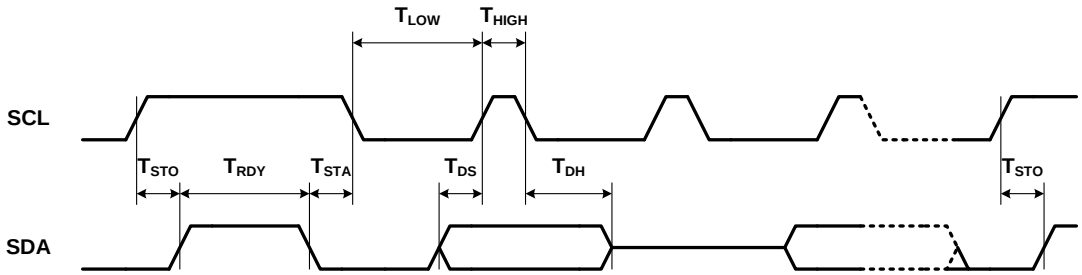
3.5 HOST INTERFACE I/O CHARACTERISTICS

3.5.1 I2C INTERFACE

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	0	-	3.6	V
V_{OUT}	Output voltage range	0	-	VBUS	V
V_{IH}	Input threshold voltage for logic HIGH	1.2	-	-	V
V_{IL}	Input threshold voltage for logic LOW	-	-	0.6	V
V_{OL}	Output voltage for logic LOW	-	-	0.4	V
RPU	Input pull-up resistance	none	none	none	KΩ

(NOTE)
1. I_O = 4mA
2. VBUS is defined by the pull-up voltage

3.5.2 I2C INTERFACE TIMING



SYMBOL	PARAMETER	FAST-MODE		HS-MODE		UNIT
		MIN	MAX	MIN	MAX	
F_{SCL}	SCL clock frequency	0	400	0	1000	KHz
T_{LOW}	LOW period of SCL	1300	-	500	-	ns
T_{HIGH}	HIGH period of SCL	600	-	260	-	ns
T_{STA}	Hold time for START condition	600	-	260	-	ns
T_{STO}	Setup time for STOP condition	600	-	260	-	ns
T_{DH}	Data hold time	0	900	0	900	ns
T_{DS}	Data set-up time	100	-	50	-	ns
T_{rC}	Rise time of SCL	20	300	20	120	ns
T_{fC}	Fall time of SCL	20	300	20	120	ns
T_{rD}	Rise Time of SDA	20	300	20	120	ns
T_{fD}	Fall time of SDA	20	300	20	120	ns
T_{RDY}	Ready time between STOP and START condition	20	-	20	-	us

3.5.3 INTERRUPT

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	0	-	3.6	V
V_{OUT}	Output voltage range	0	-	VBUS	V
V_{IH}	Input threshold voltage for logic HIGH	1.2	-	-	V
V_{IL}	Input threshold voltage for logic LOW	-	-	0.6	V
V_{OL}	Output voltage for logic LOW	-	-	0.4	V
RPU	Input pull-up resistance	none	none	none	KΩ

(NOTE)
1. I_O = 4mA
2. VBUS is defined by the pull-up voltage

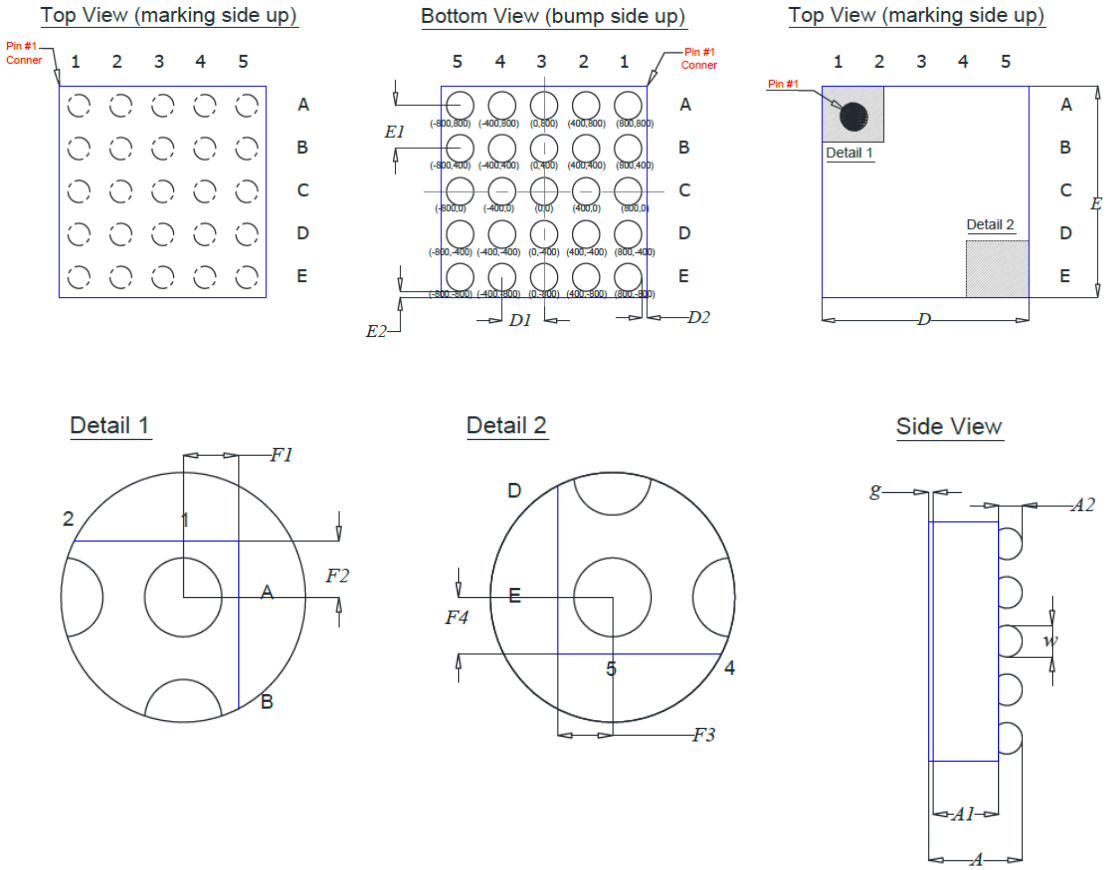
3.6 TX

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage range	0	-	3.3	V
F_{CLK}	TX clock frequency	1	-	2000	KHz
T_{rise}	Rising time	5	-	60	ns
T_{fall}	Falling time	5	-	60	ns

3.7 RX

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	0	-	3.6	V

3.8 Package Information (25-ball WLCSP)



Unit : mm

DIMENSION				
Symbols	MIN	NOM	MAX	NOTE
A	0.432	0.470	0.508	± 0.038
A 1	0.230	0.245	0.260	± 0.015
A 2	0.180	0.200	0.220	± 0.020
D		1.970		± 0.030
E		1.970		± 0.030
D1		0.400		
D2		0.055		
E1		0.400		
E2		0.055		
F1		0.185		Ball center to die edge
F2		0.185		Ball center to die edge
F3		0.185		Ball center to die edge
F4		0.185		Ball center to die edge
g	0.022	0.025	0.028	± 0.003
w	0.234	0.260	0.286	± 0.026

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