Osptek Display

TFT LCD SPECIFICATION

Model No:

YDP400BT001-V4

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by Shenzhen Osprey Optoelectronics Technology Co., Ltd.
LCD specification: Dots 720xRGBx720
As to basic specification of the driver IC, refer to the IC (Sitronix：ST7703I) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

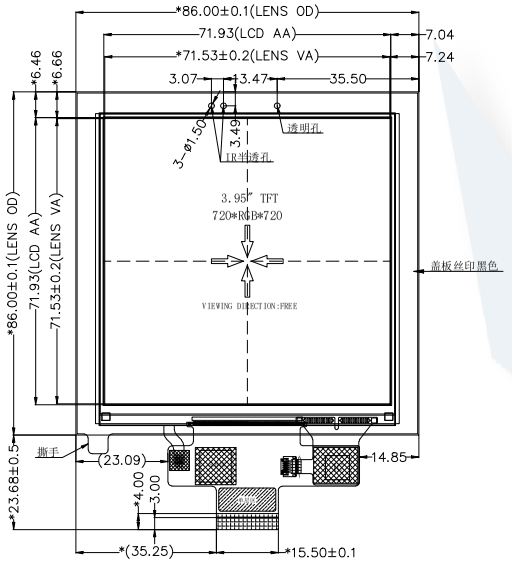
Structure: TFT PANNEL+IC +FPC+BL+CTP;
ALL Viewing Type LCD
720 dot-segment and 720 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

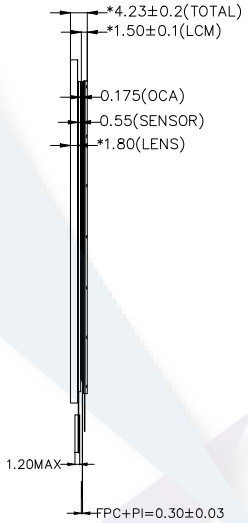
1.3 Applications:

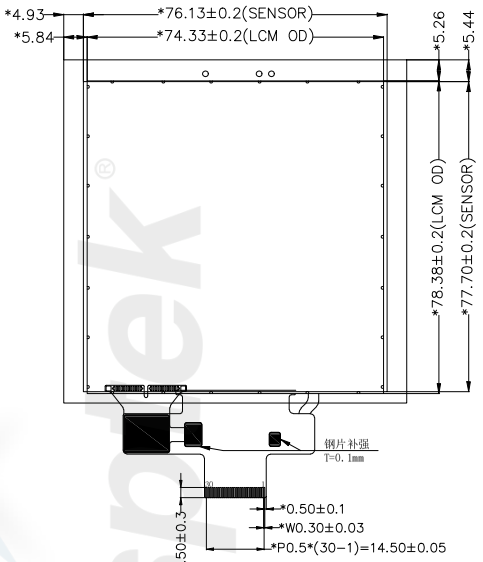
2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	720*3RGB(H)X720(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.0999 (H) x 0.0999 (V)	mm
Active area	71.93(H) x 71.93(V)	mm
Viewing direction	ALL Viewing	--
TFT Driver IC	ST7703I	--
TFT interface	4lane MIPI Interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	74.33(W) ×78.38(H) ×1.50(T)	mm
LCM+CTP Size(W*H*T)	86.00(W) ×86.00(H) ×4.23(T)	mm
Touch structure	G+G	--
Touch Driver IC	GT911	--
Touch Interface	I2C	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
00	First Desing	2023.02.10	
01	盖板厚度由0.7mm改为1.8mm	2023.05.25	







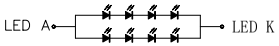
FPC展开出货

PIN	Explanation
1	LEDA
2	LEDK
3	LEDK
4	VCI
5	IOVCC
6	RESET
7	TE
8	PWM
9	GND
10	D0_P
11	D0_N
12	GND
13	D1_P
14	D1_N
15	GND
16	CLK_P
17	CLK_N
18	GND
19	D2_P
20	D2_N
21	GND
22	D3_P
23	D3_N
24	GND
25	TP_INT
26	TP_SDA
27	TP_SCL
28	TP_RST
29	TP_VCC
30	TP_VCC

技术参数：
1.结构：G+G
Cover LENS:旭硝子0.7mm
IC型号：GT911
2.工作电压：2.8V-3.3V
3.透光率：≥82%
4.表面硬度：6H
5.工作环境：-20℃~+60℃
6.储存环境：-30℃~+70℃
7.未注尺寸公差按±0.1mm

PIN	定义
1	VCC
2	RST
3	SCL
4	SDA
5	INT
6	GND

NOTES:
1. DISPLAY TYPE: 3.95", 720*720 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: 80/80/80/80(TYP)
4. DRIVER IC:ST7703I
5. LCM (White 9 AVG 1/6) :
   Brightness: TBDcd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 8 chip white LEDs If=40mA,Vf=11.2V~12.8V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



深圳市鱼鹰光电科技有限公司				Mobile:	
PART NO.:	YDP400BT001-V4			MODULE NO.:	01
DRAWN BY:	LIU	DATE:	2023.05.25	PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
TP Operating Temperature & Humidity (20% ~ 90%RH)	T_{OPR}	-20	+60	°C
TP SStorage Temperature & Humidity (20% ~ 90%RH)	T_{STG}	-30	+70	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V
Current Consumption	I_{DD}	--	--	--	mA
	$I_{DD-SLEEP}$	--	--	--	uA

4.2 Back-Light Unit Characeristics

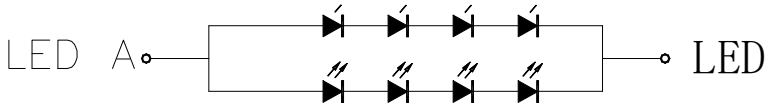
The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	11.2		12.8	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD+CTP)	Lv	--	TBD	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDK	Power supply for backlight cathode input terminal.	
3	LEDK	Power supply for backlight cathode input terminal.	
4	VCI	Power Supply For LCD.	
5	IOVCC	Power Supply For I/O.	
6	RESET	Reset signal input terminal. Active at ‘L’.	
7	TE	Frame head pulse for tearing effect.	
8	PWM	PWM (Pulse Width Modulation) Signal Of LED Driving.	
9	GND	Power Ground	
10	D0_P	Positive polarity of low voltage differential data 0 signal	
11	D0_N	Negative polarity of low voltage differential data 0 signal	
12	GND	Power Ground	
13	D1_P	Positive polarity of low voltage differential data 1 signal	
14	D1_N	Negative polarity of low voltage differential data 1 signal	
15	GND	Power Ground	
16	CLK_P	Positive polarity of low voltage differential clock signal	
17	CLK_N	Negative polarity of low voltage differential clock signal	
18	GND	Power Ground	
19	D2_P	Positive polarity of low voltage differential data 2 signal	
20	D2_N	Negative polarity of low voltage differential data 2 signal	
21	GND	Power Ground	
22	D3_P	Positive polarity of low voltage differential data 3 signa	
23	D3_N	Negative polarity of low voltage differential data 3 signal	
24	GND	Power Ground	
25	CTP_INT	CTP_STOP Singnal	
26	CTP_SDA	CTP_Data Singnal	
27	CTP_SCL	CTP_Clock Singnal	
28	CTP_RST	CTP_Reset Signal input pin.	
29	CTP_VCC	CTP_Power Supply 2.8V~3.3V	
30	CTP_VCC	CTP_Power Supply 2.8V~3.3V	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

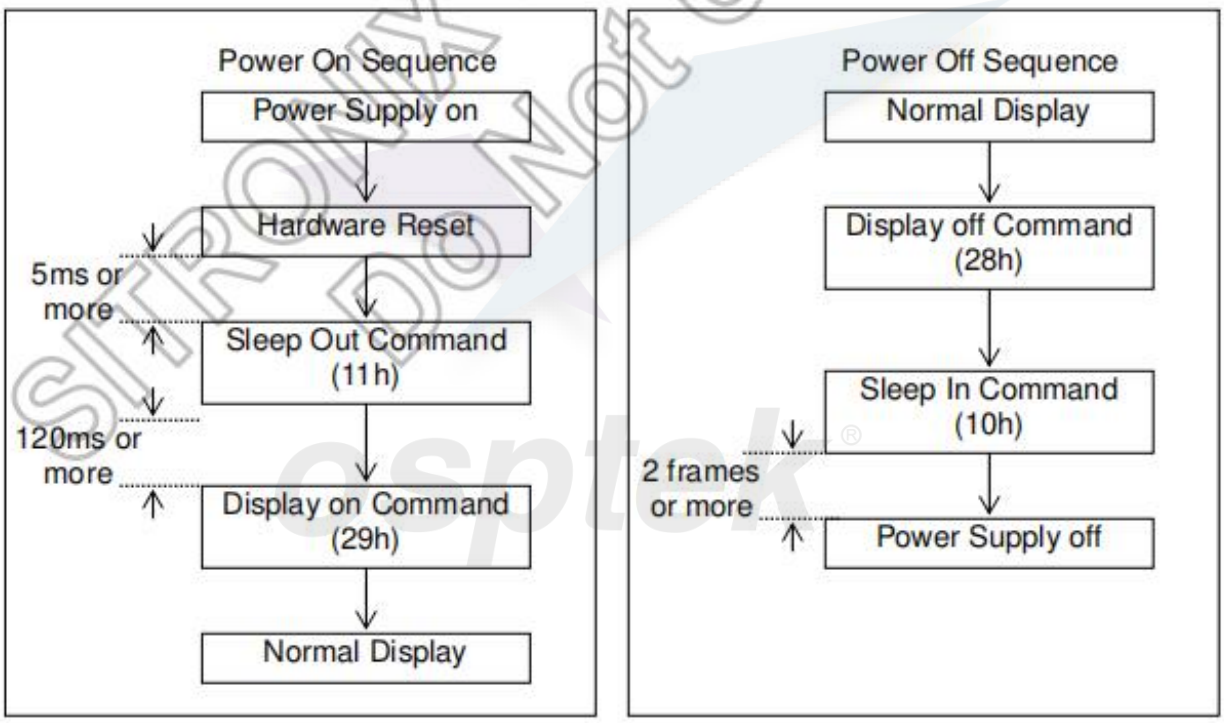


Figure 5.32: The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

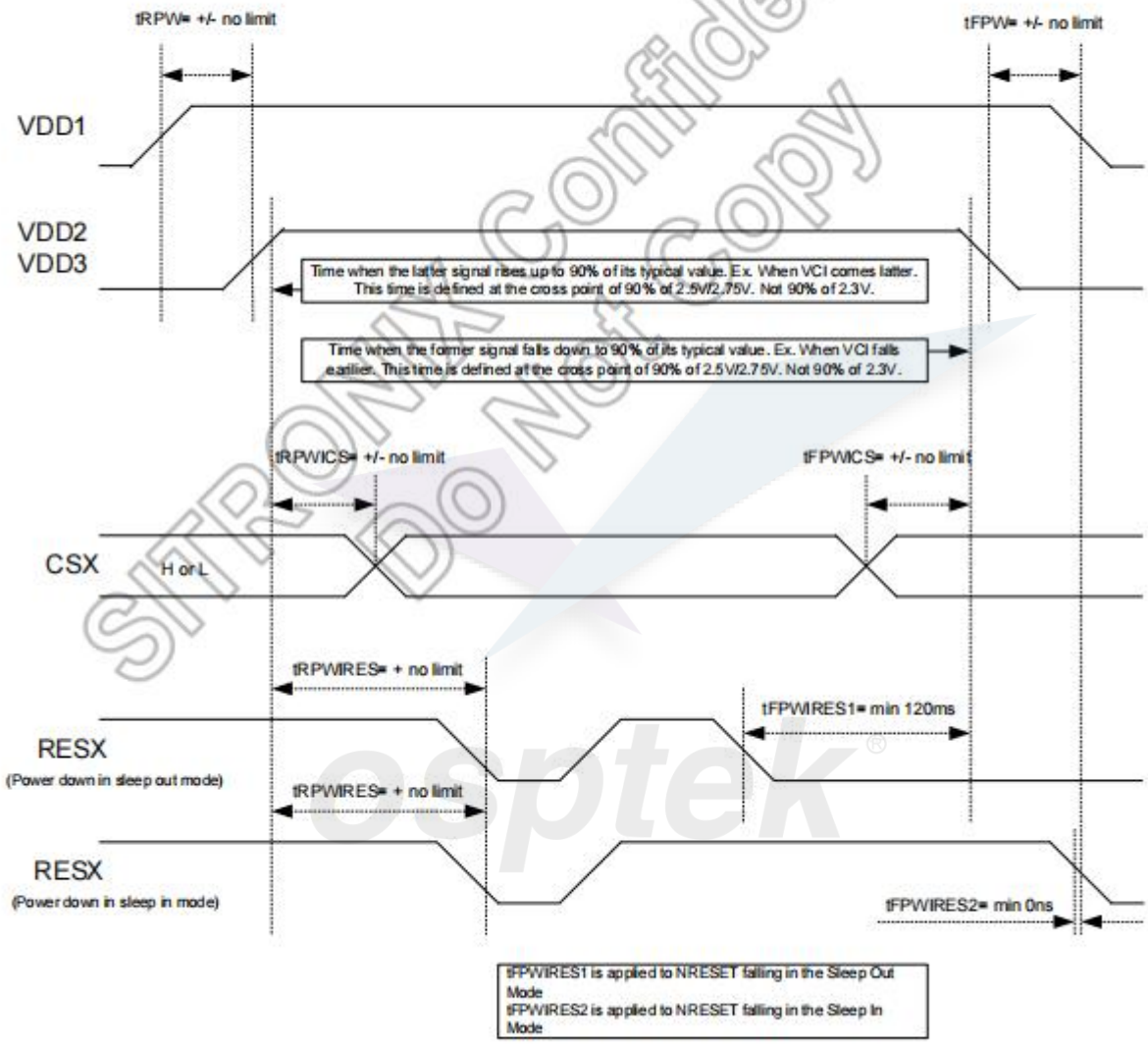
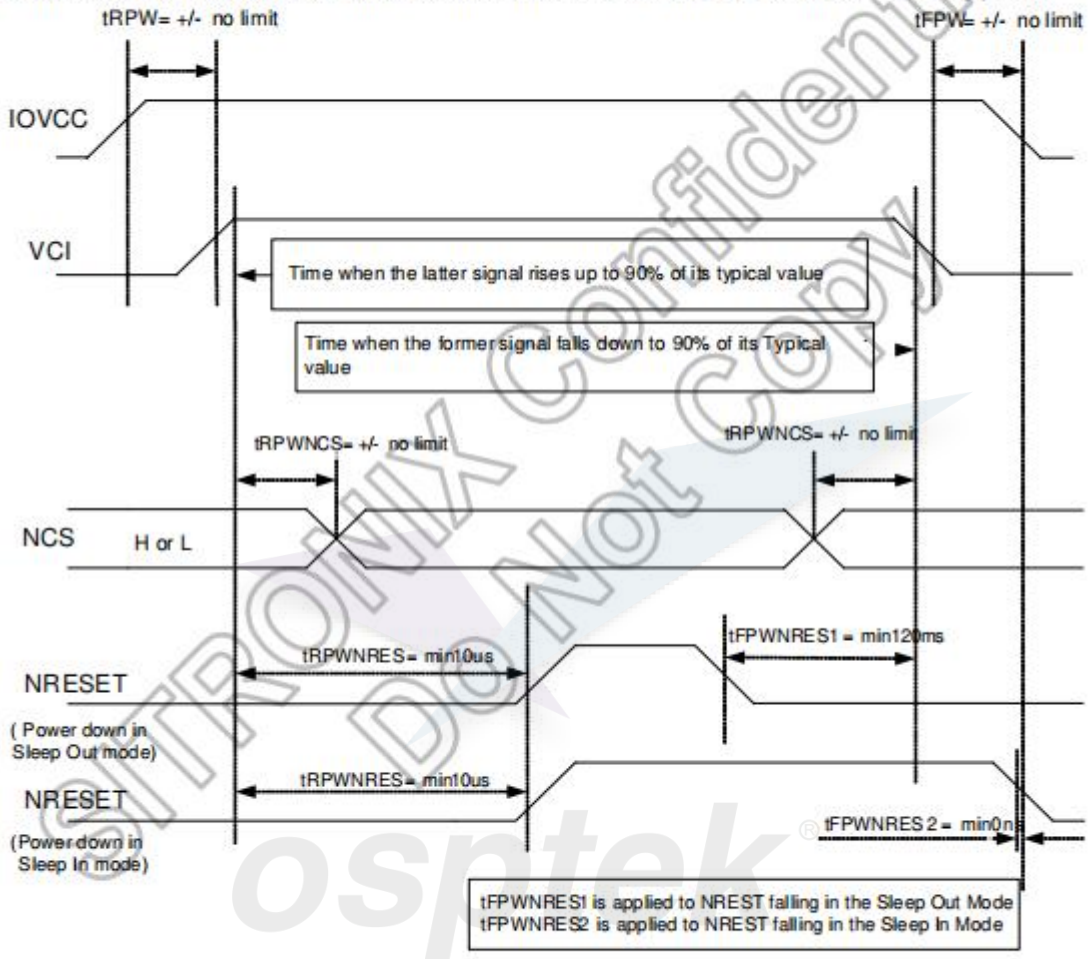


Figure 5.33: Case 1: RESX line is held high or unstable by host at power on

Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.34: Case 2: RESX line is held low by host at power on

DSI-MIPI Interface Timing Characteristics of IC

High Speed Mode

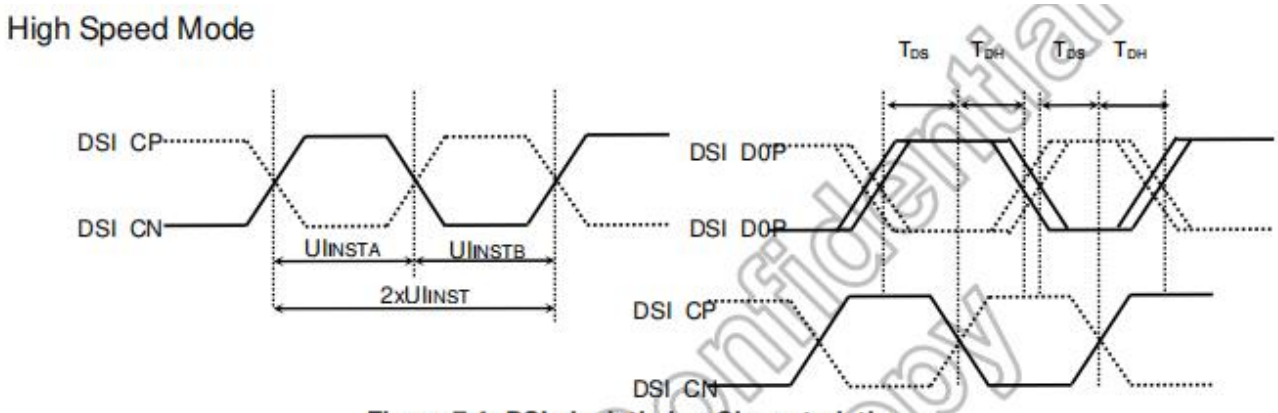


Figure 7.4: DSI clock timing Characteristics

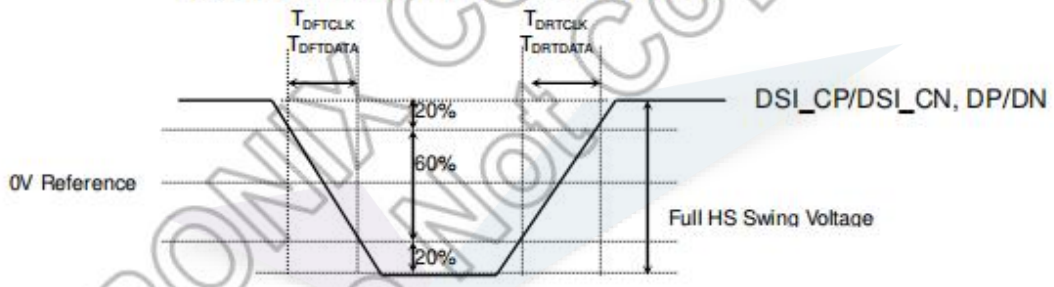


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

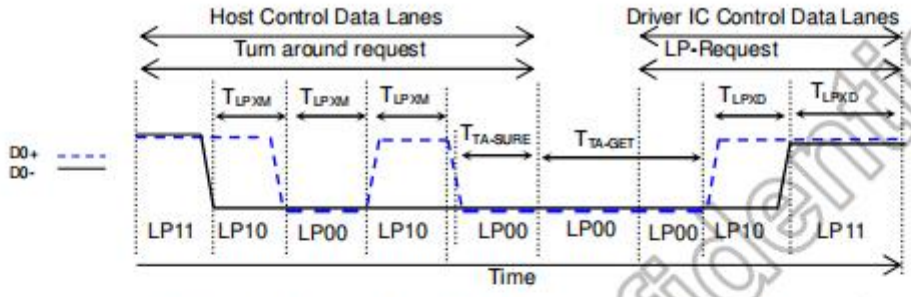


Figure 7.6: BTA from HOST to Display Module Timing

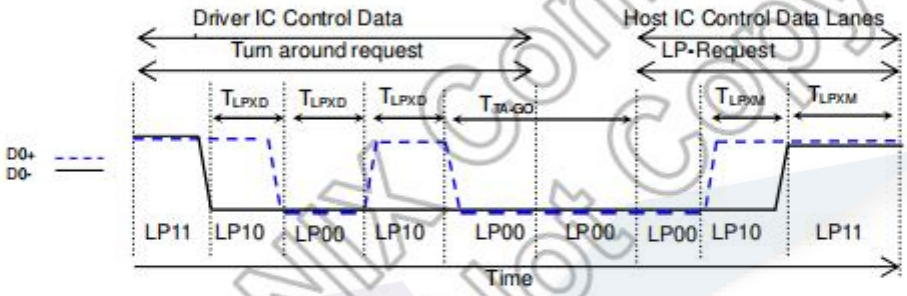


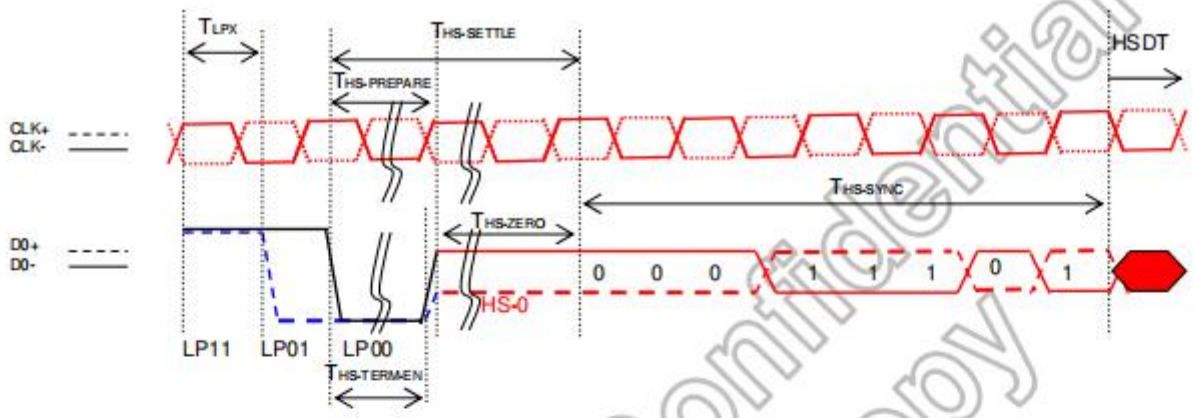
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

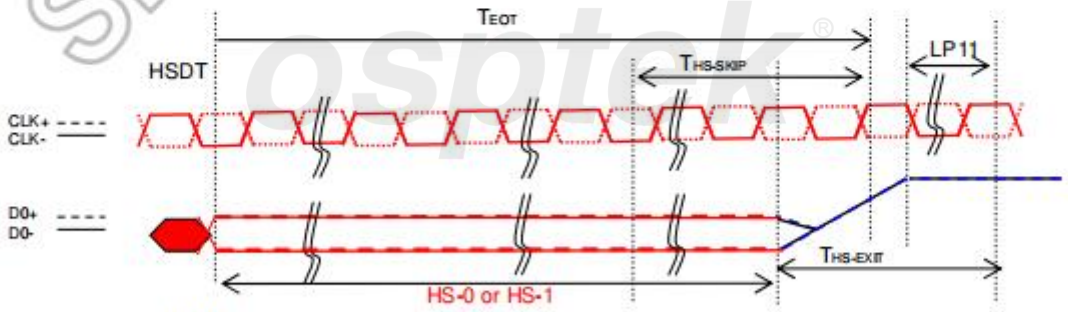
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

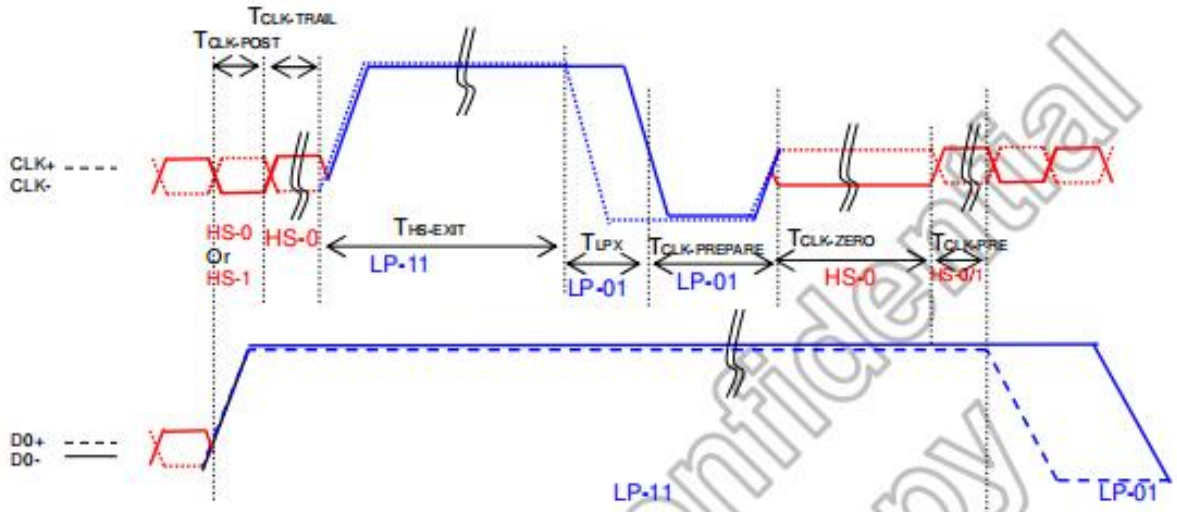
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

Reset Description:

Reset input timing

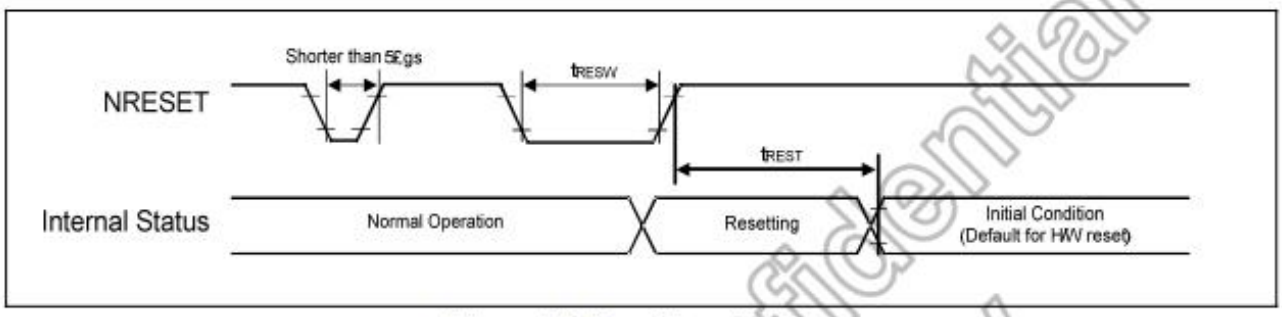


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

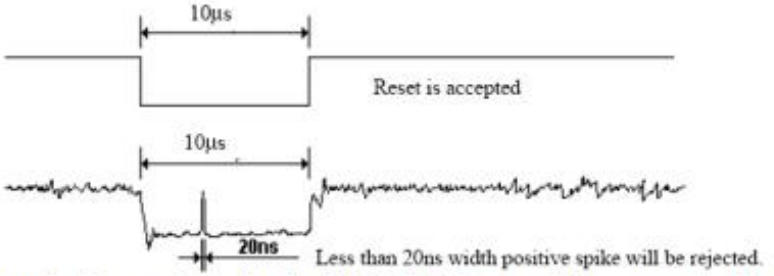
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	Θ3	CR>10	80	85	-	°	Note 1
		Θ9		80	85	-	°	
	Vertical	Θ12		80	85	-	°	
		Θ6		80	85	-	°	
Contrast Ratio		CR	Θ= 0°	800	1000	-		Note 2
Luminance		cd/m2	Θ= 0°	-	-	-		
Uniformity		%	Θ= 0°	-	-	-		
Transmittance		T(%)	Θ= 0°	4.2	4.8	-		With APF
NSTC		%	Θ= 0°	63	68	-		
Reproduction Of color	Red	Rx	Θ= 0°					Note 3 *Color filter Glass(with out OC with C light)
		Ry						
	Green	Gx						
		Gy						
	Blue	Bx						
		By						
White		Wx	Θ= 0°	0.281	0.296	0.311		
		Wy		0.304	0.319	0.334		
Response Time		Tr+Tf	Θ= 0°	-	25	35	ms	Note 4

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are

determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'dock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).

2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 2) Luminance Contrast Ratio (CR) is defined mathematically.

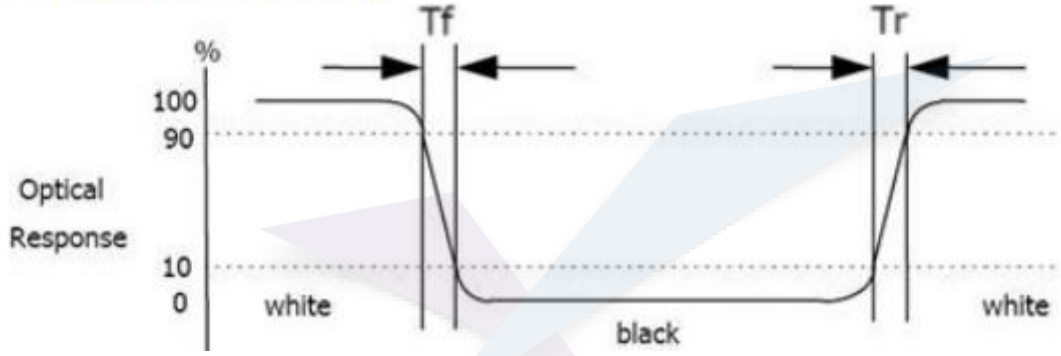
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table1 shall be calculated from The spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the Color filter Glass.

4. The electro-optical response time measurements shall be made as FIG.4 by switching the "data" input signal ON and OFF.

The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Tf.

Figure 1 Response Time Testing



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~60℃（30min），10 cycles	

9. Packing Method----TBD

- END -