ST7802

Datasheet

Version 0.3

2024/06

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST7802, a 16.7M-color single-chip controller/driver for LTPS AMOLED, is capable of supporting up to 480RGBx600 with internal display data RAM. The 240-channel source driver has true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter.

The ST7802 provides several system interfaces, which include 8-bit parallel interface, SPI, Dual-SPI, Multi-SPI and MIPI interface. While host send display data through these interfaces, ST7802 stores display data, which is 1/2 compressed, in the on-chip display data RAM of 3,456,000 bits. In addition, because of the integrated power circuit, it is possible to make a display system with zero capacitor.

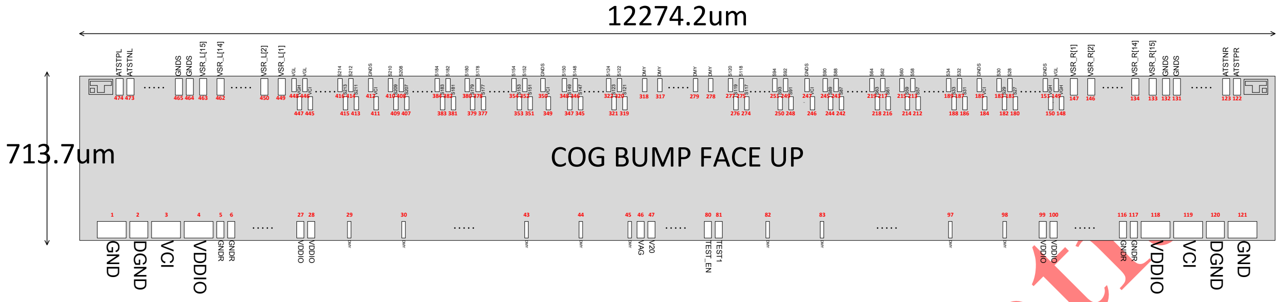
2 FEATURES

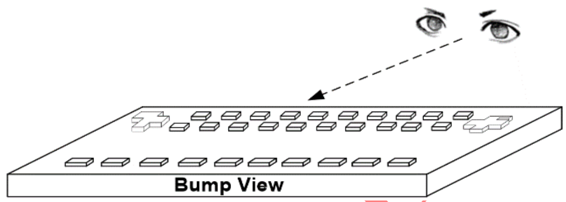
- Single Chip AMOLED Controller/Driver with Display RAM
- Display Resolution
  - 480RGBx600
  - 480RGBx480
  - 454RGBx454
  - 390RGBx390
  - 368RGBx448
  - 320RGBx360
  - 320RGBx320
  - 300RGBx300
  - 240RGBx240
  - 240RGBx720
  - 128RGBx128
  - Others: configurable by registers
- Display RAM
  - 3,456,000 bits
- Display Mode
  - Full Color Mode: 16.7M colors
  - Idle Mode: 16.7M, 4096, 8 colors
- Interface
  - 8 bit parallel interface
  - SPI, Dual-SPI, Multi-SPI
  - MIPI Display Serial Interface (1 clock and 1 data lane pairs, Max: 550Mbps)
- Display Features
  - 5 sets (HBM / idle / normal123) of gamma curve with separated RGB gamma setting
  - Partial display
  - Low frame rate selection
  - Zigzag cancellation(R-corner/Curved-edge/Notch)
  - Subpixel rendering compensation
  - Brightness control: Linear or Gamma curve
- Control External Power IC by Single Wire signal
- On Chip Build-In Circuits
  - VREFP/VREFN1/VREFN2 for panel voltage
  - VGH/VGL for gate control signal
  - Internal OSC for display clock

  - Source output 1:6 / 1:9 / 1:12 MUX
- Power Supply
  - I/O voltage (to DGND): 1.65V ~ 3.6V
  - Analog voltage (VCI to GND) : 2.7V ~ 3.6V
- On Chip Power System
  - Gate driver HIGH level (VGH to GND): VCI, +3.6V ~ +10.0V
  - Gate driver LOW level (VGL to GND): -10.0V ~ -3.6V
  - Positive reference voltage (VREFP to GND): +0.5V ~ +5.0V
  - Negative reference voltage (VREFN to GND): -4.5V ~ -0.5V
  - Negative reference voltage (VREFN2 to GND): -4.5V ~ -0.5V
  - Gamma HIGH level (VGMP to GND): +2.0V ~ +6.3V
  - Gamma LOW level (VGSP to GND): +0.15V ~ +4.5V
- Package
  - COF/COG

3 PAD ARRANGEMENT

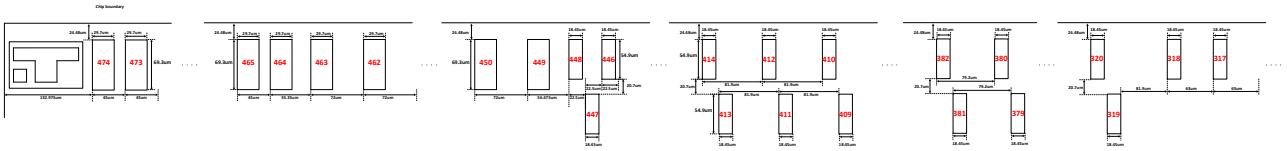
3.1 Bump Dimension



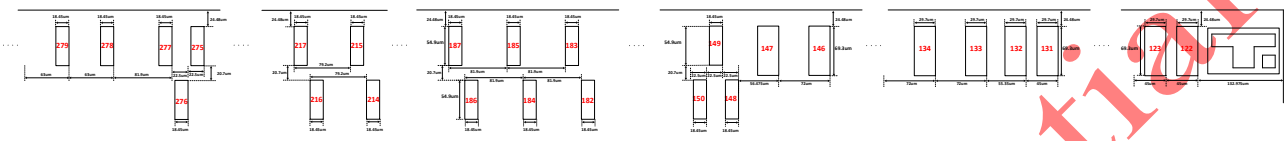


Au bump height	9 µm (COG)
Au bump size	**Gate :** 29.7µm x 69.3µm **Source :** 18.45µm x 54.9µm **Input Dummy :** 14.85um x 69.3um **Input Pads :** 119.7µm x 69.3µm; 74.7um x 69.3um; 29.7um x 69.3um

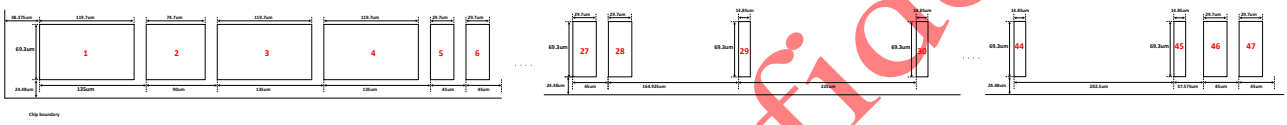
- **Output Pads Left**



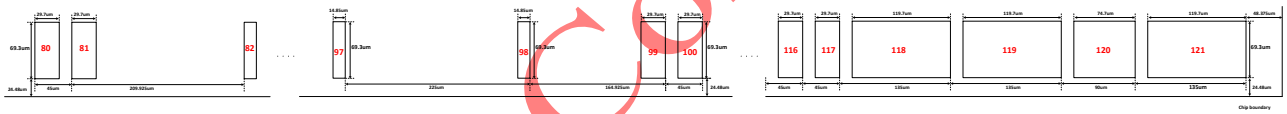
Output Pads Right



- **Input Pads Left**

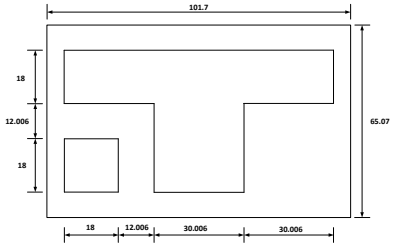


- **Input Pads Right**

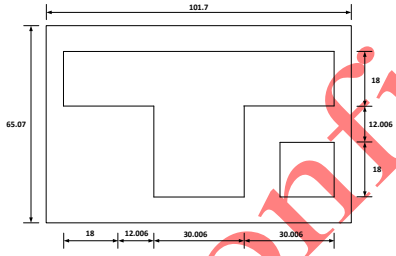


3.2 Alignment Mark Dimension

Alignment Mark ALIGN_L : (X,Y)=(-6071.4, 295.605)



Alignment Mark ALIGN_R : (X,Y)=(+6071.4, 295.605)



3.3 Chip Information

Chip size	12274.2μm x 713.7μm
Chip thickness	200 μm
Pad Location	Pad center
Coordinate Origin	Chip center

4 PAD CENTER COORDINATES

PAD No.	Pad Name	X	Y
1	GND	-6030	-297.72
2	DGND	-5917.5	-297.72
3	VCI	-5805	-297.72
4	VDDIO	-5670	-297.72
5	GNDR	-5580	-297.72
6	GNDR	-5535	-297.72
7	VPP	-5490	-297.72
8	IM1	-5445	-297.72
9	CSX	-5400	-297.72
10	DCX	-5355	-297.72
11	D7	-5310	-297.72
12	D6	-5265	-297.72
13	D5	-5220	-297.72
14	D4	-5175	-297.72
15	D3	-5130	-297.72
16	D2	-5085	-297.72
17	D1	-5040	-297.72
18	D0	-4995	-297.72
19	RESXL	-4950	-297.72
20	WRX_SCL	-4905	-297.72
21	IM0	-4860	-297.72
22	RDX	-4815	-297.72
23	TEL	-4770	-297.72
24	TE1L	-4725	-297.72
25	SWIREL	-4680	-297.72
26	DGND	-4635	-297.72
27	VDDIO	-4590	-297.72
28	VDDIO	-4545	-297.72
29	DMY	-4387.5	-297.72
30	DMY	-4162.5	-297.72
31	DMY	-3937.5	-297.72
32	DMY	-3712.5	-297.72
33	DMY	-3487.5	-297.72
34	DMY	-3262.5	-297.72
35	DMY	-3037.5	-297.72
36	DMY	-2812.5	-297.72
37	DMY	-2587.5	-297.72
38	DMY	-2362.5	-297.72
39	DMY	-2137.5	-297.72
40	DMY	-1912.5	-297.72
41	DMY	-1687.5	-297.72
42	DMY	-1462.5	-297.72
43	DMY	-1237.5	-297.72
44	DMY	-1012.5	-297.72
45	DMY	-810	-297.72
46	VAG	-765	-297.72
47	V20	-720	-297.72
48	GNDG	-675	-297.72
49	VCI	-630	-297.72
50	AVDDG	-585	-297.72
51	AVDDG	-540	-297.72
52	VGMP	-495	-297.72
53	VGSP	-450	-297.72
54	GNDG	-405	-297.72
55	AVDD	-360	-297.72
56	AVDD	-315	-297.72
57	GNDG	-270	-297.72
58	VCL	-225	-297.72
59	VCL	-180	-297.72
60	GND	-135	-297.72
61	DTEST0	-90	-297.72
62	DTEST1	-45	-297.72
63	DTEST2	0	-297.72
64	DTEST3	45	-297.72
65	DTEST4	90	-297.72
66	DTEST5	135	-297.72
67	DTEST6	180	-297.72
68	DTEST7	225	-297.72
69	VDDIO	270	-297.72
70	VDDIO	315	-297.72
71	DGND	360	-297.72
72	DGND	405	-297.72
73	DVDD	450	-297.72
74	DVDD	495	-297.72
75	TESTIN1	540	-297.72
76	TESTIN2	585	-297.72
77	TESTIN3	630	-297.72
78	TESTIN4	675	-297.72
79	EXTCLK	720	-297.72
80	TEST_EN	765	-297.72
81	TEST1	810	-297.72
82	DMY	1012.5	-297.72
83	DMY	1237.5	-297.72
84	DMY	1462.5	-297.72
85	DMY	1687.5	-297.72
86	DMY	1912.5	-297.72
87	DMY	2137.5	-297.72
88	DMY	2362.5	-297.72
89	DMY	2587.5	-297.72
90	DMY	2812.5	-297.72
91	DMY	3037.5	-297.72
92	DMY	3262.5	-297.72
93	DMY	3487.5	-297.72
94	DMY	3712.5	-297.72
95	DMY	3937.5	-297.72
96	DMY	4162.5	-297.72

PAD No.	Pad Name	X	Y
97	DMY	4387.5	-297.72
98	DMY	4612.5	-297.72
99	VDDIO	4770	-297.72
100	VDDIO	4815	-297.72
101	DGND	4860	-297.72
102	DGND	4905	-297.72
103	DCSWAP	4950	-297.72
104	PSWAP	4995	-297.72
105	SWIRER	5040	-297.72
106	TE1R	5085	-297.72
107	TER	5130	-297.72
108	RESXR	5175	-297.72
109	DGND	5220	-297.72
110	CKP	5265	-297.72
111	CKN	5310	-297.72
112	DGND	5355	-297.72
113	DP	5400	-297.72
114	DN	5445	-297.72
115	DGND	5490	-297.72
116	GNDR	5535	-297.72
117	GNDR	5580	-297.72
118	VDDIO	5670	-297.72
119	VCI	5805	-297.72
120	DGND	5917.5	-297.72
121	GND	6030	-297.72
122	ATSTPR	5990.4	297.72
123	ATSTNR	5945.4	297.72
124	VGL	5900.4	297.72
125	VGH	5855.4	297.72
126	VGL	5810.4	297.72
127	VREFP	5765.4	297.72
128	VREFN	5720.4	297.72
129	VREFN2	5675.4	297.72

PAD No.	Pad Name	X	Y
130	GNDG	5630.4	297.72
131	GNDS	5585.4	297.72
132	GNDS	5540.4	297.72
133	VSR_R[15]	5485.05	297.72
134	VSR_R[14]	5413.05	297.72
135	VSR_R[13]	5341.05	297.72
136	VSR_R[12]	5269.05	297.72
137	VSR_R[11]	5197.05	297.72
138	VSR_R[10]	5125.05	297.72
139	VSR_R[9]	5053.05	297.72
140	VSR_R[8]	4981.05	297.72
141	VSR_R[7]	4909.05	297.72
142	VSR_R[6]	4837.05	297.72
143	VSR_R[5]	4765.05	297.72
144	VSR_R[4]	4693.05	297.72
145	VSR_R[3]	4621.05	297.72
146	VSR_R[2]	4549.05	297.72
147	VSR_R[1]	4477.05	297.72
148	VGH	4426.2	229.32
149	VGL	4403.7	304.92
150	VGH	4381.2	229.32
151	GNDS	4358.7	304.92
152	VCI	4336.2	229.32
153	SR	4313.7	304.92
154	S1	4291.2	229.32
155	S2	4268.7	304.92
156	S3	4246.2	229.32
157	S4	4223.7	304.92
158	S5	4201.2	229.32
159	S6	4178.7	304.92
160	S7	4156.2	229.32
161	S8	4133.7	304.92
162	S9	4111.2	229.32

PAD No.	Pad Name	X	Y
163	S10	4088.7	304.92
164	S11	4066.2	229.32
165	S12	4043.7	304.92
166	S13	4021.2	229.32
167	S14	3998.7	304.92
168	S15	3976.2	229.32
169	S16	3953.7	304.92
170	S17	3931.2	229.32
171	S18	3908.7	304.92
172	S19	3886.2	229.32
173	S20	3863.7	304.92
174	S21	3841.2	229.32
175	S22	3818.7	304.92
176	S23	3796.2	229.32
177	S24	3773.7	304.92
178	S25	3751.2	229.32
179	S26	3728.7	304.92
180	S27	3706.2	229.32
181	S28	3683.7	304.92
182	S29	3661.2	229.32
183	S30	3638.7	304.92
184	VCI	3579.3	229.32
185	GNDS	3556.8	304.92
186	S31	3497.4	229.32
187	S32	3474.9	304.92
188	S33	3452.4	229.32
189	S34	3429.9	304.92
190	S35	3407.4	229.32
191	S36	3384.9	304.92
192	S37	3362.4	229.32
193	S38	3339.9	304.92
194	S39	3317.4	229.32
195	S40	3294.9	304.92

PAD No.	Pad Name	X	Y
196	S41	3272.4	229.32
197	S42	3249.9	304.92
198	S43	3227.4	229.32
199	S44	3204.9	304.92
200	S45	3182.4	229.32
201	S46	3159.9	304.92
202	S47	3137.4	229.32
203	S48	3114.9	304.92
204	S49	3092.4	229.32
205	S50	3069.9	304.92
206	S51	3047.4	229.32
207	S52	3024.9	304.92
208	S53	3002.4	229.32
209	S54	2979.9	304.92
210	S55	2957.4	229.32
211	S56	2934.9	304.92
212	S57	2912.4	229.32
213	S58	2889.9	304.92
214	S59	2867.4	229.32
215	S60	2844.9	304.92
216	S61	2788.2	229.32
217	S62	2765.7	304.92
218	S63	2743.2	229.32
219	S64	2720.7	304.92
220	S65	2698.2	229.32
221	S66	2675.7	304.92
222	S67	2653.2	229.32
223	S68	2630.7	304.92
224	S69	2608.2	229.32
225	S70	2585.7	304.92
226	S71	2563.2	229.32
227	S72	2540.7	304.92
228	S73	2518.2	229.32

PAD No.	Pad Name	X	Y
229	S74	2495.7	304.92
230	S75	2473.2	229.32
231	S76	2450.7	304.92
232	S77	2428.2	229.32
233	S78	2405.7	304.92
234	S79	2383.2	229.32
235	S80	2360.7	304.92
236	S81	2338.2	229.32
237	S82	2315.7	304.92
238	S83	2293.2	229.32
239	S84	2270.7	304.92
240	S85	2248.2	229.32
241	S86	2225.7	304.92
242	S87	2203.2	229.32
243	S88	2180.7	304.92
244	S89	2158.2	229.32
245	S90	2135.7	304.92
246	VCI	2083.05	229.32
247	GNDS	2060.55	304.92
248	S91	1994.4	229.32
249	S92	1971.9	304.92
250	S93	1949.4	229.32
251	S94	1926.9	304.92
252	S95	1904.4	229.32
253	S96	1881.9	304.92
254	S97	1859.4	229.32
255	S98	1836.9	304.92
256	S99	1814.4	229.32
257	S100	1791.9	304.92
258	S101	1769.4	229.32
259	S102	1746.9	304.92
260	S103	1724.4	229.32
261	S104	1701.9	304.92

PAD No.	Pad Name	X	Y
262	S105	1679.4	229.32
263	S106	1656.9	304.92
264	S107	1634.4	229.32
265	S108	1611.9	304.92
266	S109	1589.4	229.32
267	S110	1566.9	304.92
268	S111	1544.4	229.32
269	S112	1521.9	304.92
270	S113	1499.4	229.32
271	S114	1476.9	304.92
272	S115	1454.4	229.32
273	S116	1431.9	304.92
274	S117	1409.4	229.32
275	S118	1386.9	304.92
276	S119	1364.4	229.32
277	S120	1341.9	304.92
278	DMY	1260	304.92
279	DMY	1197	304.92
280	DMY	1134	304.92
281	DMY	1071	304.92
282	DMY	1008	304.92
283	DMY	945	304.92
284	DMY	882	304.92
285	DMY	819	304.92
286	DMY	756	304.92
287	DMY	693	304.92
288	DMY	630	304.92
289	DMY	567	304.92
290	DMY	504	304.92
291	DMY	441	304.92
292	DMY	378	304.92
293	DMY	315	304.92
294	DMY	252	304.92

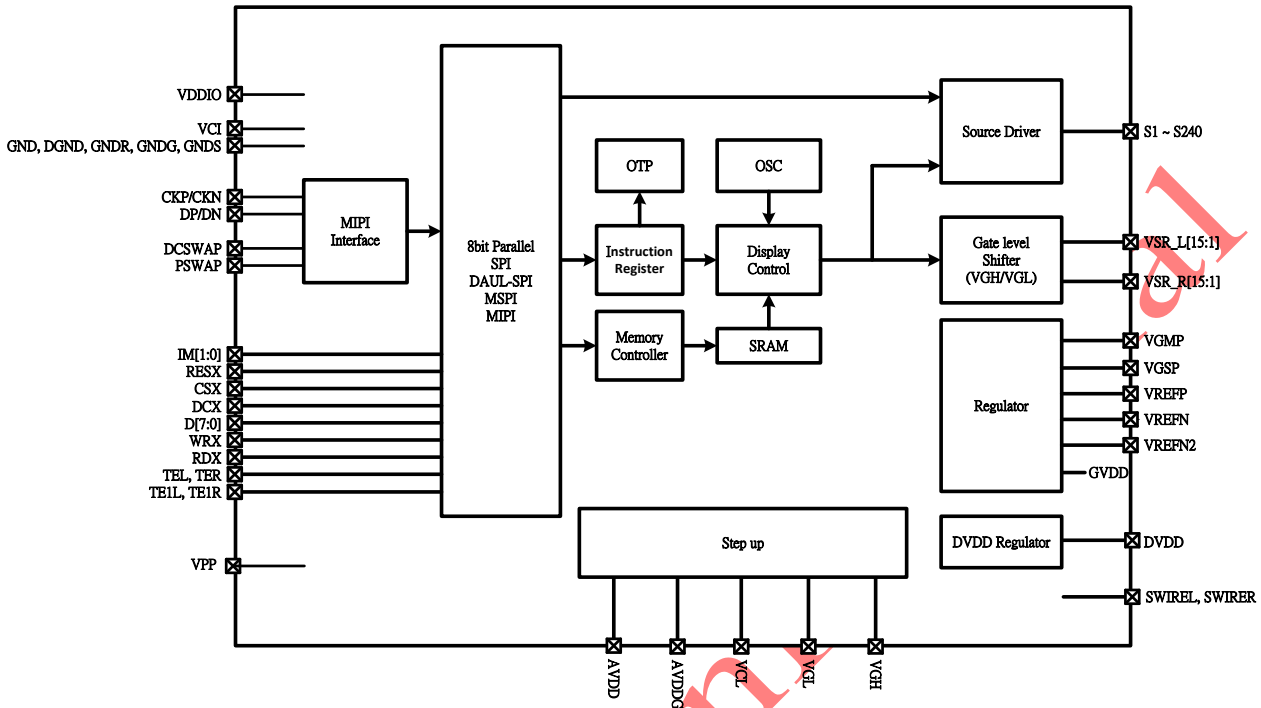
PAD No.	Pad Name	X	Y
295	DMY	189	304.92
296	DMY	126	304.92
297	DMY	63	304.92
298	DMY	0	304.92
299	DMY	-63	304.92
300	VCI	-126	304.92
301	VREFN	-189	304.92
302	GNDS	-252	304.92
303	VREFP	-315	304.92
304	VREFN2	-378	304.92
305	DMY	-441	304.92
306	DMY	-504	304.92
307	DMY	-567	304.92
308	DMY	-630	304.92
309	DMY	-693	304.92
310	DMY	-756	304.92
311	DMY	-819	304.92
312	DMY	-882	304.92
313	DMY	-945	304.92
314	DMY	-1008	304.92
315	DMY	-1071	304.92
316	DMY	-1134	304.92
317	DMY	-1197	304.92
318	DMY	-1260	304.92
319	S121	-1341.9	229.32
320	S122	-1364.4	304.92
321	S123	-1386.9	229.32
322	S124	-1409.4	304.92
323	S125	-1431.9	229.32
324	S126	-1454.4	304.92
325	S127	-1476.9	229.32
326	S128	-1499.4	304.92
327	S129	-1521.9	229.32
328	S130	-1544.4	304.92
329	S131	-1566.9	229.32
330	S132	-1589.4	304.92
331	S133	-1611.9	229.32
332	S134	-1634.4	304.92
333	S135	-1656.9	229.32
334	S136	-1679.4	304.92
335	S137	-1701.9	229.32
336	S138	-1724.4	304.92
337	S139	-1746.9	229.32
338	S140	-1769.4	304.92
339	S141	-1791.9	229.32
340	S142	-1814.4	304.92
341	S143	-1836.9	229.32
342	S144	-1859.4	304.92
343	S145	-1881.9	229.32
344	S146	-1904.4	304.92
345	S147	-1926.9	229.32
346	S148	-1949.4	304.92
347	S149	-1971.9	229.32
348	S150	-1994.4	304.92
349	VCI	-2060.55	229.32
350	GNDS	-2083.05	304.92
351	S151	-2135.7	229.32
352	S152	-2158.2	304.92
353	S153	-2180.7	229.32
354	S154	-2203.2	304.92
355	S155	-2225.7	229.32
356	S156	-2248.2	304.92
357	S157	-2270.7	229.32
358	S158	-2293.2	304.92
359	S159	-2315.7	229.32
360	S160	-2338.2	304.92
361	S161	-2360.7	229.32
362	S162	-2383.2	304.92
363	S163	-2405.7	229.32
364	S164	-2428.2	304.92
365	S165	-2450.7	229.32
366	S166	-2473.2	304.92
367	S167	-2495.7	229.32
368	S168	-2518.2	304.92
369	S169	-2540.7	229.32
370	S170	-2563.2	304.92
371	S171	-2585.7	229.32
372	S172	-2608.2	304.92
373	S173	-2630.7	229.32
374	S174	-2653.2	304.92
375	S175	-2675.7	229.32
376	S176	-2698.2	304.92
377	S177	-2720.7	229.32
378	S178	-2743.2	304.92
379	S179	-2765.7	229.32
380	S180	-2788.2	304.92
381	S181	-2844.9	229.32
382	S182	-2867.4	304.92
383	S183	-2889.9	229.32
384	S184	-2912.4	304.92
385	S185	-2934.9	229.32
386	S186	-2957.4	304.92
387	S187	-2979.9	229.32
388	S188	-3002.4	304.92
389	S189	-3024.9	229.32
390	S190	-3047.4	304.92
391	S191	-3069.9	229.32
392	S192	-3092.4	304.92
393	S193	-3114.9	229.32

PAD No.	Pad Name	X	Y
394	S194	-3137.4	304.9
395	S195	-3159.9	229.3
396	S196	-3182.4	304.9
397	S197	-3204.9	229.3
398	S198	-3227.4	304.9
399	S199	-3249.9	229.3
400	S200	-3272.4	304.9
401	S201	-3294.9	229.3
402	S202	-3317.4	304.9
403	S203	-3339.9	229.3
404	S204	-3362.4	304.9
405	S205	-3384.9	229.3
406	S206	-3407.4	304.9
407	S207	-3429.9	229.3
408	S208	-3452.4	304.9
409	S209	-3474.9	229.3
410	S210	-3497.4	304.9
411	VCI	-3556.8	229.3
412	GNDS	-3579.3	304.9
413	S211	-3638.7	229.3
414	S212	-3661.2	304.9
415	S213	-3683.7	229.3
416	S214	-3706.2	304.9
417	S215	-3728.7	229.3
418	S216	-3751.2	304.9
419	S217	-3773.7	229.3
420	S218	-3796.2	304.9
421	S219	-3818.7	229.3
422	S220	-3841.2	304.9
423	S221	-3863.7	229.3
424	S222	-3886.2	304.9
425	S223	-3908.7	229.3
426	S224	-3931.2	304.9

PAD No.	Pad Name	X	Y
427	S225	-3953.7	229
428	S226	-3976.2	305
429	S227	-3998.7	229
430	S228	-4021.2	305
431	S229	-4043.7	229
432	S230	-4066.2	305
433	S231	-4088.7	229
434	S232	-4111.2	305
435	S233	-4133.7	229
436	S234	-4156.2	305
437	S235	-4178.7	229
438	S236	-4201.2	305
439	S237	-4223.7	229
440	S238	-4246.2	305
441	S239	-4268.7	229
442	S240	-4291.2	305
443	SL	-4313.7	229
444	GNDS	-4336.2	305
445	VCI	-4358.7	229
446	VGL	-4381.2	305
447	VGH	-4403.7	229
448	VGL	-4426.2	305
449	VSR_L[1]	-4477.05	298
450	VSR_L[2]	-4549.05	298
451	VSR_L[3]	-4621.05	298
452	VSR_L[4]	-4693.05	298
453	VSR_L[5]	-4765.05	298
454	VSR_L[6]	-4837.05	298
455	VSR_L[7]	-4909.05	298
456	VSR_L[8]	-4981.05	298
457	VSR_L[9]	-5053.05	298
458	VSR_L[10]	-5125.05	298
459	VSR_L[11]	-5197.05	298

PAD No.	Pad Name	X	Y
460	VSR_L[12]	-5269.05	297.72
461	VSR_L[13]	-5341.05	297.72
462	VSR_L[14]	-5413.05	297.72
463	VSR_L[15]	-5485.05	297.72
464	GNDS	-5540.4	297.72
465	GNDS	-5585.4	297.72
466	GNDG	-5630.4	297.72
467	VREFN2	-5675.4	297.72
468	VREFN	-5720.4	297.72
469	VREFP	-5765.4	297.72
470	VGL	-5810.4	297.72
471	VGH	-5855.4	297.72
472	VGL	-5900.4	297.72
473	ATSTNL	-5945.4	297.72
474	ATSTPL	-5990.4	297.72

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDDIO	I	Power supply for I/O system.	VDDIO
VCI	I	Power supply for internal circuit.	VCI
GND	I	System ground for internal circuit.	GND
GNDR	I	System ground for internal circuit.	GND
GNDG	I	System ground for internal circuit.	GND
GNDS	I	System ground for internal circuit.	GND
DGND	I	System ground for internal circuit.	GND

6.2 Bus Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td colspan="4">Digital Control</td></tr>
<tr><td>RESXR
RESXL</td><td>I</td><td>The external reset input signal.
RESXR and RESXL are short-circuited within the chip.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td><td>MPU</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>The system interface select
<table>
<tr><th>IM1</th><th>IM0</th><th>Display Data or Commnad</th></tr>
<tr><td>0</td><td>0</td><td>MIPI + 3-wire SPI</td></tr>
<tr><td>0</td><td>1</td><td>MIPI + 4-wire SPI</td></tr>
<tr><td>1</td><td>0</td><td>MIPI + MSPI</td></tr>
<tr><td>1</td><td>1</td><td>MIPI + 8-bit parallel interface</td></tr>
</table>
If only use MIPI interface, leave IM0 and IM1 open and CSX as VDDIO.</td><td>VDDIO/
GND</td></tr>
<tr><td colspan="4">SPI and 8-bit Parallel Interface</td></tr>
<tr><td>CSX</td><td>I</td><td>A chip select signal for SPI and 8-bit parallel interface.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to VDDIO level when not in use.</td><td>MPU</td></tr>
<tr><td>DCX</td><td>I</td><td>Command or parameter select signal for 4SPI and 8-bit parallel interface.
Low: Command
High: Parameter
Leave the pin open when not in use.</td><td>MPU</td></tr>
<tr><td>WRX</td><td>I</td><td>Serial clock (SCL) input for SPI interface.
Write clock (WRX) input for 8-bit parallel interface.
Leave the pin open when not in use.</td><td>MPU</td></tr>
<tr><td>RDX</td><td>I/O</td><td>Serial data input (SDA) and output (SDO) pin for SPI Interface
Read clock (RDX) input for 8-bit parallel interface.
Leave the pin open when not in use.</td><td>MPU</td></tr>
<tr><td>D7 ~ D0</td><td>I/O</td><td>8-bit parallel interface data bus
Leave the pin open when not in use.</td><td>MPU</td></tr>
<tr><td colspan="4">Power Control</td></tr>
<tr><td>SWIREL,
SWIRER</td><td>O</td><td>Power IC single wire control pin.
SWIREL and SWIRER are short-circuited within the chip.
Leave the pin open when not in use.</td><td>PMU</td></tr>
<tr><td colspan="4">MIPI Interface</td></tr>
<tr><td>DP</td><td>I/O</td><td>MIPI DSI differential data pair.</td><td>MIPI</td></tr>
</table>

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>DN</td><td></td><td>Leave the pin open when not in use.</td><td></td></tr>
<tr><td>CKP
CKN</td><td>I</td><td>MIPI DSI differential clock pair.
Leave the pin open when not in use.</td><td>MIPI</td></tr>
<tr><td>DCSWAP
PSWAP</td><td>I</td><td>MIPI clock and data lane sequence select pins
<table>
<tr><th>DCSWAP</th><th>PSWAP</th><th>DP</th><th>DN</th><th>CKP</th><th>CKN</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>D0_P</td><td>D0_N</td><td>CLK_P</td><td>CLK_N</td></tr>
<tr><td>1</td><td>D0_N</td><td>D0_P</td><td>CLK_N</td><td>CLK_P</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>CLK_P</td><td>CLK_N</td><td>D0_P</td><td>D0_N</td></tr>
<tr><td>1</td><td>CLK_N</td><td>CLK_P</td><td>D0_N</td><td>D0_P</td></tr>
</table>
If only use SPI or P80 interface, leave DCSWAP and PSWAP open.</td><td>VDDIO/
GND</td></tr>
</table>

6.3 Driver Output Pins

Name	I/O	Description	Connect pin
VGH	O	Positive gate driver output.	AMOLED
VGL	O	Negative gate driver output.	AMOLED
VREFP	O	Positive bias voltage for AMOLED panel	AMOLED
VREFN	O	Negative bias voltage for AMOLED panel	AMOLED
VREFN2	O	Negative bias voltage for AMOLED panel	AMOLED
VSR_L [1:15]	O	Gate control signals and the swing voltage level is VGH to VGL.	AMOLED
VSR_R [1:15]	O	Gate control signals and the swing voltage level is VGH to VGL.	AMOLED
S1 ~ S240	O	Source output for the panel.	AMOLED
ATSTPL, ATSTPR	O	Positive LDO output pin	OPEN
ATSTNL, ATSTNR	O	Negative LDO output pin	OPEN

6.4 Test and other pins

Name	I/O	Description	Connect pin
VCL	O	Power pin for negative step-up voltage.	OPEN
AVDD	O	Power pin for positive step-up voltage.	OPEN
AVDDG	O	Power pin for positive step-up voltage.	OPEN
VAG	O	Test pin for internal power.	OPEN
V20	O	Test pin for internal power.	OPEN
DVDD	O	Power pin for digital circuit.	OPEN
VGMP	O	A power output for gamma high voltage.	OPEN
VGSP	O	A power output for gamma low voltage.	OPEN
TEL, TER	O	Synchronize signal pin to another device. TEL and TER are short-circuited within the chip. ***Leave the pin open when not in use.***	MPU
TE1L, TE1R	O	Synchronize signal pin to another device. TE1L and TE1R are short-circuited within the chip. ***Leave the pin open when not in use.***	MPU
EXTCLK	I	Digital test clock input pin.	OPEN
TESTEN	I	Test control pin.	OPEN
TEST1	I	Test control pin.	OPEN
TESTIN4 ~ TESTIN1	I	Digital test input pin. ***Leave the pin open when not in use.***	OPEN
VPP	I	Test pin for OTP. ***Leave the pin open when not in use.***	OPEN

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VCI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDIO	- 0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDIO + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ VDDIO + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristics for panel driving

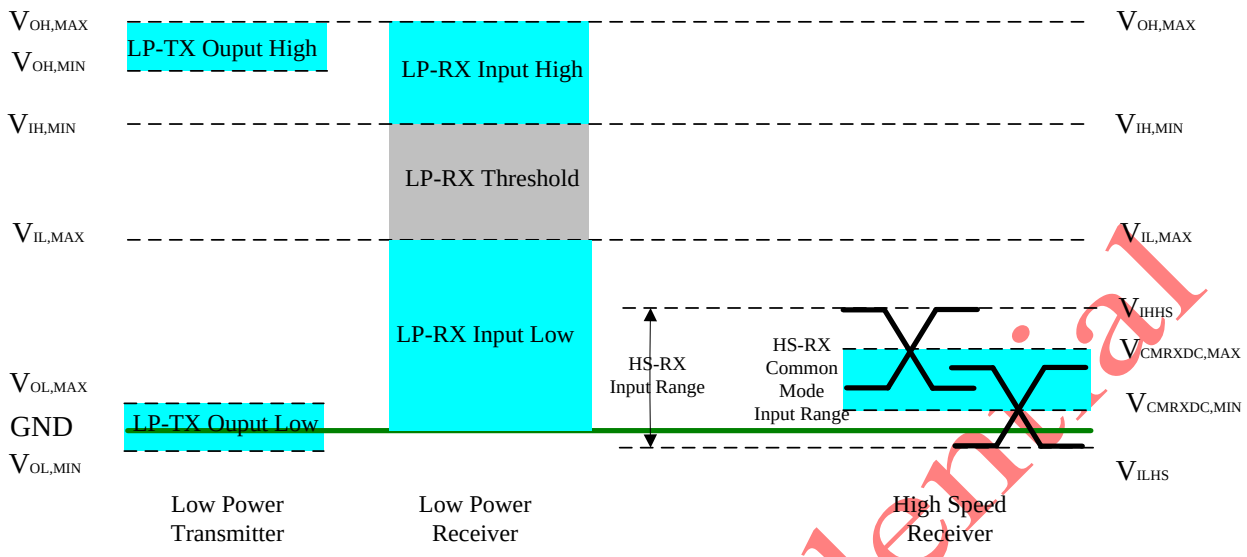
Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VCI	Operating voltage	2.7	3.3	3.6	V	
Interface Operation Voltage	VDDIO	I/O Supply Voltage	1.65	1.8	3.6	V	
Gate Driver High Voltage	VGH		3.6	6	10	V	
Gate Driver Low Voltage	VGL		-10	-6	-3.6	V	
Gate Driver Supply Voltage		| VGH-VGL |			20	V	
Driver Supply Voltage	AVDD		4.0	5.6	6.6	V	
Driver Supply Current	IAVDD			1.5		mA	
Positive Reference Voltage	VREFP		0.5		5.0	V	
Negative Reference Voltage	VREFN		-4.5		-0.5	V	
Negative Reference Voltage	VREFN2		-4.5		-0.5	V	
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDIO		VDDIO	V	Note 1
Logic-Low Input Voltage	VIL		DGND		0.3VDDIO	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDIO		VDDIO	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	DGND		0.2VDDIO	V	Note 1
Differential Input High Threshold Voltage	VIT+			0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-		-50	0		mV	
Single-ended Receiver Input Operation Voltage Range	VIR		0.5		1.2	V	
Logic-High Input Current	IIH	VIN = VDDIO			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = DGND	-1			uA	Note 1
Input Leakage Current	ILO	IOH = -1.0mA	-0.1		0.1	uA	Note 1
Source Driver							
Gamma Reference Voltage(High)	VGMP		2.0		6.3	V	
Gamma Reference Voltage(Low)	VGSP		0.15		4.5	V	
Source Voltage Deviation	V_{DEV}			5		mV	
Oscillator							

OSC Frequency	F_{OSC}		42.32	46	49.68	MHz	

Table 2 Basic DC Characteristics

Notes:
1. Typical: VDDIO=1.8V, VCI=3.3V; Ta=25 ℃

7.3 DC Characteristics for MIPI



VDDIO=1.8V, VCI=3.3V, GND=0V, Ta=25 ℃

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.4 Power Consumption

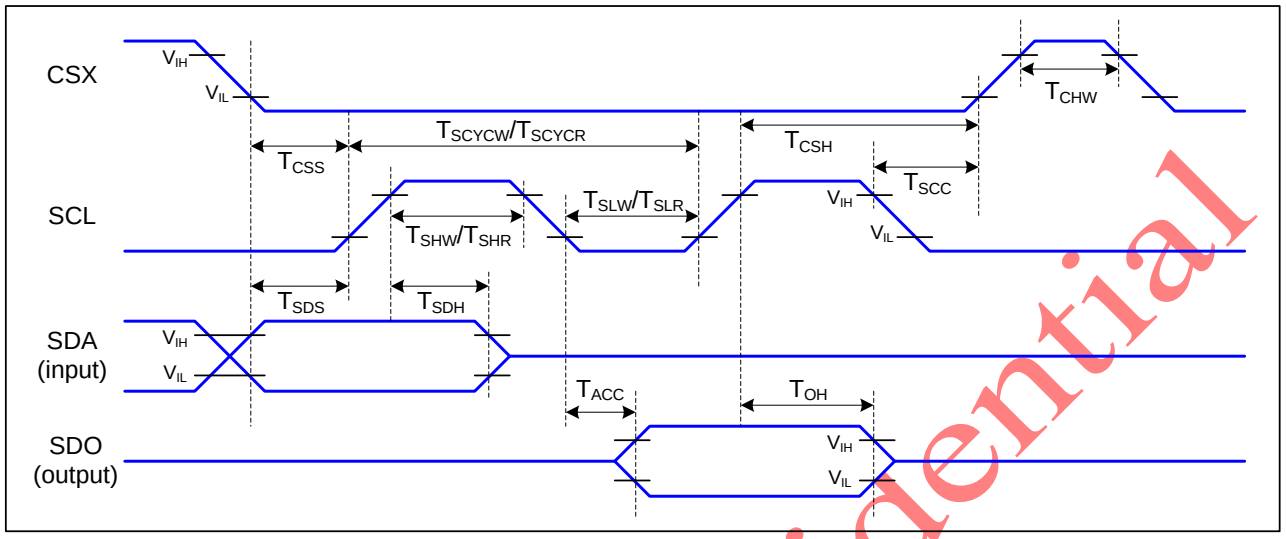
VDDIO=1.8V, VCI=3.3V, GND=0V, Ta=25 ℃

Parameter	Symbol	Condition	Max.	Unit
Sleep in Mode	I_{SLP_VDDIO}	VDDIO = 1.8V VCI = 3.3V D0P/N = CLKP/N = LP11	TBD	uA
	I_{SLP_VCI}		TBD	uA
Deep Standby Mode	I_{DSTB_VDDIO}	VDDIO = 1.8V VCI = 3.3V D0P/N = CLKP/N = LP11	TBD	uA
	I_{DSTB_VCI}		TBD	uA

7.5 AC Characteristics

7.5.1 3-wire SPI Serial Data Transfer Interface Characteristics:

3-SPI Interface Timing Characteristics

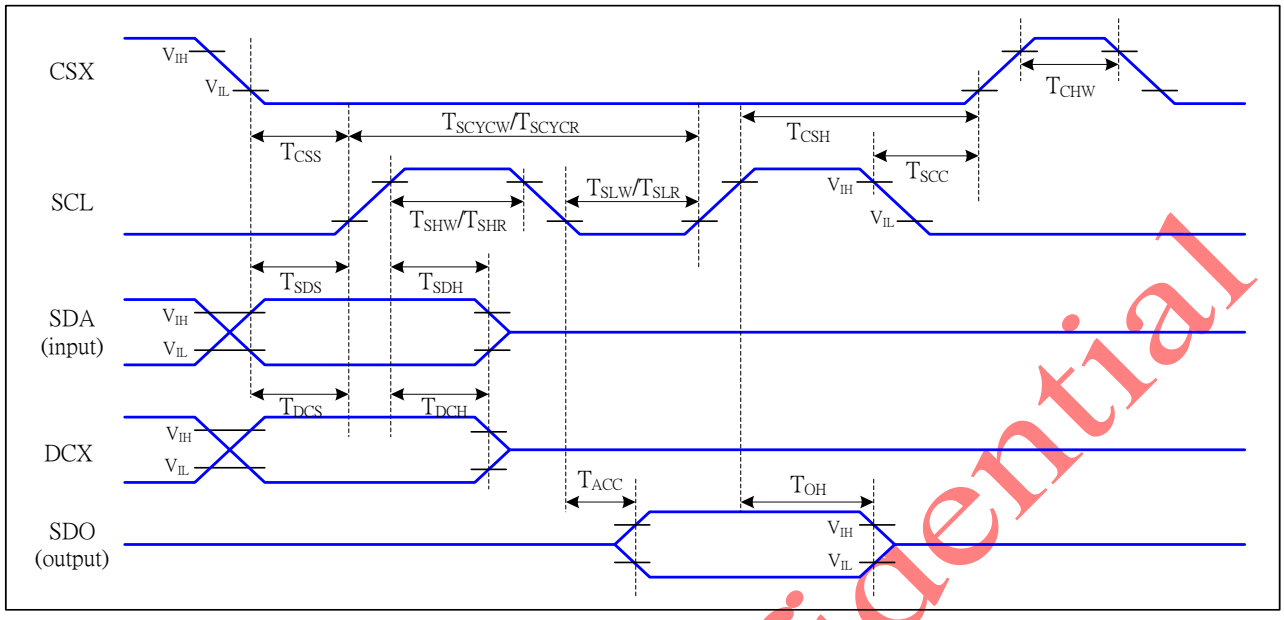


VDDIO=1.8V,VCI=3.3V, GND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	10		ns	
	T_{CSH}	Chip select hold time (write)	10		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	300		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	140		ns	
	T_{SLR}	SCL “L” pulse width (Read)	140		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	120	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	10		ns	

7.5.2 4-wire SPI Serial Data Transfer Interface Characteristics:

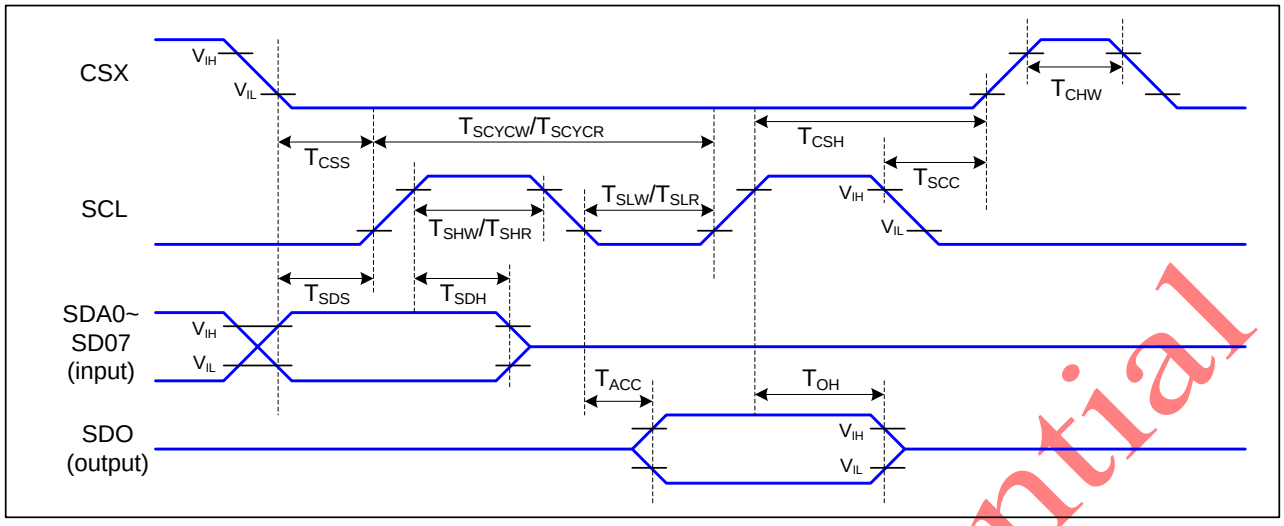
4-wire SPI Interface Timing Characteristics



VDDIO=1.8V,VCI=3.3V, GND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	300		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	140		ns	
	T_{SLR}	SCL “L” pulse width (Read)	140		ns	
DCX	T_{DCS}	DCX setup time	7		ns	
	T_{DCH}	DCX hold time	7		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	120	ns	For maximum CL=30pF
	T_{OH}	Output hold time	10		ns	For minimum CL=8pF

7.5.3 MSPI Interface Characteristics:

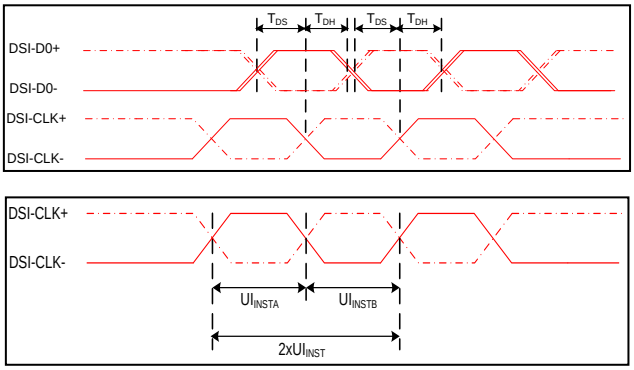


VDDIO=1.8V,VCI=3.3V, GND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	20		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	9		ns	
	T_{SLW}	SCL “L” pulse width (Write)	9		ns	
	T_{SCYCR}	Serial clock cycle (Read)	300		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	140		ns	
	T_{SLR}	SCL “L” pulse width (Read)	140		ns	
SDA (DIN)	T_{SDS}	Data setup time	9		ns	
	T_{SDH}	Data hold time	9		ns	
DOUT	T_{ACC}	Access time	10	120	ns	For maximum CL=30pF
	T_{OH}	Output hold time	10		ns	For minimum CL=8pF

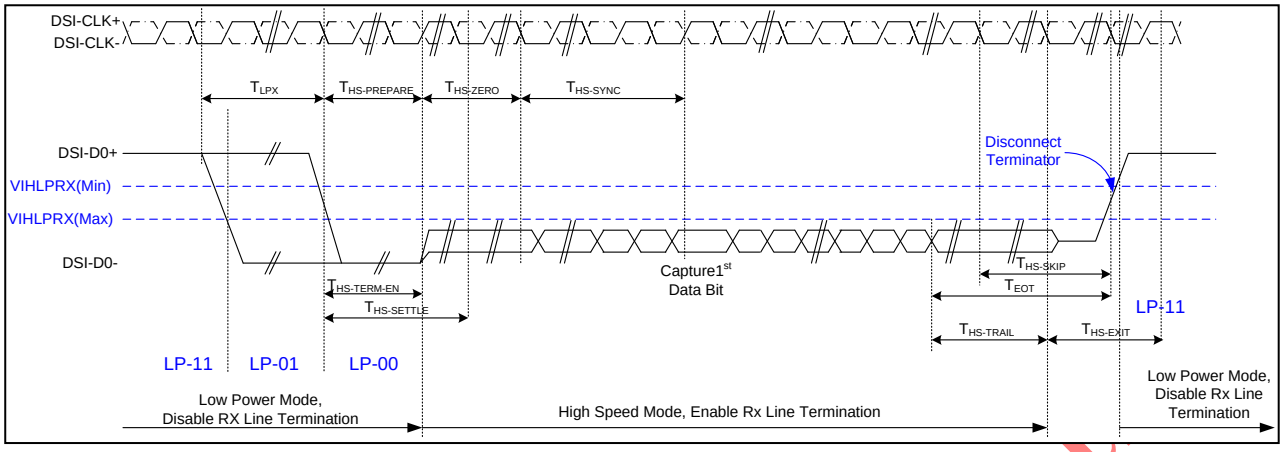
7.5.4 MIPI DSI Timing Characteristics:

High Speed Mode – Clock Channel Timing



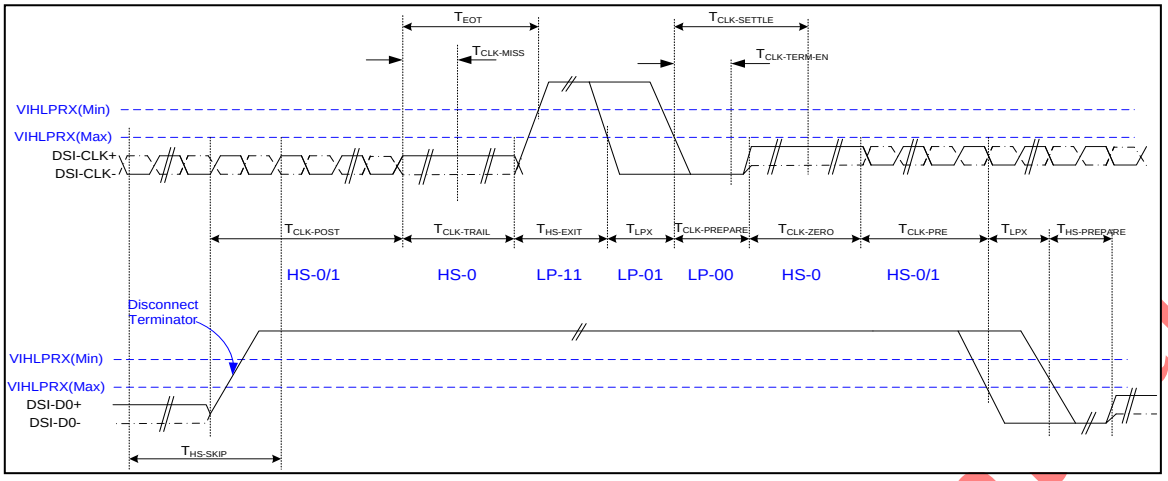
Signal	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
CKP/N	UI_{INSTA} ,UI_{INSTB}	UI instantaneous	1.82	-	12.5	ns	
fCKP/N	F_{DSICLK}	DSI-CLK+/- frequency	40	-	275	MHz	
DP/N	T_{DS}	Data to clock setup time	0.2	-	-	UI	
DP/N	T_{DH}	Data to clock hold time	0.2	-	-	UI	

High-Speed Data Transmission



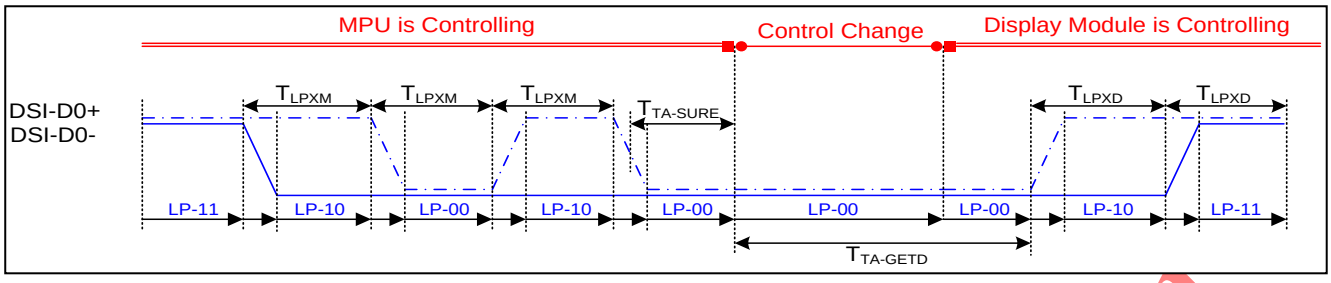
Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns
Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPAR}$	$T_{CLK-SETTLE}$	95	-	300	ns
Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPAR}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	$T_{HS-SETTLE}$	85+6UI	-	145+10UI	ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}+T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

Bus Turn-around Procedure



Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	-
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}	-	2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	5 T_{LPX}	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	4 T_{LPX}	-	ns

7.5.5 Reset Timing

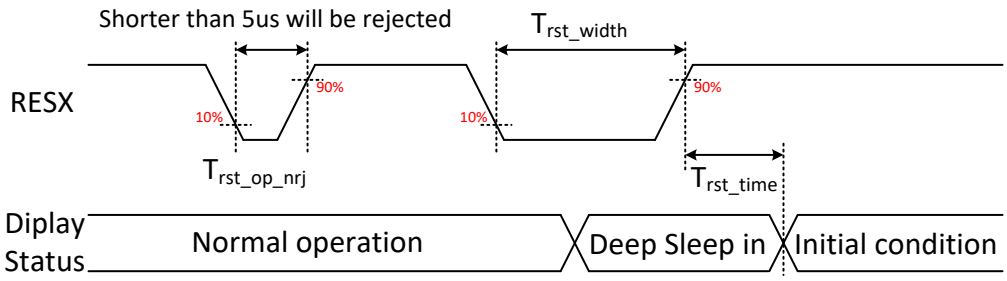


Figure 1 Reset Operation

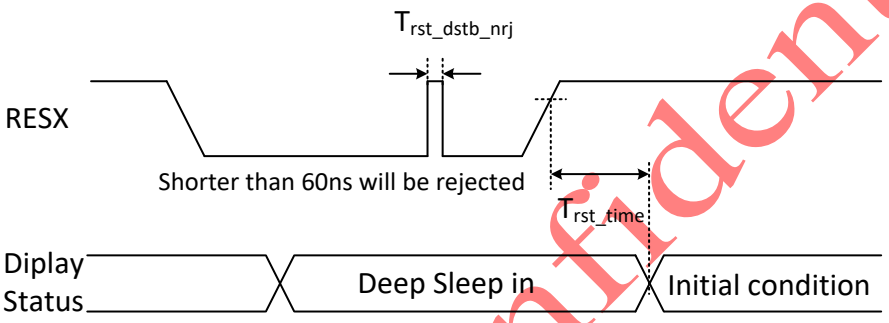


Figure 2 Reset Noise Rejected Diagram

Reset Timing Characteristics VDDIO=1.65~1.95V Ta=25℃

Parameter	Symbol	Specification			Unit
		Min.	Typ.	Max.	
Reset low width	Trst_width	1	-	-	ms
Reset time	Trst_time	2	-	-	ms
OP noise reject	Trst_op_nrj	-	-	5	us
DSLPI Noise reject	Trst_dslpi_nrj	-	-	60	ns

- During the reset period, the display will be blanked, then return to default condition for IC initialization

- It is necessary to wait 2ms after releasing HWRST pin before sending commands.

8 FUNCTION DESCRIPTION

8.1 System Interface

ST7802 supports 8-bit parallel Interface, SPI, Dual-SPI, Multi-SPI, and MIPI serial interfaces. Selection of these interfaces are set by IM[1:0] pins and DSPI_EN bit as shown below.

IM1	IM0	DSPI_EN	Interface	Data pins
0	0	0	MIPI + 3-wire SPI	D0P/N, RDX,
0	0	1	MIPI + Dual-SPI	D0P/N, RDX, DCX
0	1	0	MIPI + 4-wire SPI	D0P/N, RDX, DCX
0	1	1	MIPI + Dual-SPI	D0P/N, RDX, DCX
1	0	-	MIPI + Multi-SPI	D0P/N, RDX, DCX, D0 ~ D5
1	1	-	MIPI + 8-bit parallel interface	D0P/N, D0 ~ D7

8.2 SPI Interface

The Serial Peripheral Interface (SPI) is either 3-wire or 4-wire bi-directional interface for communication between the micro controller and the AMOLED driver. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.2.1 3-wire SPI

The 3-wire SPI is selected by setting the IM[1:0] pins as “00” level and register DSPI_EN bit as “0”. The following are the pin names and descriptions.

Pin Name	Description
CSX	Chip selection signal
WRX	Serial input CLK (SCL)
RDX	Serial input data and output data (SDA)

8.2.1.1 Write Mode

The write mode of the interface means the micro controller writes commands and data to the AMOLED driver. In the write mode of 3-wire serial interface contains a D/CX (data/command) select bit and a transmission byte. If the D/C bit is “0”, the transmission byte is interpreted as a command byte. If the D/C bit is “1”, the transmission byte is display data, or stored in the command register as parameter data.

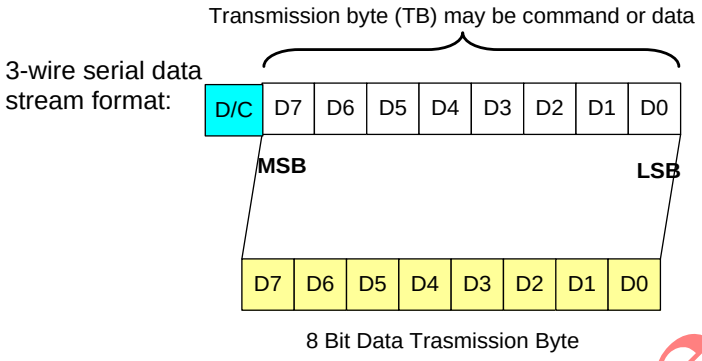


Figure 3 3-wire serial data stream format

The instruction of ST7802 can be sent in any order, and the MSB is transmitted first. The 3-wire serial interface is initialized when the CSX keeps high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

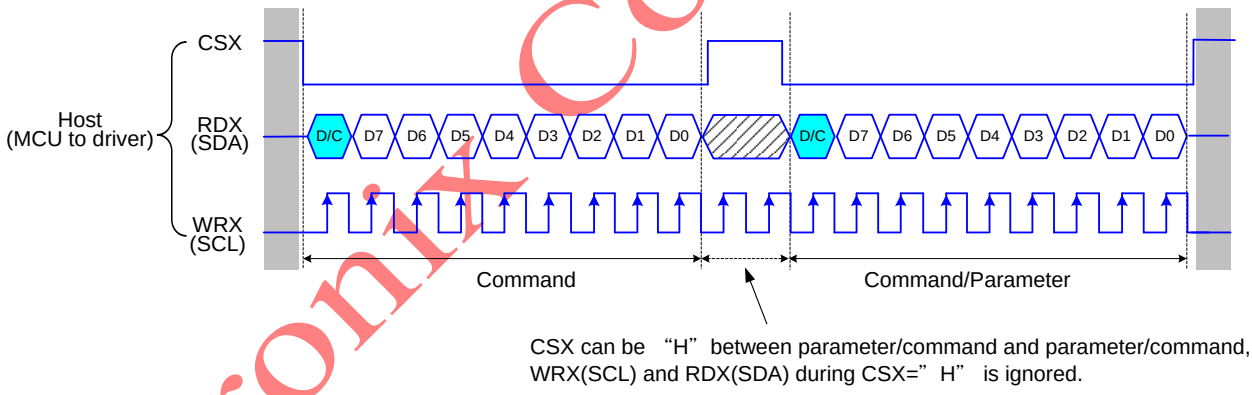
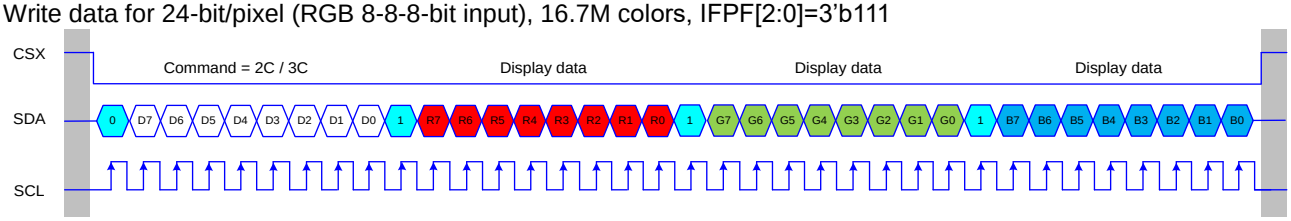


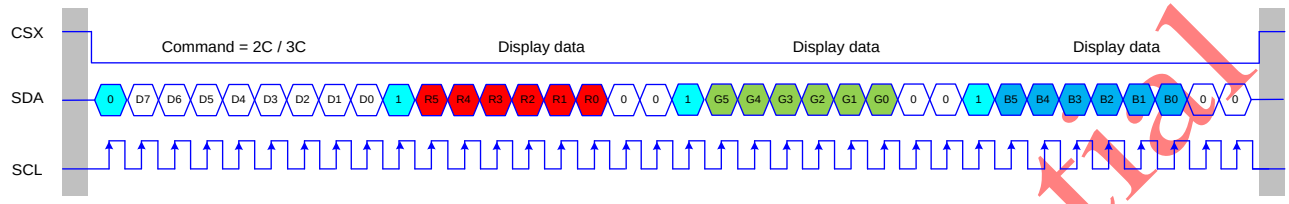
Figure 4 3-wire serial interface write protocol

8.2.1.2 3-wire SPI color format

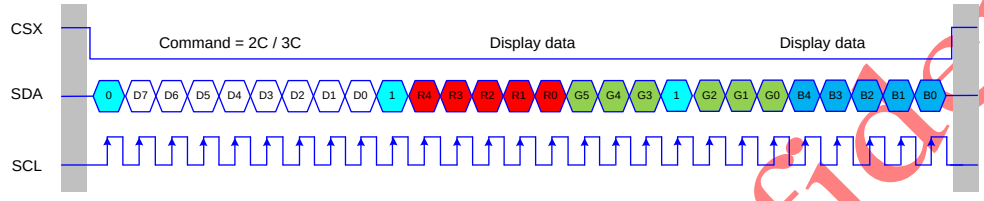
Write data for 24-bit/pixel (RGB 8-8-8-bit input), 16.7M colors, IFPF[2:0]=3'b111



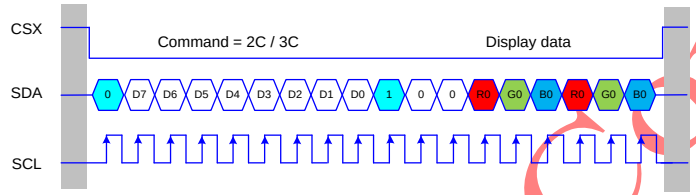
Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K colors, IFPF[2:0]=3'b110



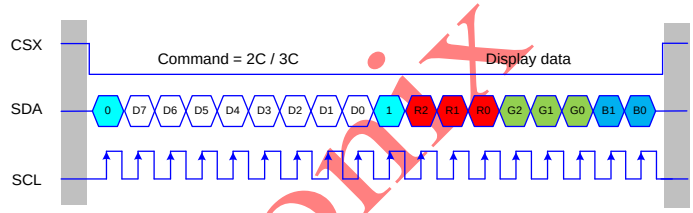
Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K colors, IFPF[2:0]=3'b101



Write data for 3-bit/pixel (RGB 1-1-1-bit input), 8 colors, IFPF[2:0]=3'b011



Write data for 8-bit/pixel (RGB 3-3-2-bit input), 256 colors, IFPF[2:0]=3'b010



Write data for 8-bit/pixel, gray 256 colors, IFPF[2:0]=3'b001

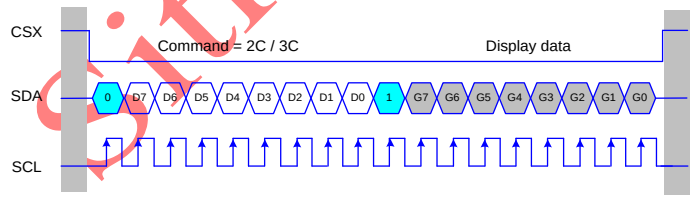


Figure 5 3-wire SPI color format

8.2.1.3 Read Mode

In the read mode of the interface, the host reads the register value from the ST7802. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The

ST7802 samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock).

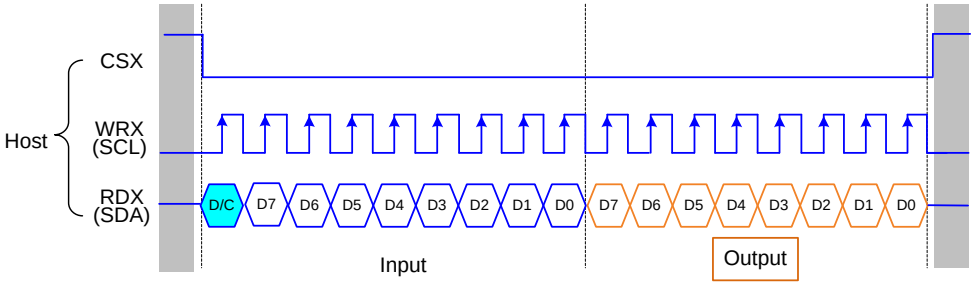


Figure 6 3-wire serial interface read protocol

8.2.2 4-wire SPI

The 4-wire SPI is selected by setting the IM[1:0] pins as “01” level and DSPI_EN bit as “0” level. The following are the pin names and descriptions.

Pin Name	Description
CSX	Chip selection signal
DCX	Data is regarded as a command when DCX is low Data is regarded as a parameter or data when DCX is high
WRX	Serial input CLK (SCL)
RDX	Serial input data and output data (SDA)

8.2.2.1 Write Mode

The write mode of the interface means the host writes commands and data to ST7802. The 4-wire serial data packet contains a data/command and a transmission byte. If DCX is “low”, the transmission byte is interpreted as a command byte. If DCX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

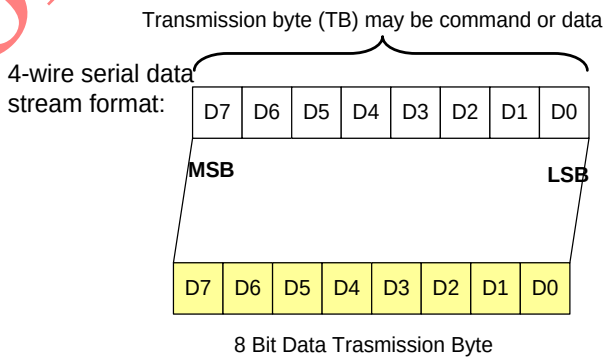


Figure 7 4-wire serial data stream format

The host drives the CSX pin to low and the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional DCX signal is used, a byte is eight read cycle long. The 4-wire serial interface writes sequence described in the Figure as below.

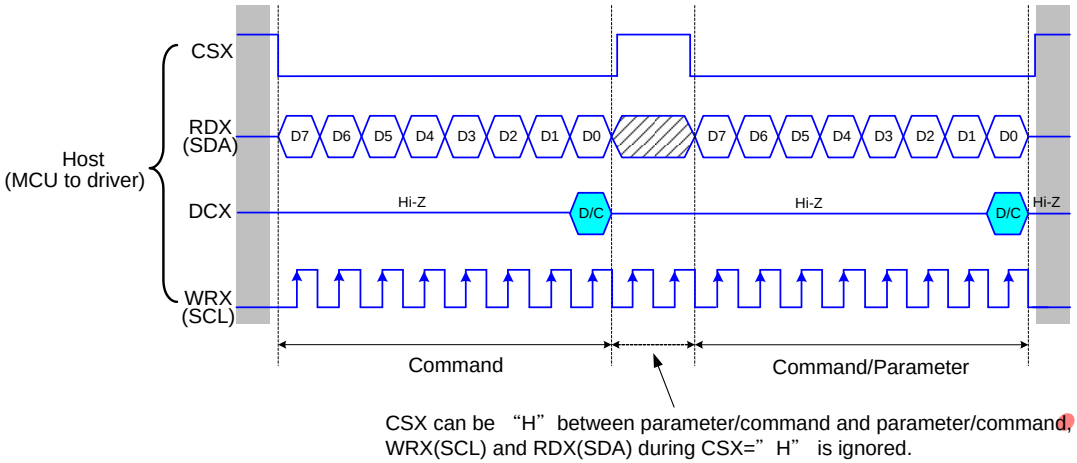
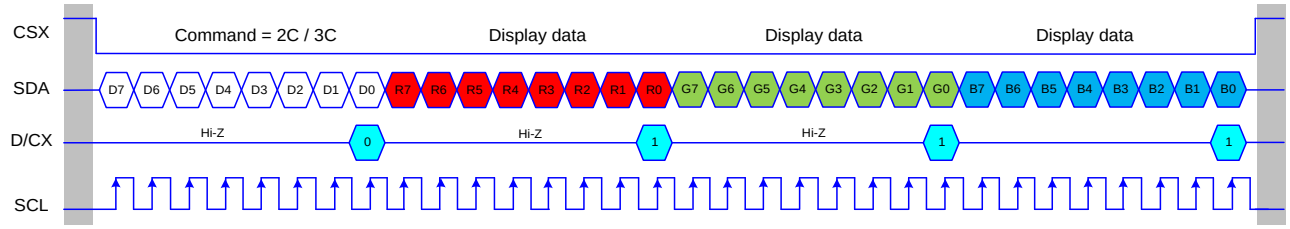


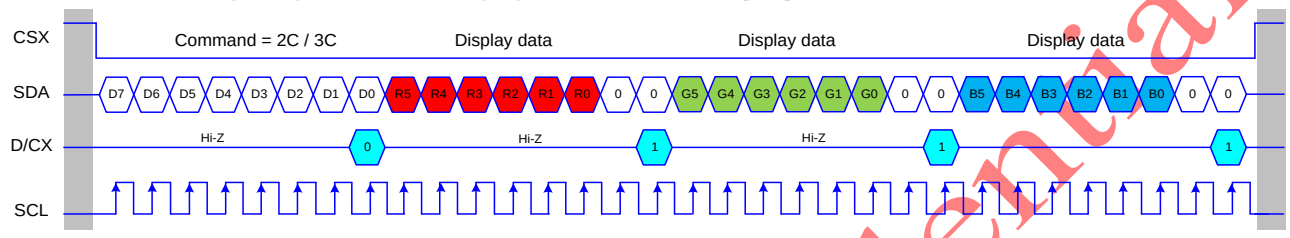
Figure 8 4-wire serial interface write protocol

8.2.2.1 4-wire SPI color format

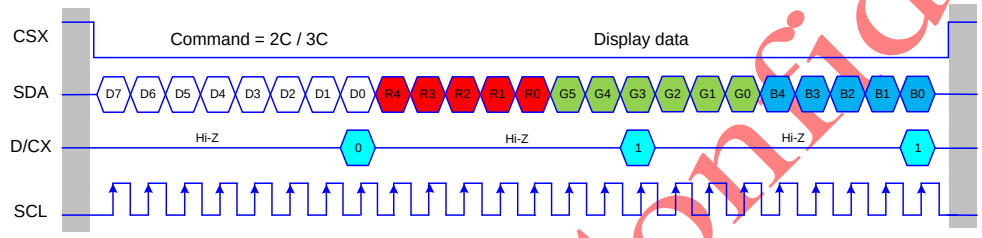
Write data for 24-bit/pixel (RGB 8-8-8-bit input), 16.7M colors, IFPF[2:0]=3'b111



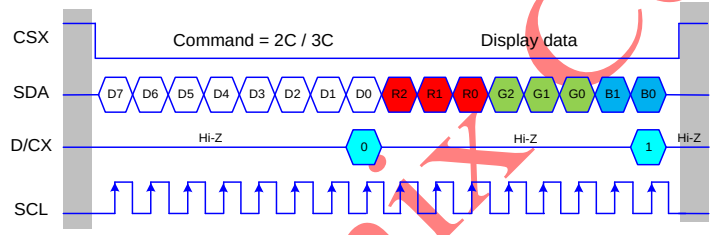
Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K colors, IFPF[2:0]=3'b110



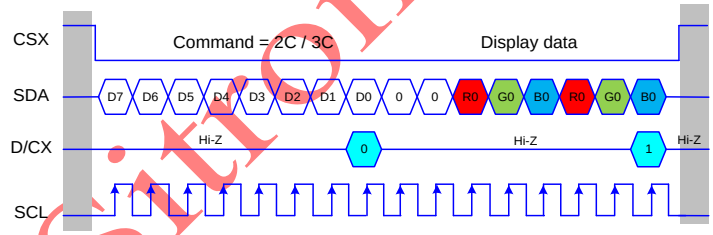
Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K colors, IFPF[2:0]=3'b101



Write data for 8-bit/pixel (RGB 3-3-2-bit input), 256 colors, IFPF[2:0]=3'b010



Write data for 3-bit/pixel (RGB 1-1-1-bit input), 8 colors, IFPF[2:0]=3'b011



Write data for 8-bit/pixel, gray 256 colors, IFPF[2:0]=3'b001

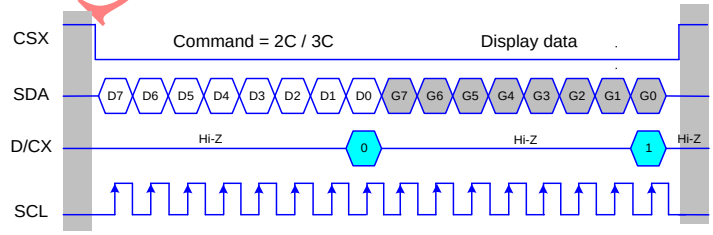


Figure 9 4-wire SPI color format

8.2.2.2 Read Mode

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

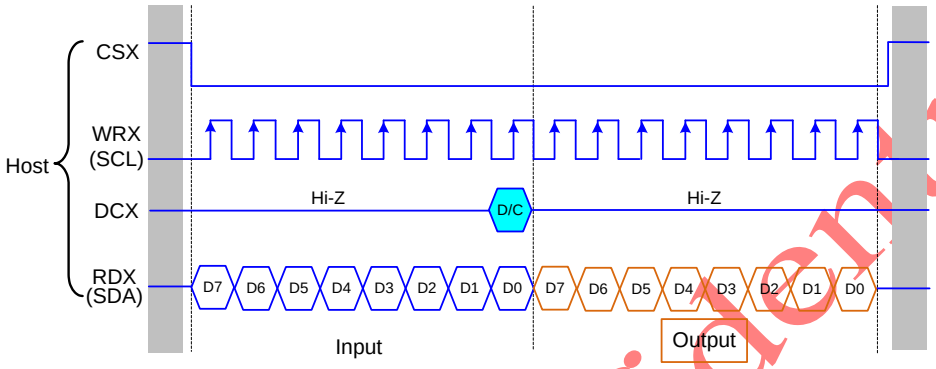


Figure 10 4-wire serial interface read protocol

8.3 Dual-SPI Interface

The Dual-SPI interface is selected by setting the IM[1:0] pins as “00” or “01” level and DSPI_EN bit as “1” level.

The following are the pin names and descriptions.

Pin Name	Description	
	IM[1:0]=2’b00	IM[1:0]=2’b01
CSX	Chip selection signal	Chip selection signal
DCX	Serial input for pixel data	Serial input for pixel data Control signal for command or parameter
WRX	Serial input CLK (SCL)	Serial input CLK (SCL)
RDX	Serial input data and output data (SDA)	Serial input data and output data (SDA)

8.3.1 Write command mode

When host writes commands or parameters to ST7802, DCX is not regarded as serial input data pin. The protocol would be the same as 3-wire SPI if IM[1:0]=2’b00 or 4-wire SPI if IM[1:0]=2’b01.

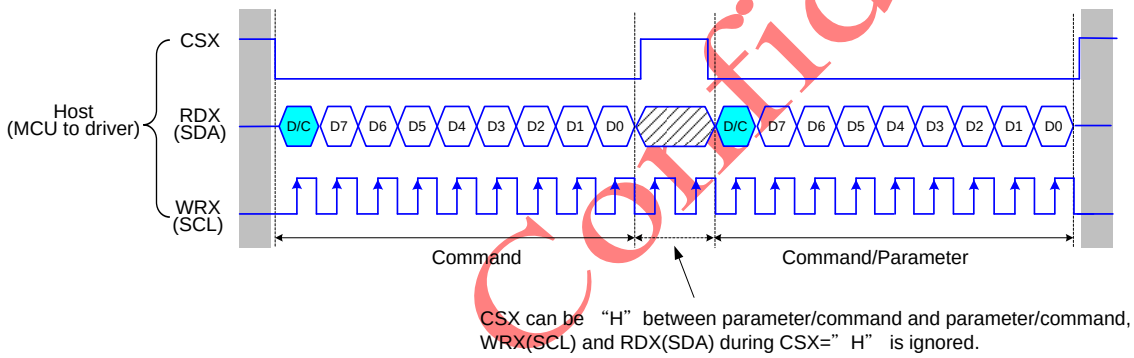


Figure 11 IM[1:0]=2’b00, 3-wire SPI write protocol

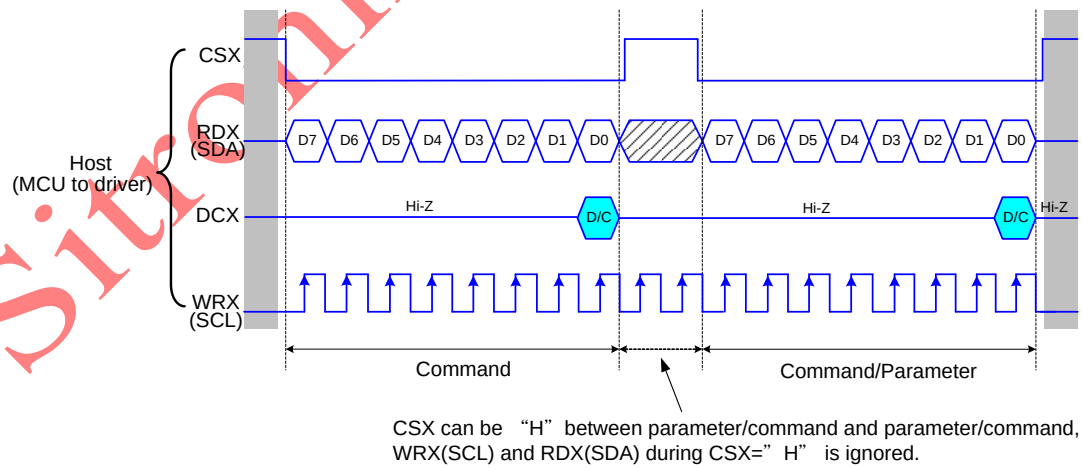


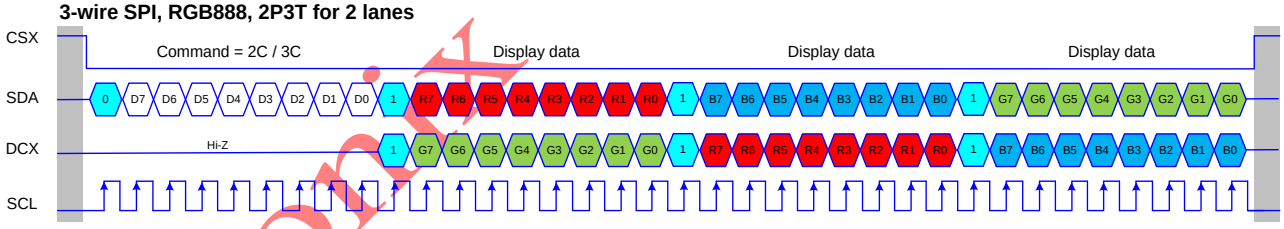
Figure 12 IM[1:0]=2’b01, 4-wire SPI write protocol

8.3.2 Write pixel data

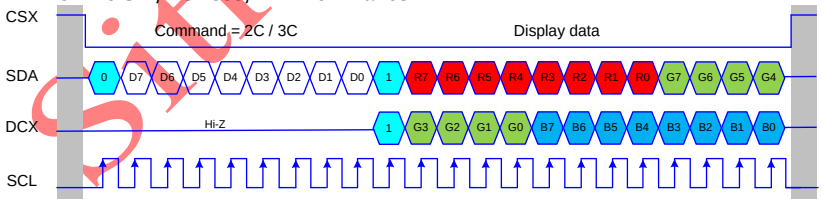
Compared to 3-wire or 4-wire SPI utilizes one RDX(SDA) as data lane, Dual-SPI both utilizes RDX(SDA) and DCX as data lanes. In this interface, the pixel data should be written according the following figure.

DSPI_EN	IM[1:0]	IFPF[2:0]	DSPI_CFG[1:0]	Data format
1	2'b00	3'b111	2'b11	3-wire SPI, RGB888, 2P3T for 2 lanes
1	2'b00	3'b111	2'b10	3-wire SPI, RGB888, 1P1T for 2 lanes
1	2'b00	3'b111	2'b00	3-wire SPI, RGB888, 1P1T for 1 lane
1	2'b00	3'b110	2'b11	3-wire SPI, RGB666, 2P3T for 2 lanes
1	2'b00	3'b110	2'b10	3-wire SPI, RGB666, 1P1T for 2 lanes
1	2'b00	3'b110	2'b00	3-wire SPI, RGB666, 1P1T for 1 lane
1	2'b00	3'b101	2'b10	3-wire SPI, RGB565, 1P1T for 2 lanes
1	2'b00	3'b101	2'b00	3-wire SPI, RGB565, 1P1T for 1 lane
1	2'b01	3'b111	2'b11	4-wire SPI, RGB888, 2P3T for 2 lanes
1	2'b01	3'b111	2'b10	4-wire SPI, RGB888, 1P1T for 2 lanes
1	2'b01	3'b111	2'b00	4-wire SPI, RGB888, 1P1T for 1 lane
1	2'b01	3'b110	2'b11	4-wire SPI, RGB666, 2P3T for 2 lanes
1	2'b01	3'b110	2'b10	4-wire SPI, RGB666, 1P1T for 2 lanes
1	2'b01	3'b110	2'b00	4-wire SPI, RGB666, 1P1T for 1 lane
1	2'b01	3'b101	2'b10	4-wire SPI, RGB565, 1P1T for 2 lanes
1	2'b01	3'b101	2'b00	4-wire SPI, RGB565, 1P1T for 1 lane

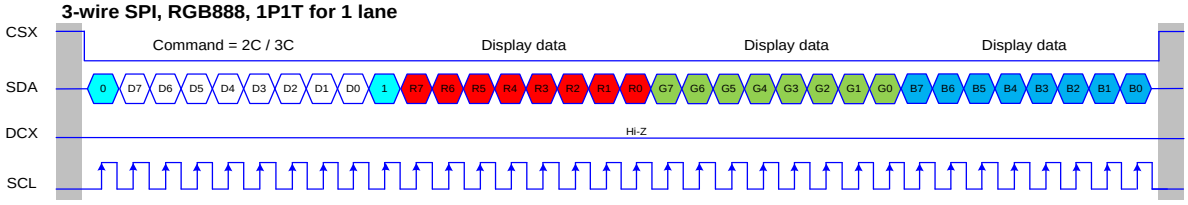
3-wire SPI, RGB888, 2P3T for 2 lanes



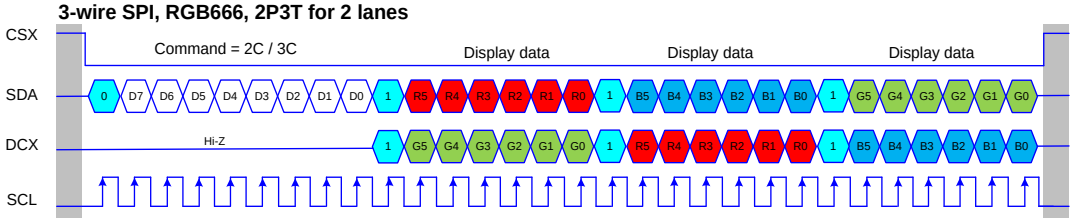
3-wire SPI, RGB888, 1P1T for 2 lanes



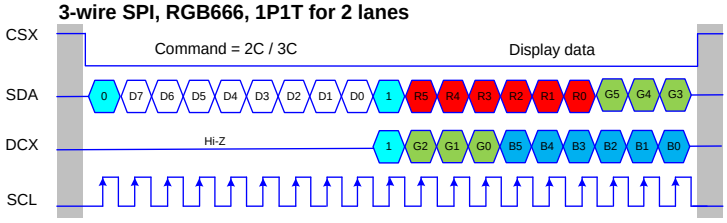
3-wire SPI, RGB888, 1P1T for 1 lane



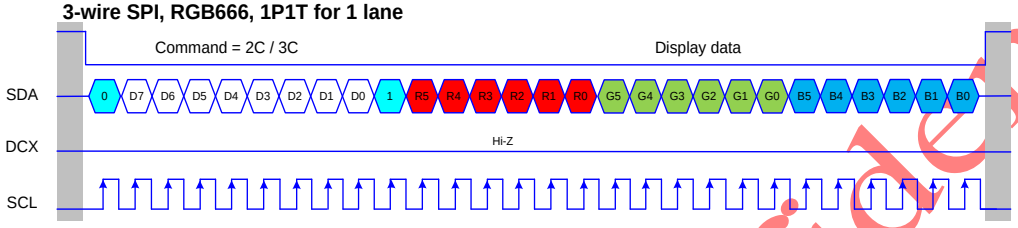
3-wire SPI, RGB666, 2P3T for 2 lanes



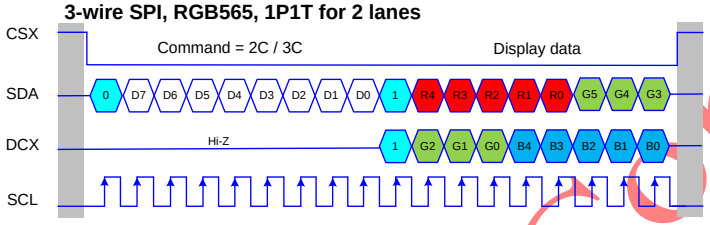
3-wire SPI, RGB666, 1P1T for 2 lanes



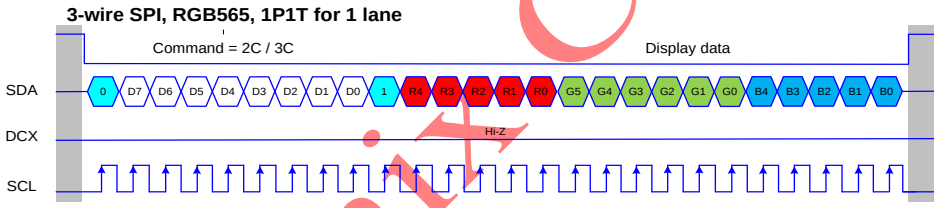
3-wire SPI, RGB666, 1P1T for 1 lane



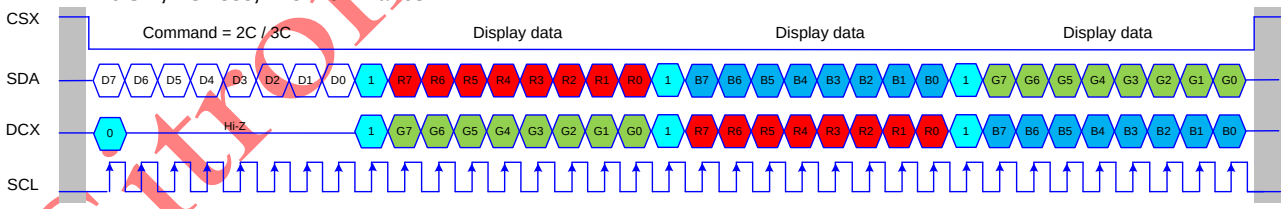
3-wire SPI, RGB565, 1P1T for 2 lanes



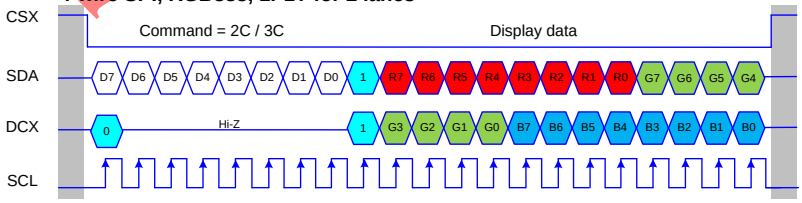
3-wire SPI, RGB565, 1P1T for 1 lane



4-wire SPI, RGB888, 2P3T for 2 lanes



4-wire SPI, RGB888, 1P1T for 2 lanes



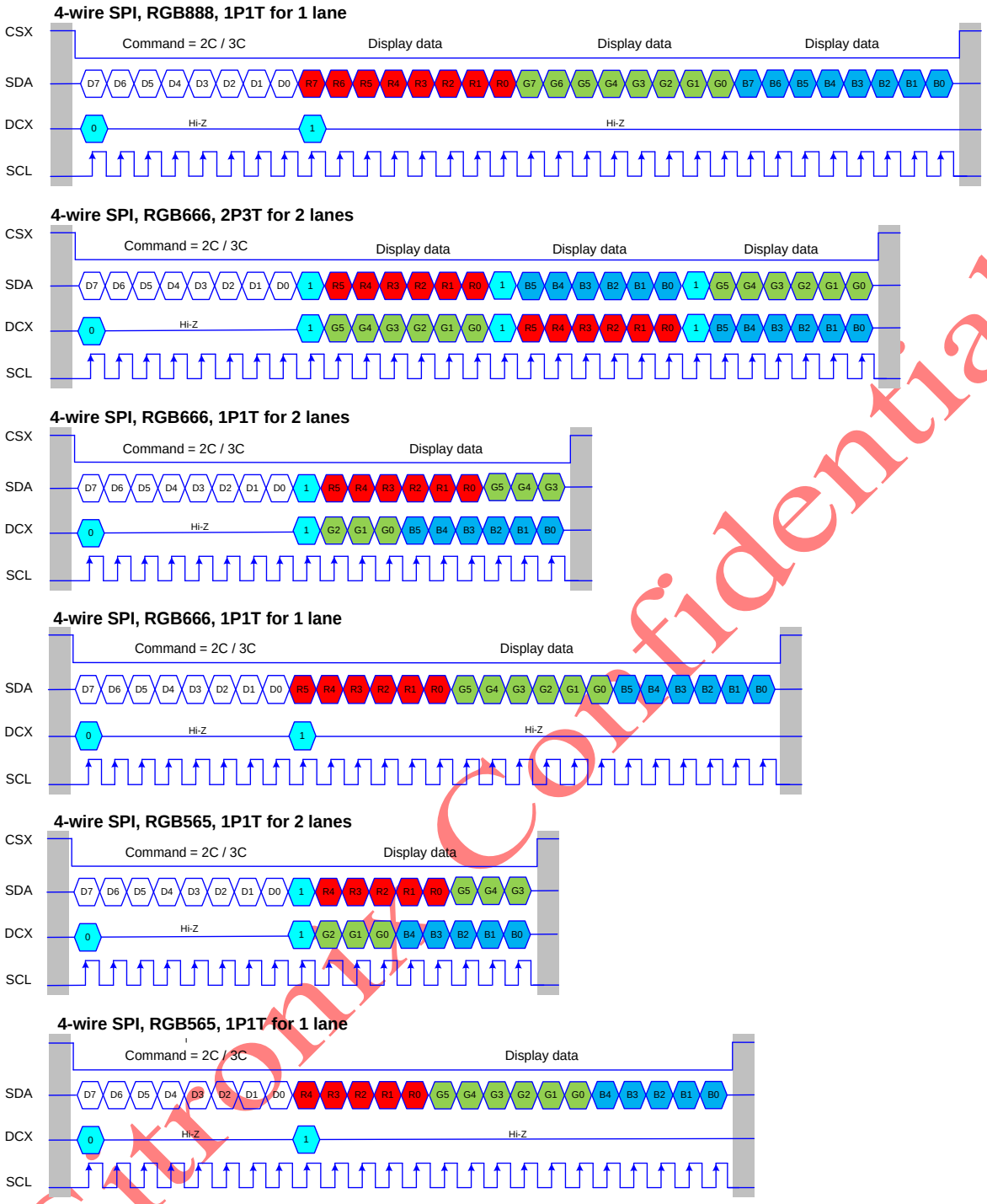


Figure 13 Dual-SPI write protocol

8.3.3 Read Mode

In the read mode of the interface, the host reads the register value from the ST7802. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. If the IM[1:0] pins as “00” level, the read sequence is the same as 3-wire SPI read protocol. If the IM[1:0] pins as “01” level, the read sequence is the same as 4-wire SPI read protocol.

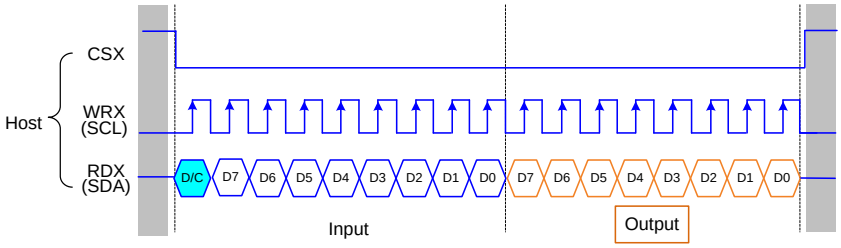


Figure 14 3-wire serial interface read protocol

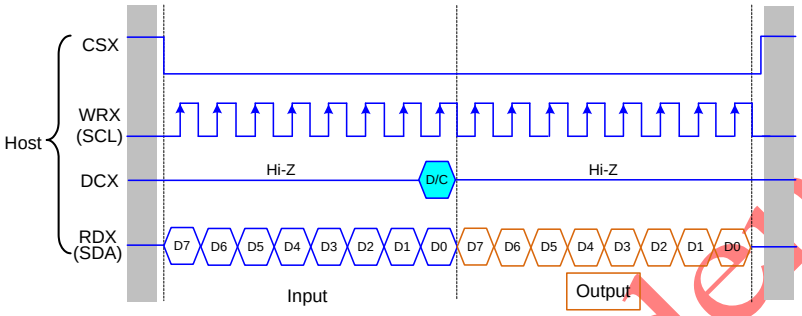


Figure 15 4-wire serial interface read protocol

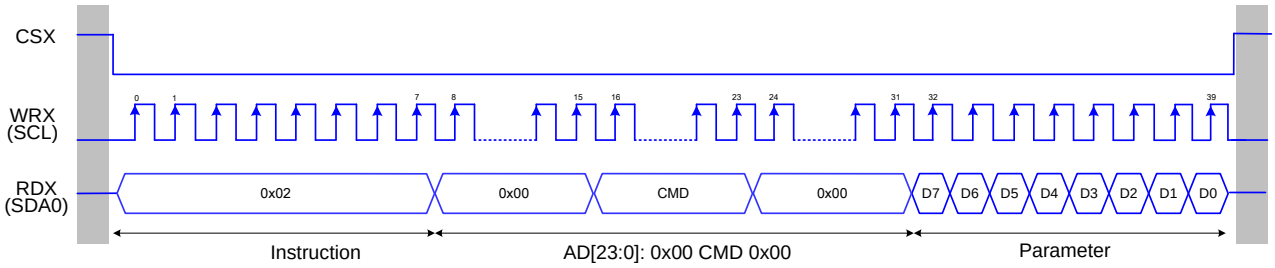
8.4 MSPI Interface

The Multi-SPI interface is selected by setting the IM[1:0] pins as “10” level. The following are the pin names and descriptions.

Pin Name	Description
WRX	Serial input CLK (SCL)
RDX	Serial input data and output data SDA0
DCX	Serial input data SDA1
D0	Serial input data SDA2
D1	Serial input data SDA3
D2	Serial input data SDA4
D3	Serial input data SDA5
D4	Serial input data SDA6
D5	Serial input data SDA7

8.4.1 Write command mode

When host writes commands or parameter to ST7802, host needs to send 1 byte of instruction and 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command and 1 byte of 0x00. After host sending instruction and AD[23:0], the following data is parameter (are parameters). When the last bit of parameter has been sent, CSX pin should be returned “1” level.

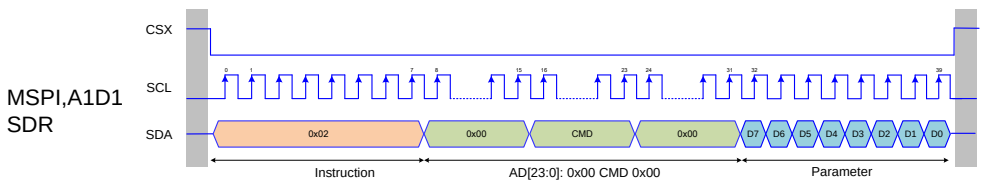


8.4.2 Write pixel data

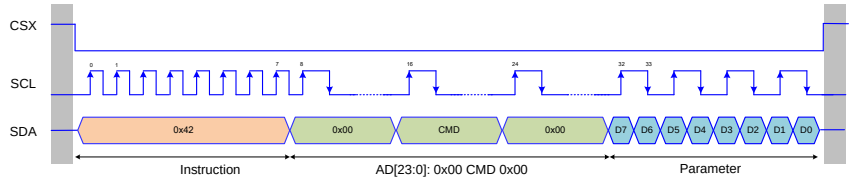
In write pixel data mode, the host sends one byte of instruction, 3 bytes of AD[23:0] and pixel data. AD[23:0] is composed of 0x00, 0x2C(0x3C) and 0x00. Parameters are pixel data according to different data format.

The instruction is transferred only by one lane, but AD[23:0] and pixel data can be transferred by 1,2,4,8 lanes depending on the instruction value. Except single data rate(SDR), ST7802 also supports double data rate(DDR) by instruction value.

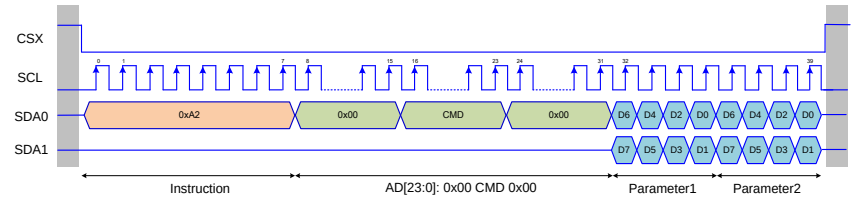
R/W	SDR/DDR	Symbol	Instruction	Lane, SDR/DDR		
				Instruction	Address	Data
Write	SDR (MSPI_DDR_EN=0)	A1D1	0x02	1 Lane SDR	1 Lane SDR	1 Lane SDR
		A1D2	0xA2		1 Lane SDR	2 Lane SDR
		A2D2	0x22		2 Lane SDR	2 Lane SDR
		A1D4	0x32		1 Lane SDR	4 Lane SDR
		A4D4	0x12		4 Lane SDR	4 Lane SDR
		A1D8	0xB2		1 Lane SDR	8 Lane SDR
		A8D8	0x82		8 Lane SDR	8 Lane SDR
	DDR Type 1 (MSPI_DDR_EN=1) (only support pixel data)	A1D2	0xA2	1 Lane SDR	1 Lane SDR	2 Lane **DDR**
		A2D2	0x22		2 Lane SDR	2 Lane **DDR**
		A1D4	0x32		1 Lane SDR	4 Lane **DDR**
		A4D4	0x12		4 Lane SDR	4 Lane **DDR**
		A1D8	0xB2		1 Lane SDR	8 Lane **DDR**
		A8D8	0x82		8 Lane SDR	8 Lane **DDR**
	DDR Type 2	A1D1	0x42	1 Lane SDR	1 Lane **DDR**	1 Lane **DDR**
		A1D2	0xE2		1 Lane **DDR**	2 Lane **DDR**
		A2D2	0x62		2 Lane **DDR**	2 Lane **DDR**
		A1D4	0x72		1 Lane **DDR**	4 Lane **DDR**
		A4D4	0x52		4 Lane **DDR**	4 Lane **DDR**
		A1D8	0xF2		1 Lane **DDR**	8 Lane **DDR** (only support pixel data)
		A8D8	0xC2		8 Lane **DDR** (4 Bytes)	8 Lane **DDR** (only support pixel data)
Read	SDR	NA	0x03	1 Lane SDR	1 Lane SDR	1 Lane SDR



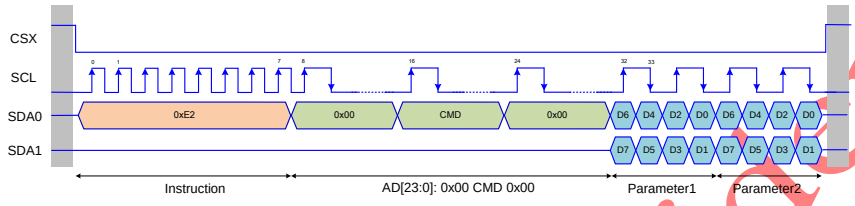
MSPI,A1D1 DDR



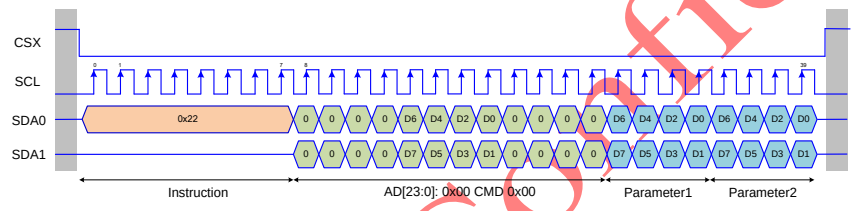
MSPI,A1D2 SDR



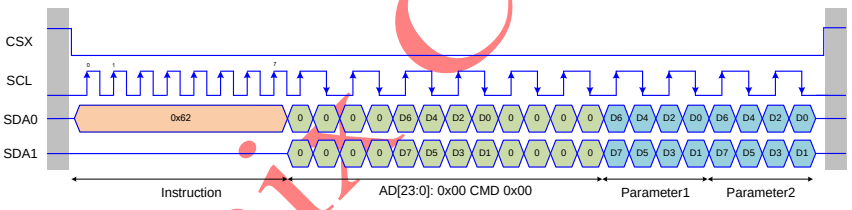
MSPI,A1D2 DDR



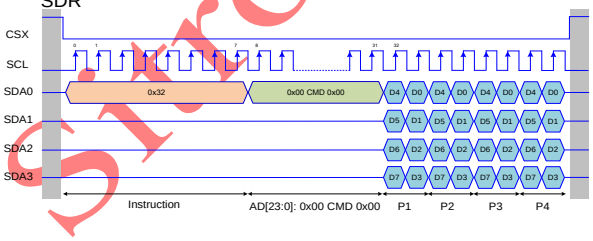
MSPI,A2D2 SDR



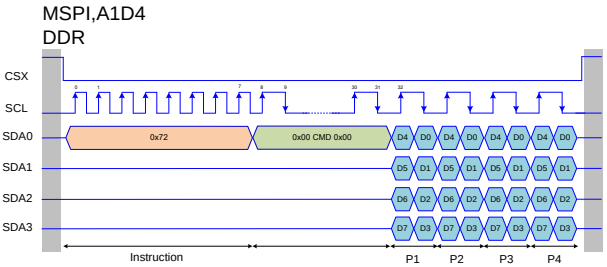
MSPI,A2D2 DDR



MSPI,A1D4 SDR

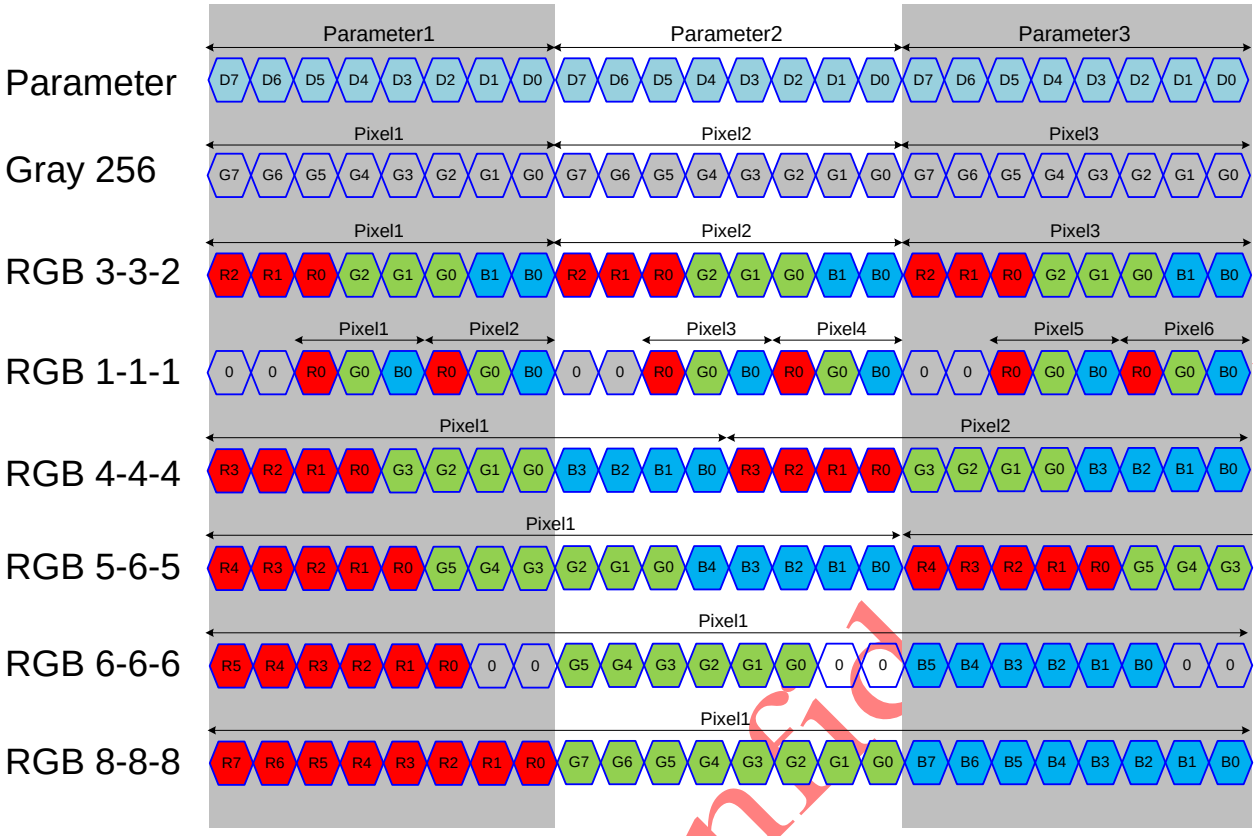


MSPI,A1D4 DDR



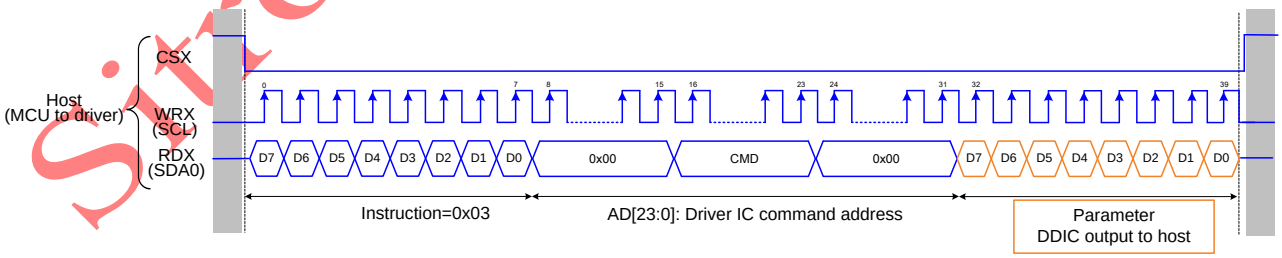
The following table are the color format supported in MSPI mode.

Color Format	IFPF[2:0]	SDR				DDR			
		A1D1	A1D2 A2D2	A1D4 A4D4	A1D8 A8D8	A1D1	A1D2 A2D2	A1D4 A4D4	A1D8 A8D8
8-bit/pixel, gray 256	3'b001	O	O	O	X	O	O	X	X
RGB 3-3-2, 256 colors	3'b010	O	O	O	X	O	O	X	X
RGB 1-1-1, 8 colors	3'b011	O	O	X	X	O	X	X	X
RGB 4-4-4, 4096 colors	3'b100	O	O	O	O	O	O	O	X
RGB 5-6-5, 65K colors	3'b101	O	O	O	O	O	O	O	X
RGB 6-6-6, 262K colors	3'b110	O	O	O	O	O	O	O	O
RGB 8-8-8, 16.7M colors	3'b111	O	O	O	O	O	O	O	O



8.4.3 Read Mode

The read mode of the interface means that the micro controller reads register value from the ST7802. The host first has to send a instruction (0x03) for read mode, then the following byte is transmitted in the opposite direction. The SDO pin is designed as a tri-state pin. It only as a output pin after the last bit of AD[23:0] has been received, and it would return a input pin after read mode. If the host uses the same pin for writing command and receiving parameter, the SDO pin can be connected to SDA pin. In the end of reading progress, CSX is required to set high level for next new command.



8.5 MIPI-DSI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

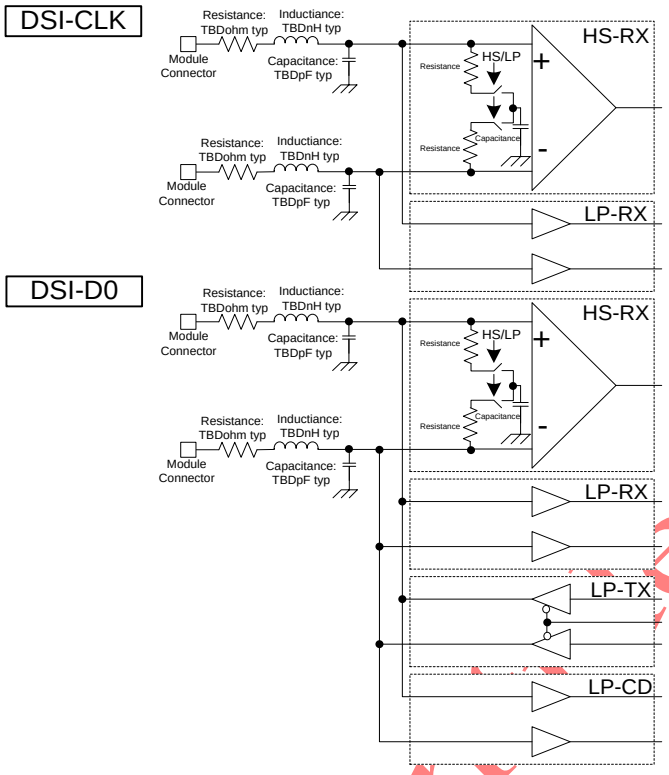
DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High-Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low-Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

8.5.1 Display Module Pin Configuration for DSI



8.5.2 Display Serial Interface (DSI)

8.5.2.1 General description

The communication can be separated two different levels between the MCU and the display module:

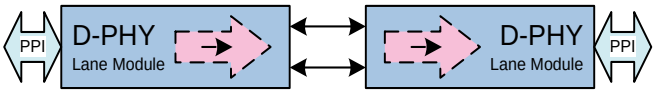
- Interface level : Low level communication
- Packet level : High level communication

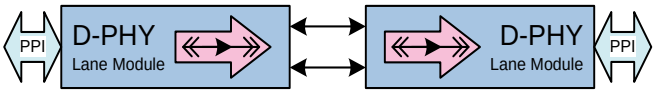
8.5.2.2 Interface level communication

8.5.2.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low-Power (LP) or High-Speed (HS) mode. Data lane1, data lane2 and data lane3 can be driven High-Speed mode only.

The Interface Color Lane Types and Support Mode

	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	

Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	

Low-Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a Low-Power mode.

High-Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High-Speed (HS) and Low-Power (LP) lane pair are defined below.

Lane Pair State Code	Line Voltage Levels		High-Speed(HS)	Low-Power(LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Request	Mark-0
LP-10	LP High	LP Low	N/A	LP-Request	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

Notes:

1. During High-Speed transmission the Low-Power observe LP-00 on the Lines.

2. If LP-11 occurs during Escape mode the Lane returns to Stop state.

8.5.2.2.2 DSI-CLOCK Lanes

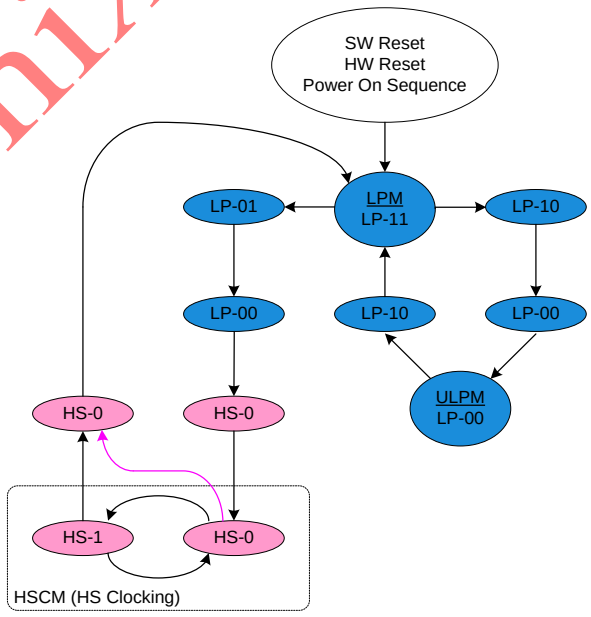
DSI-CLK+/- lanes can be driven into three different power modes: Low-Power Mode (LPM LP-11), Ultra-Low Power Mode (ULPM) or High-Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low-Power) when there is entering or leaving Low-Power Mode (LPM) or Ultra-Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low-Power) when there is entering in or leaving out High-Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.



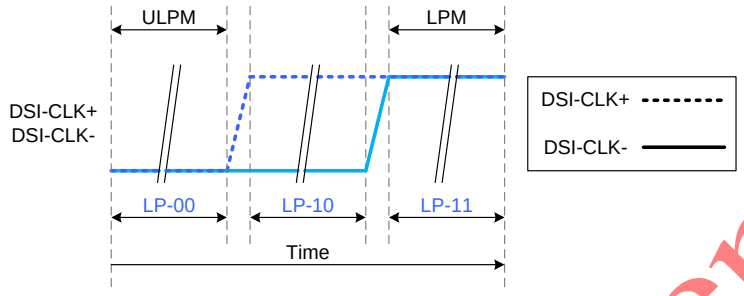
8.5.2.2.2.1 Low-Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low-Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code , in three different ways:

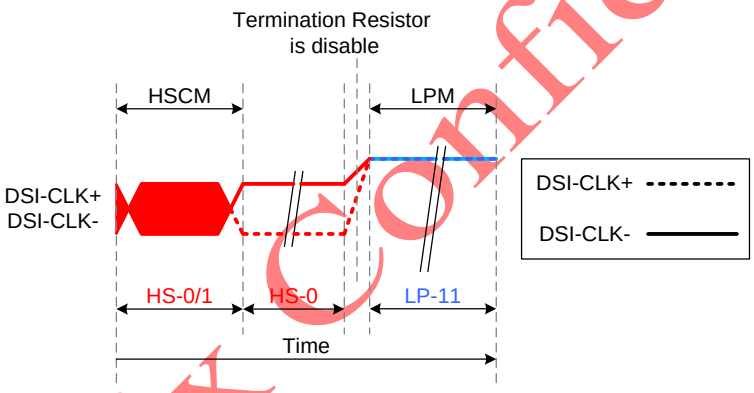
After SW Reset, HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP10=>LP-11(LPM).

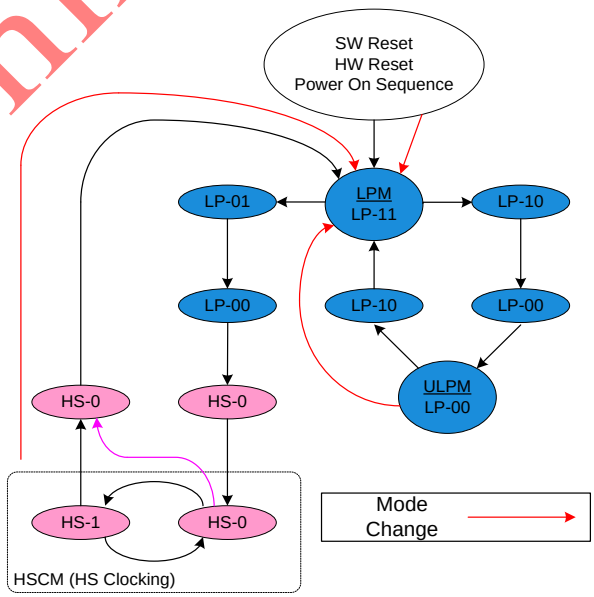
This sequence is illustrated below.



After DSI-CLK+/- lanes are leaving High-Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence form HSCM to LPM is illustrated below.

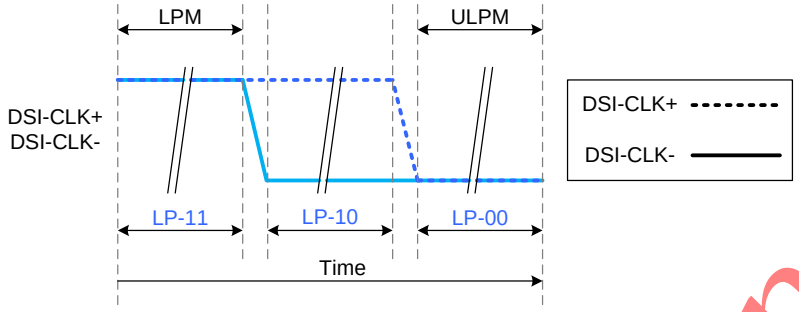


All three mode changes are illustrated a flow chart below.

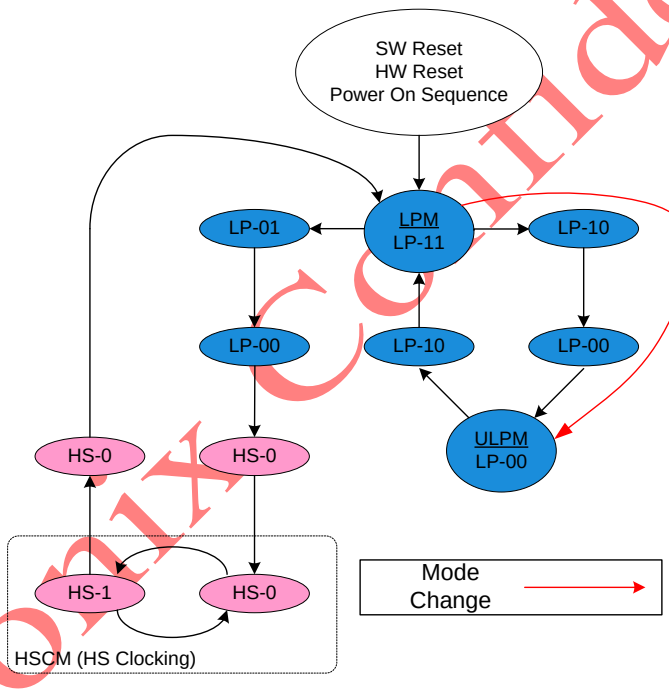


8.5.2.2.2.2 Ultra-Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra-Low Power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility if from the Low-Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence from LPM to UPLM is illustrated below:

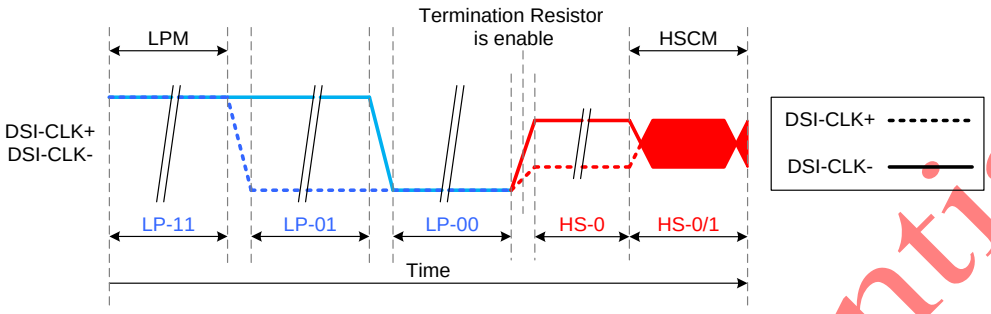


The mode change is also illustrated below:

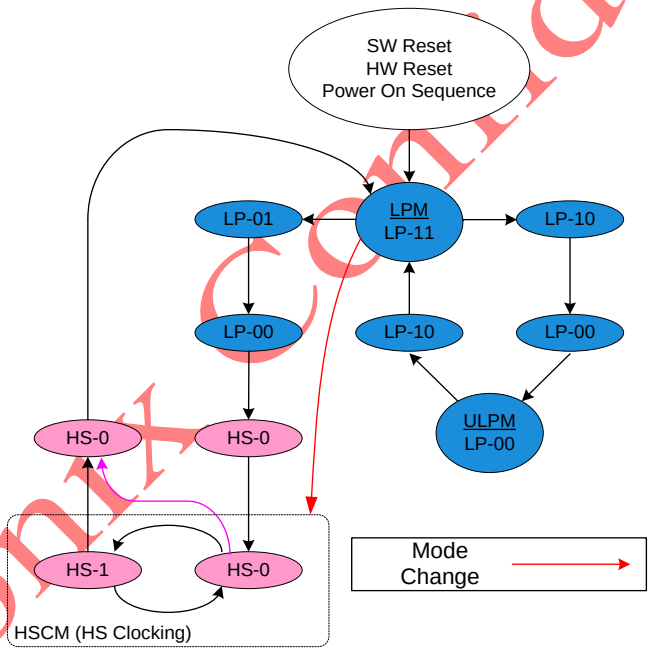


8.5.2.2.2.3 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High-Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low-Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence from LPM to HSCM is illustrated below.

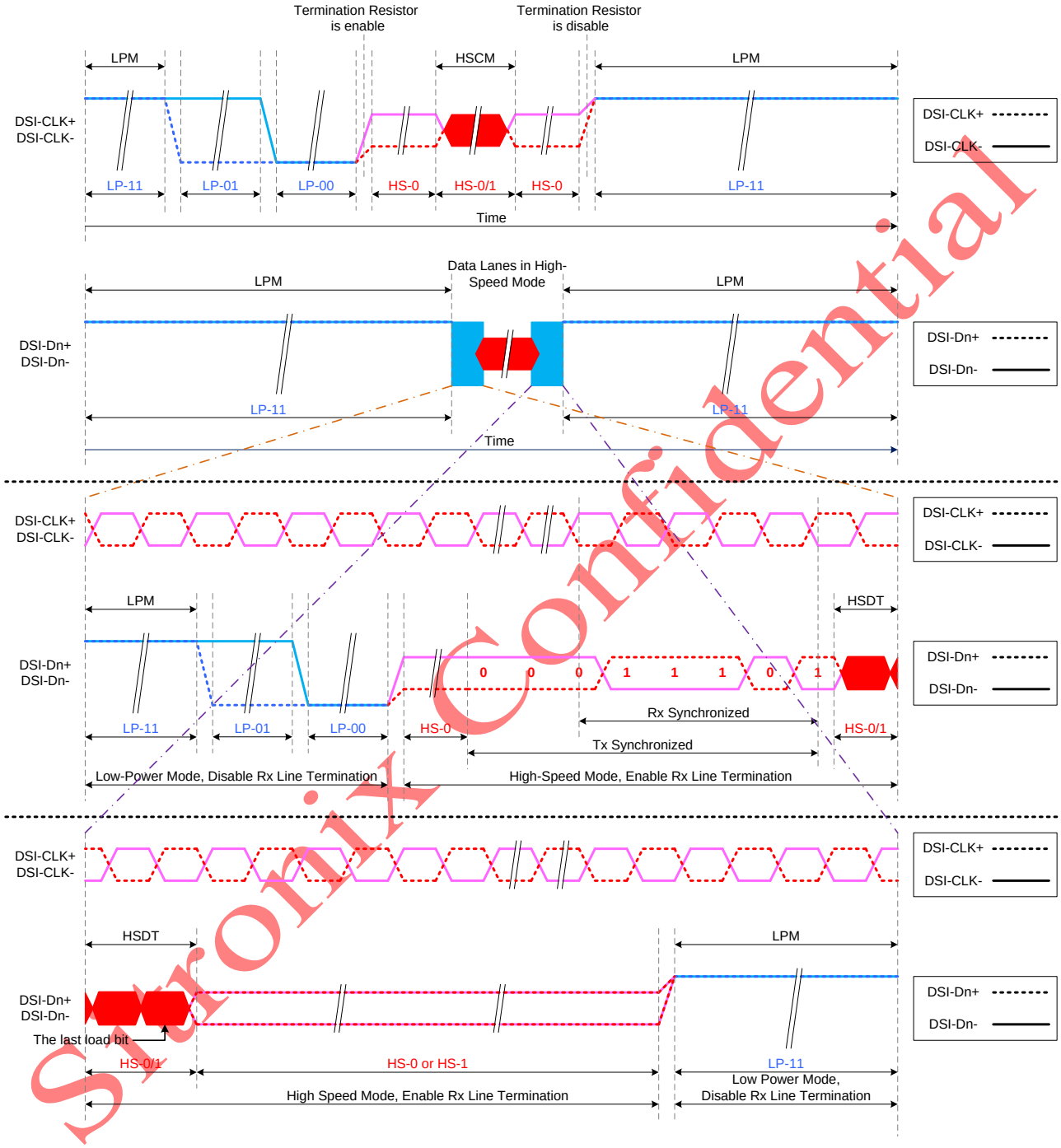


The mode change is also illustrated below:



The High-Speed clock (DSI-CLK+/-) is started before High-Speed data is sent via DSI-Dn+/- lanes. The High-Speed clock continues clocking after the High-Speed data sending has been stopped.

High-Speed Clock Burst



Note:

If the last load bits is HS-0, the transmitter changes form HS-0 to HS-1.

If the last load bits is HS-1, the transmitter changes form HS-1 to HS-0.

8.5.2.2.3 DSI-DATA Lanes

8.5.2.2.3.1 General

DSI-D0+/- data lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lane is used)

• High-Speed Data Transmission (DSI-D0+/-, DSI-D1+/-, DSI-D2+/- and DSI-D3+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lane is used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

8.5.2.2.3.2 ESCAPE MODE

Data lane0 (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low-Power (LP) mode.

These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is reset the display module

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

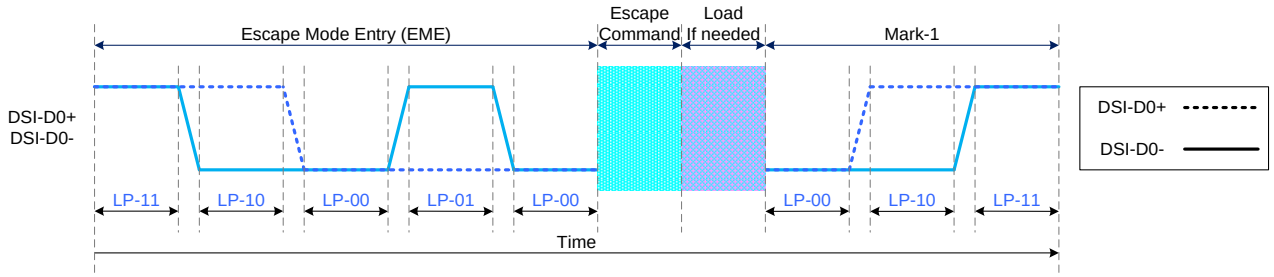
• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:



The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided two different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the Low-Power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g.

Escape commands are defined on the following table.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit➔Last Bit Transmitted)	Rx	Tx
Low-Power Data Transmission	Mode	1110 0001 $_{bin}$	-	○
Ultra-Low Power Mode	Mode	0001 1110 $_{bin}$	○	○
Underfined-1, Note 1	Mode	1001 1111 $_{bin}$	-	-
Underfined-2, Note 1	Mode	1101 1110 $_{bin}$	-	-
Remote Application Reset	Trigger	0110 0010 $_{bin}$	-	-
Underfined-3, Note 1	Trigger	0101 1101 $_{bin}$	-	-
Acknowledge	Trigger	0010 0001 $_{bin}$	-	○
Unknow-5, Note 1	Trigger	1010 0000 $_{bin}$	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "○"=Supported

4. "-"=Not Supported

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low-Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Load (Data):

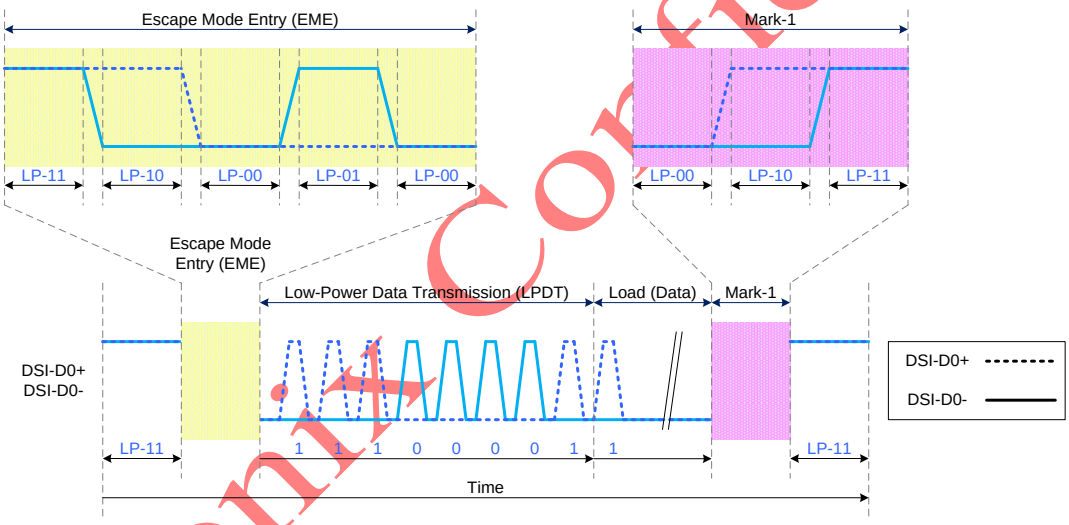
One or more bytes (8 bits)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

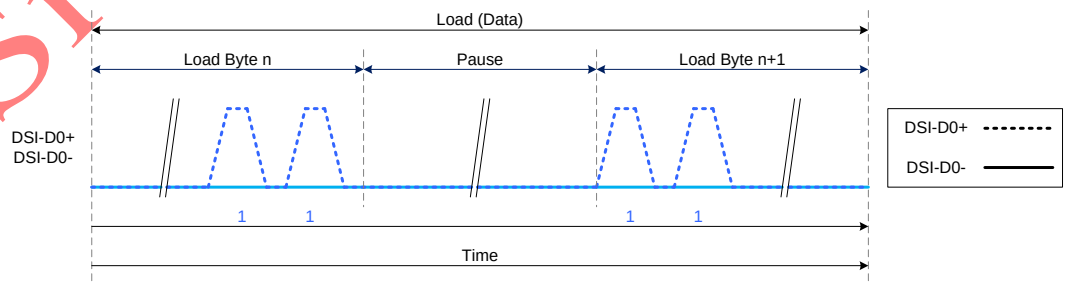
• End: LP-11

The sequence of LPDT is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical '1' in this example

The sequence of PAUSE during LPDT is illustrated below:



Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

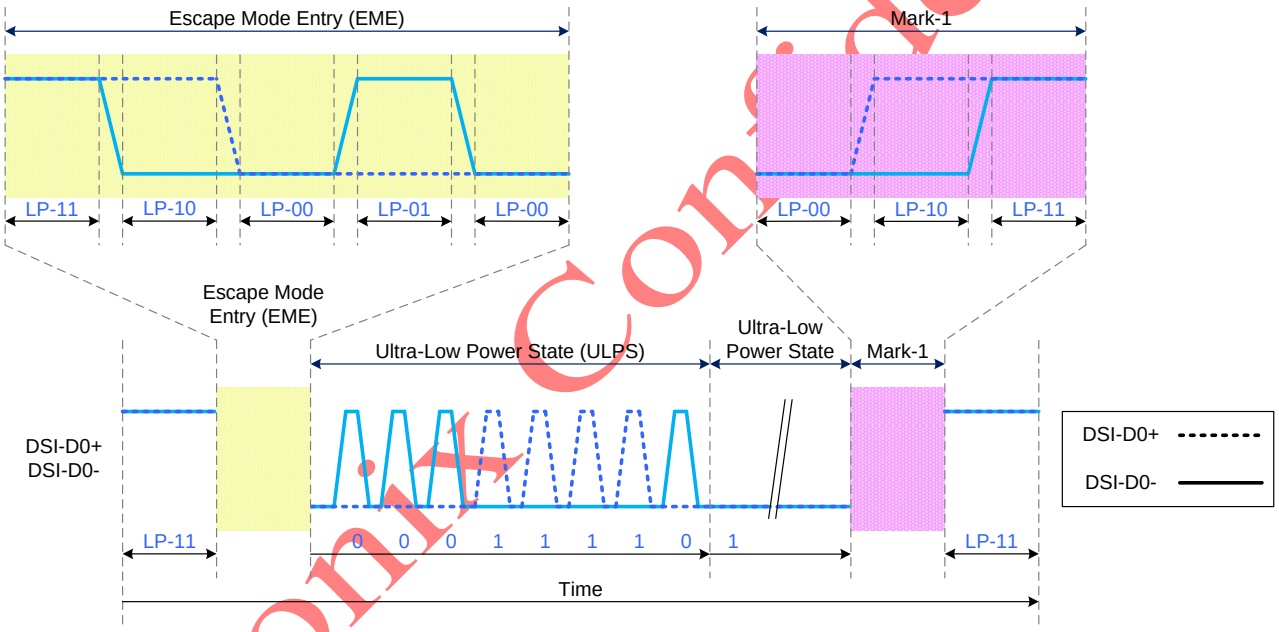
• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence of ULPS is illustrated for reference purposes below:



Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

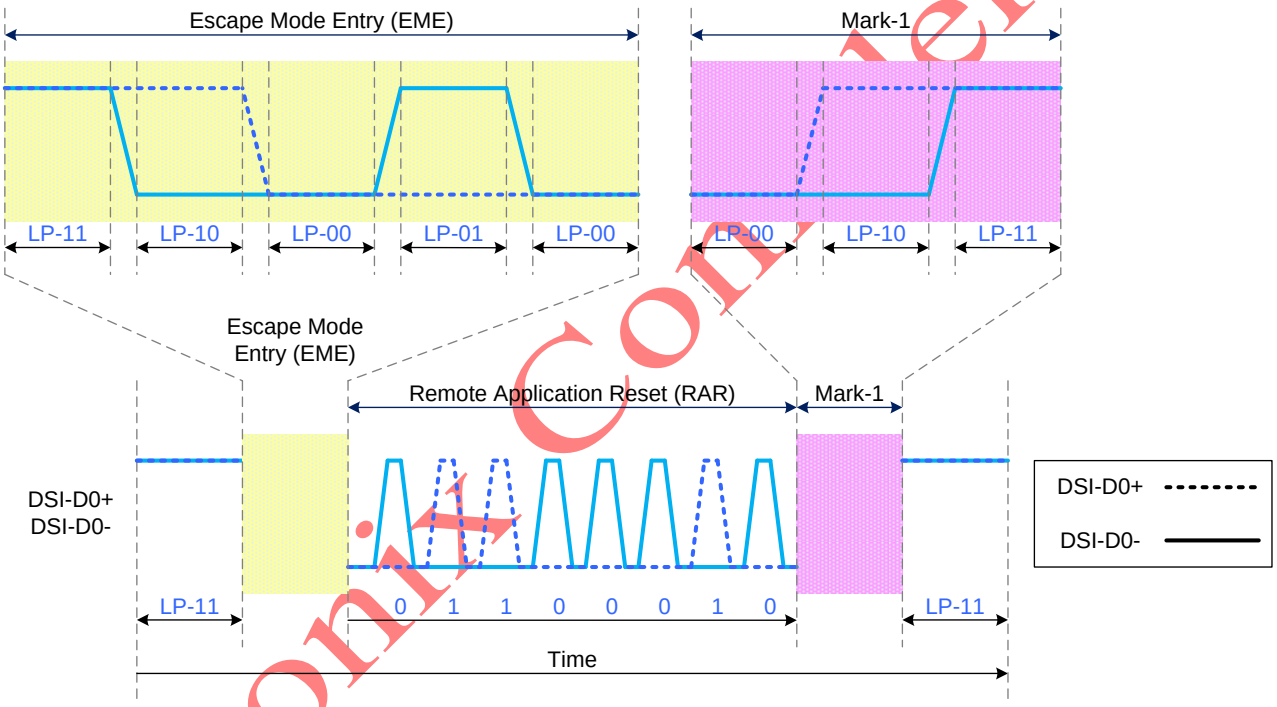
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence of RAR is illustrated for reference purposes below:



Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

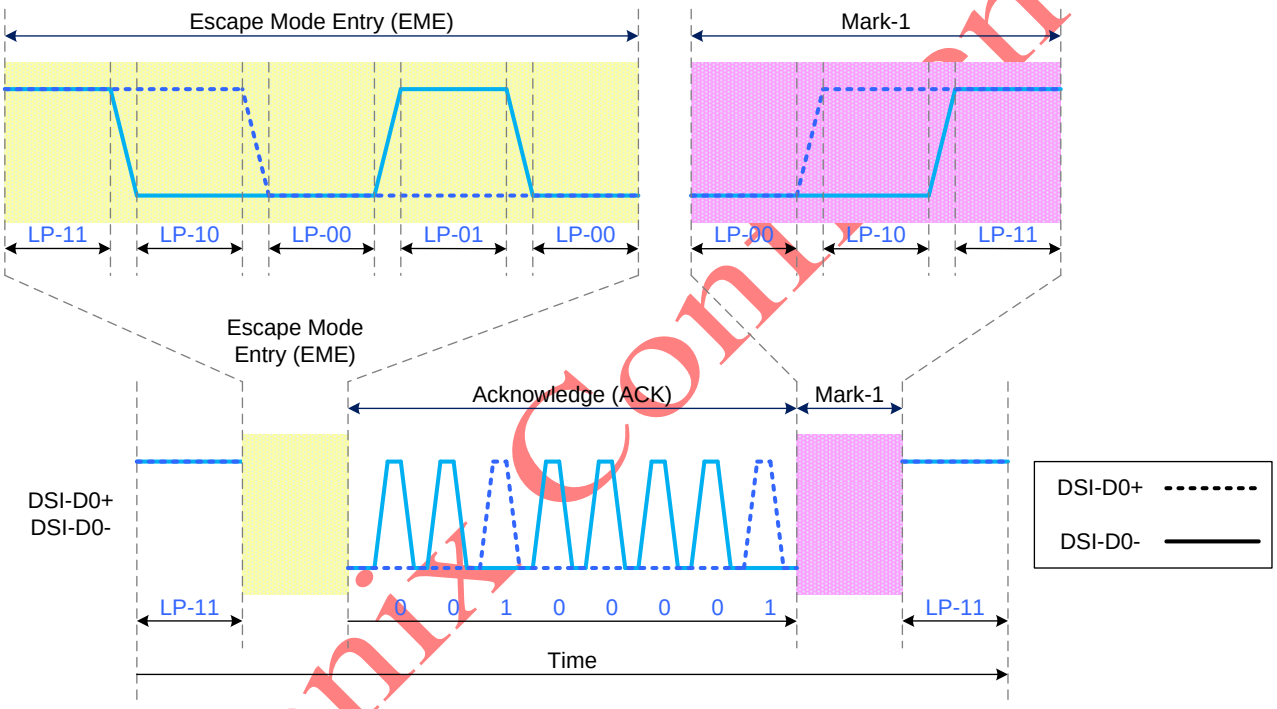
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence of ACK is illustrated for reference purposes below:



8.5.2.2.3.3 High-Speed Data Transmission (HSDT)

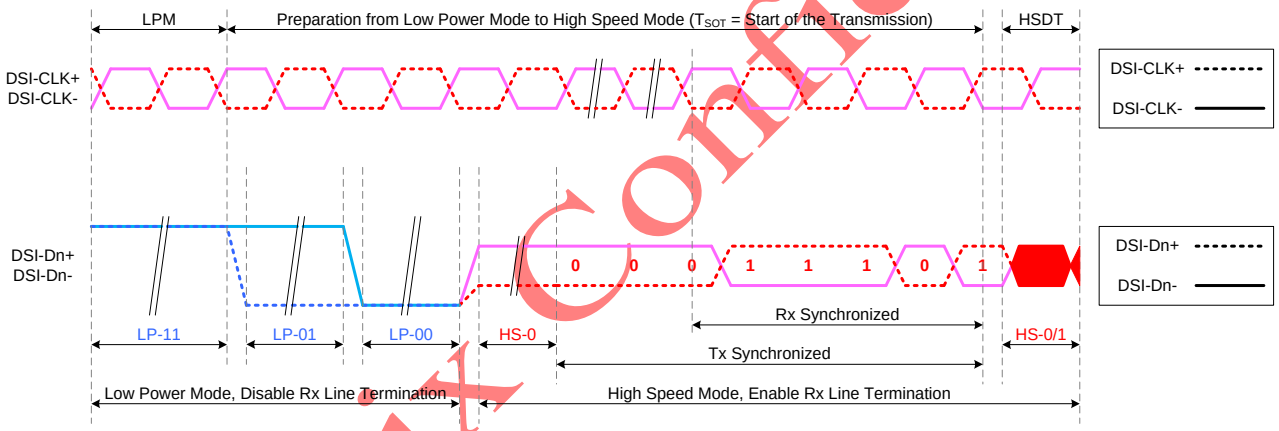
Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

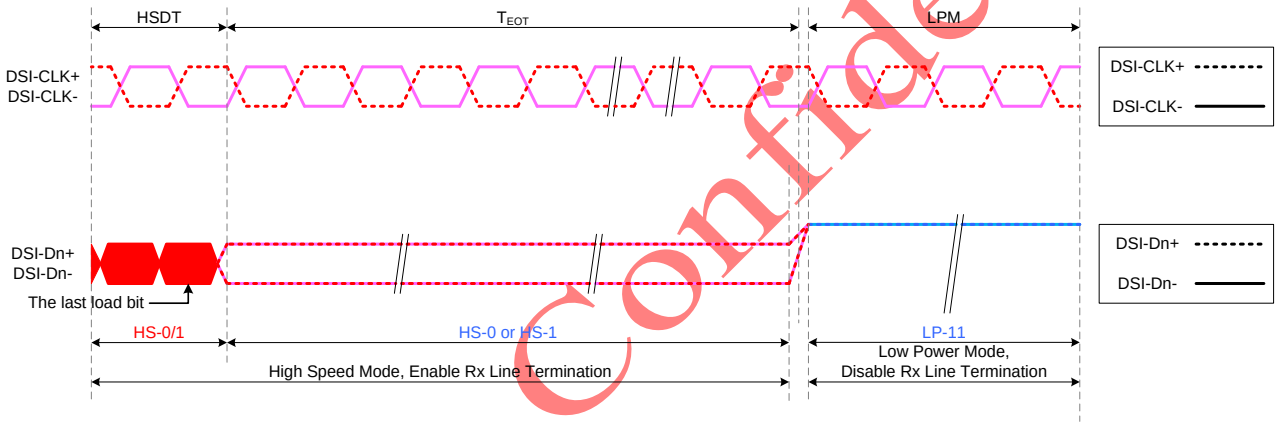
• Stops High-Speed Data Transmission

MCU changes to HS-1, if the last load bit is HS-0

MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

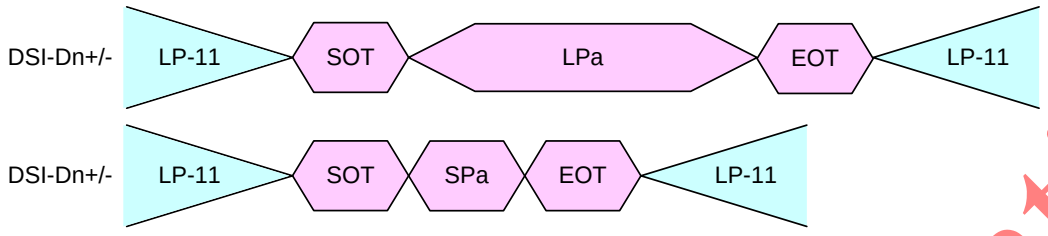


Burst of the High-Speed Data Transmission (HSDT)

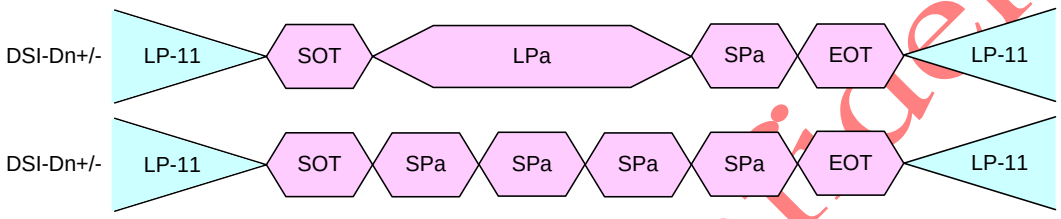
The burst of the High-Speed Data Transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

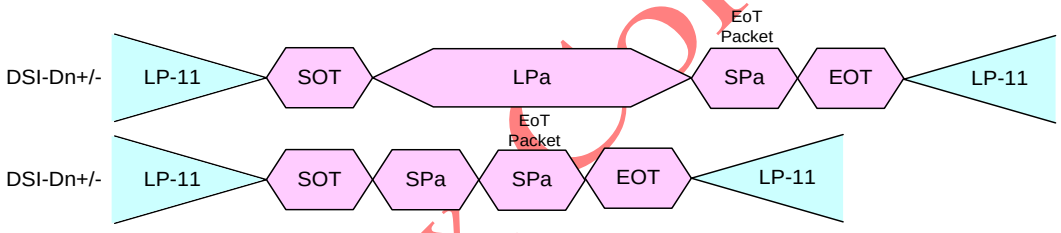
Single Packet in High-Speed Data Transmission with EoT packet disabled



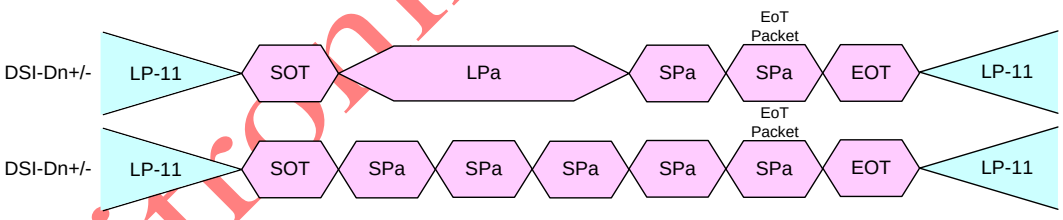
Multiple Packets in High-Speed Data Transmission with EoT packet disabled



Single Packet in High-Speed Data Transmission with EoT packet enable



Multiple Packets in High-Speed Data Transmission with EoT packet enable



Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low-Power Mode, Data lanes are’1’s (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

8.5.2.2.3.4 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module is using the same sequence when this bus turnaround procedure is used.
This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

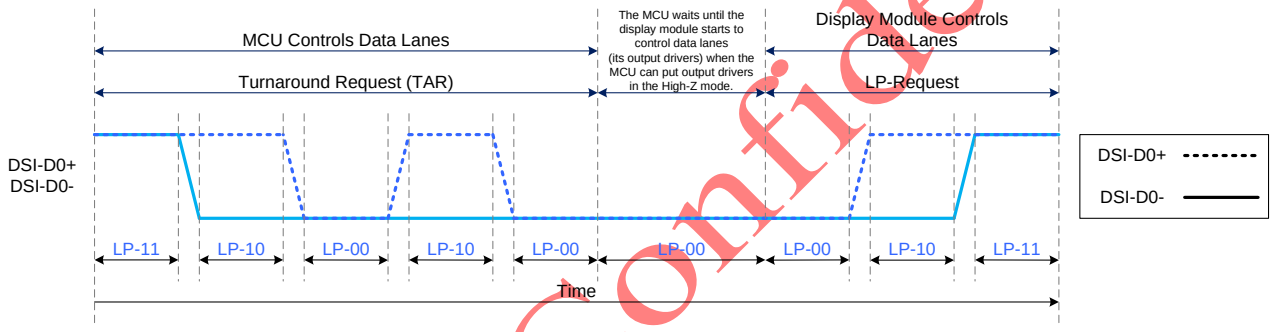
• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.



MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

8.5.2.3 Packer Level Communication

8.5.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low-Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

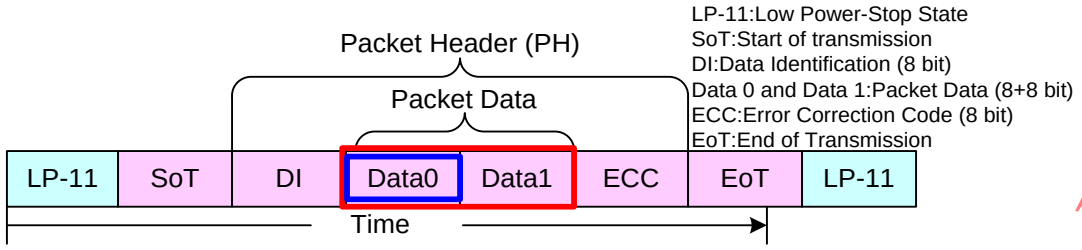
The lengths of the packets are

• Short Packet (SPa): 4 bytes

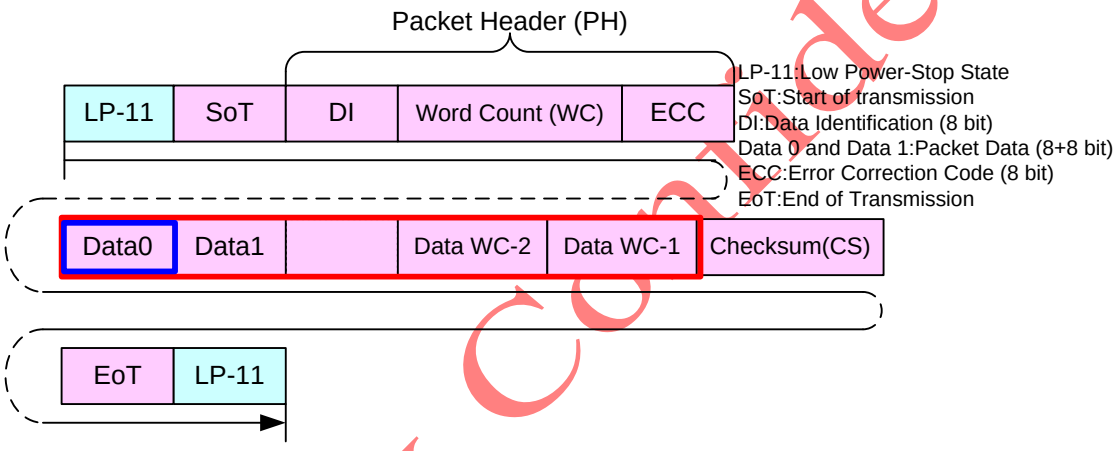
• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

Short Packet (SPa) Structure



Long Packet (LPa) Structure



Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*

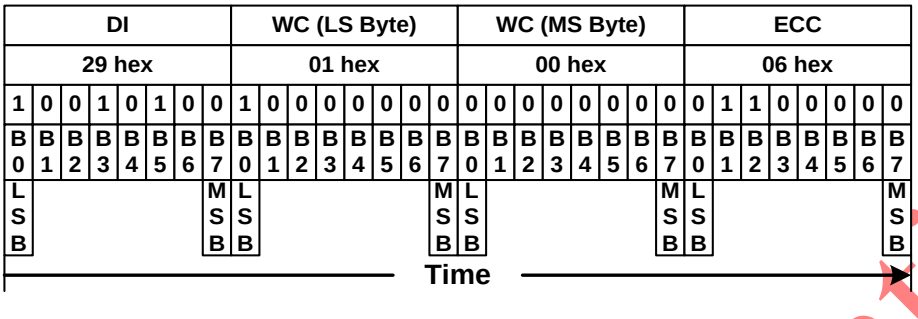
** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

8.5.2.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

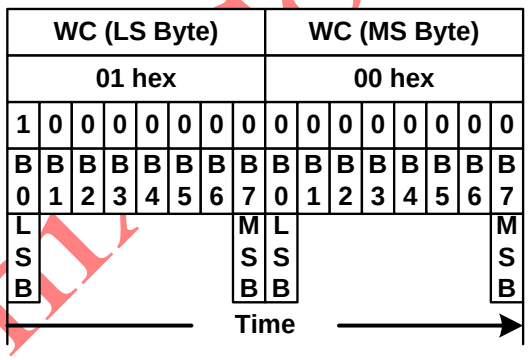
This same order is illustrated for reference purposes below.



8.5.2.3.1.2 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.



8.5.2.3.1.3 Packet Header (PH)

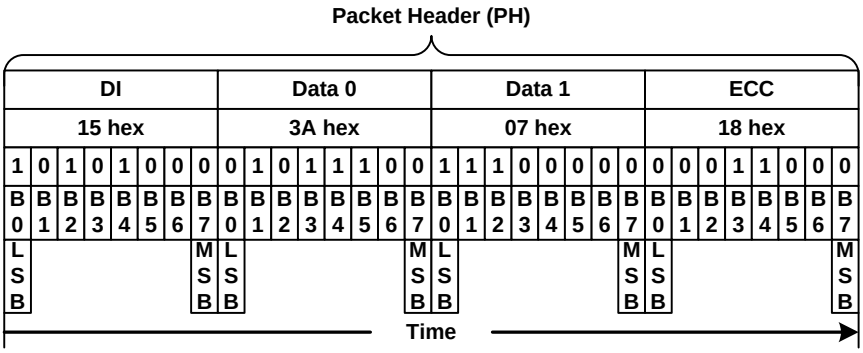
The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short

Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and Data 1
- 4th byte: Error Correction Code (ECC)

Packet Header (PH) on the Short Packet (SPa)



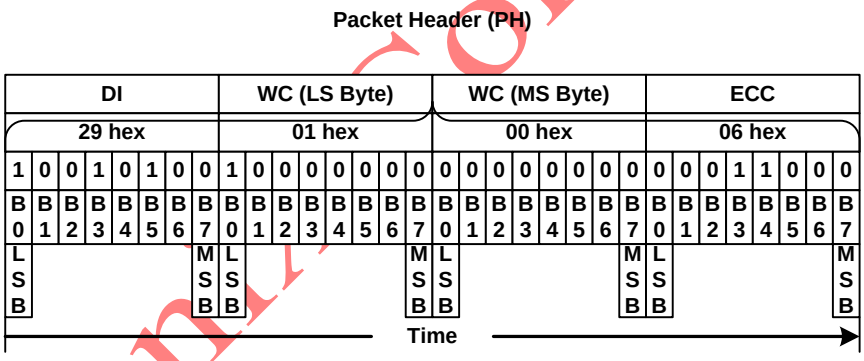
Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

Packet Header (PH) on the Long Packet (LPa)



Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

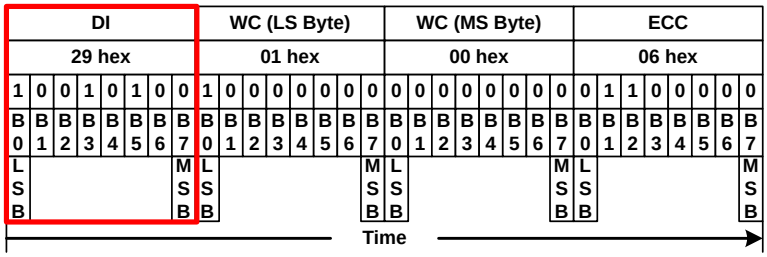
• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

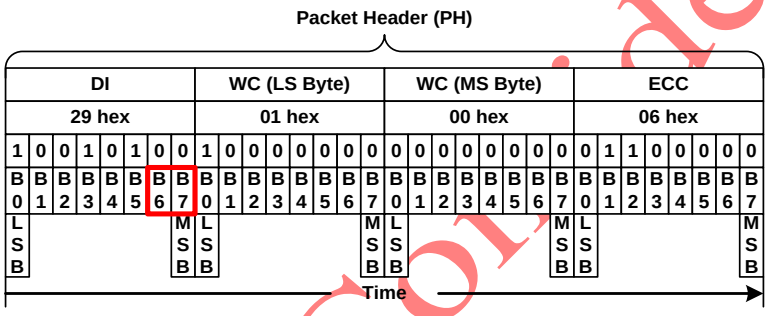
Data Identification (DI) on the Packet Header(PH)



Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

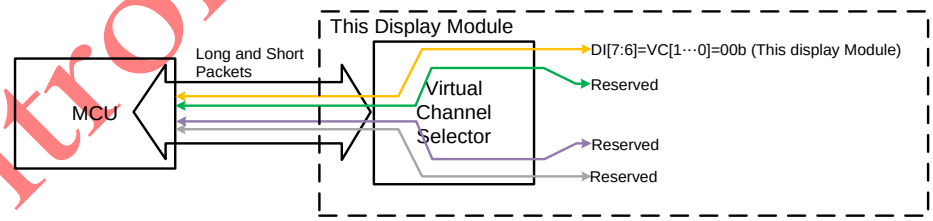


Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

• The MCU is using the virtual channel 0 when it sends packets to this display module

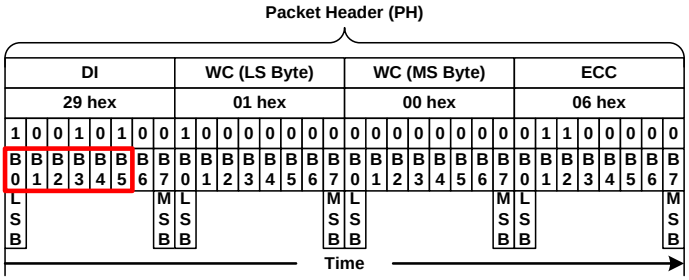
• This display module is also using the virtual channel 0 when it sends packets to the MCU

This configuration of VC is illustrated below.



Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.



This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

Data Type (DT) from MCU to the Display Module (or Other Devices)			
Data Type Hex	**Data Type Binary**	**Description**	**Packet Size**
01h	00 0001	Sync Event, V Sync Start.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

From the Display Module (or Other Devices) to the MCU

Data Type Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

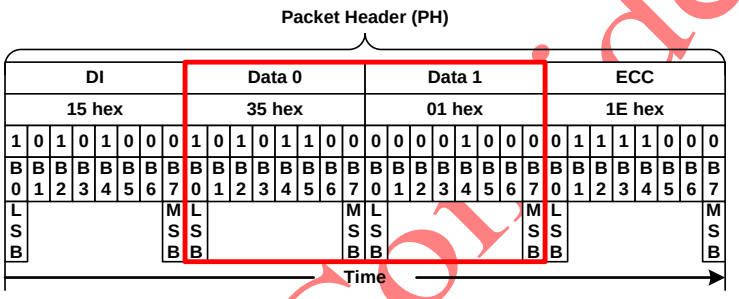
Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

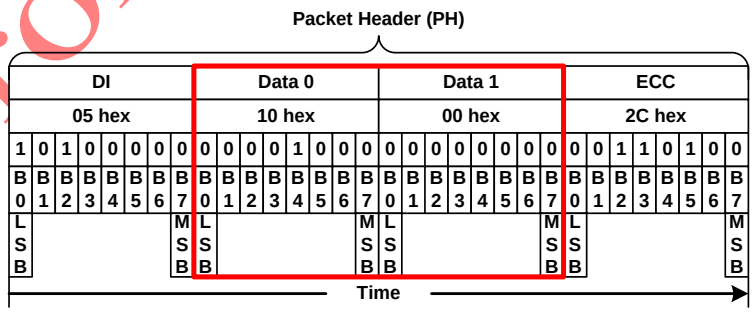


Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

Packet Data (PD) for Short Packet (SPa), 1 Bytes Information



Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

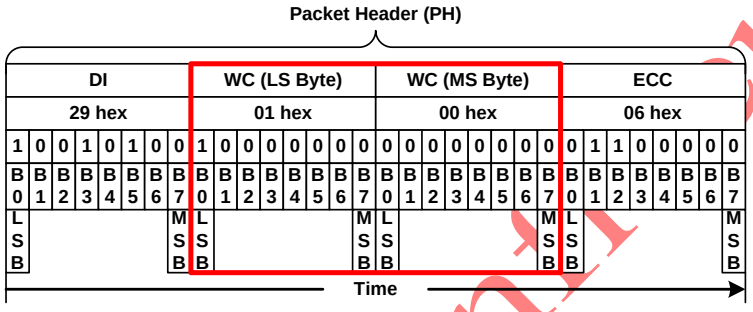
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

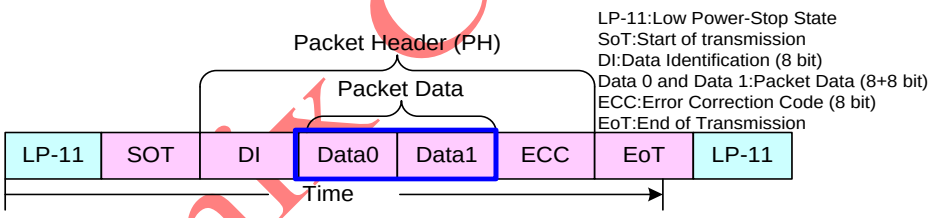
These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

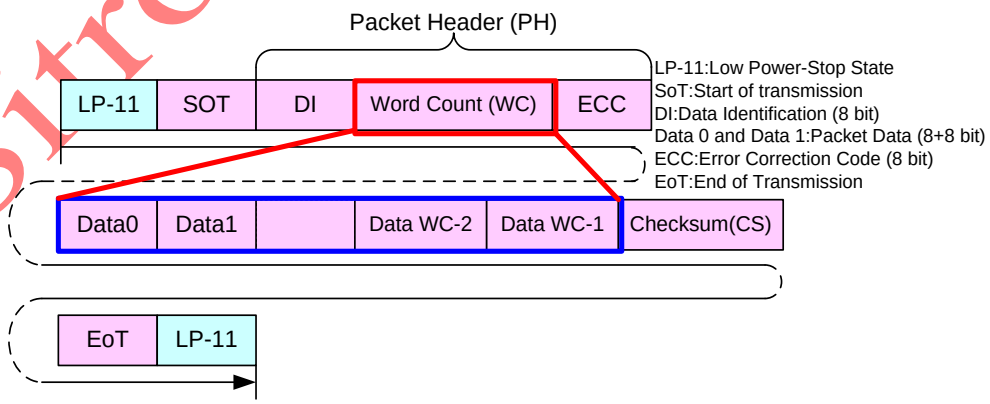
Word Count (WC) on the Long Packet (LPa)



Packet Data (PD) on the Short Packet (SPa)



Packet Data (PD) on the Long Packet (LPa)



Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

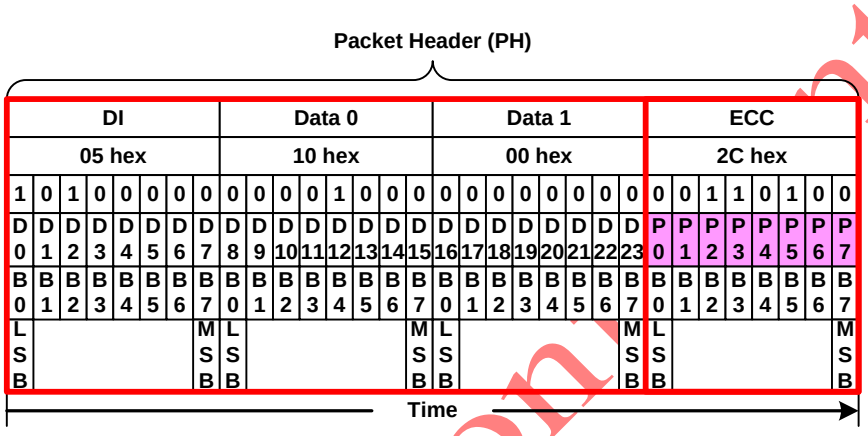
The ECC protects the following field”

• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

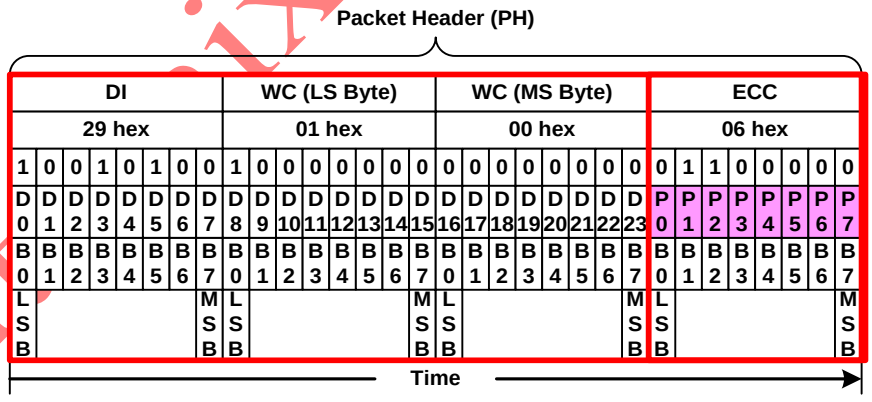
• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

D[23..0] and P[7…0] on the Short Packet (SPa)



D[23…0] and P[7…0] on the Long Packet (LPa)



Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case. Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol ‘^’ is presenting XOR function (Pn is ‘1’ if there is odd number of ‘1’s and Pn is ‘0’ if there is even number of ‘1’s), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

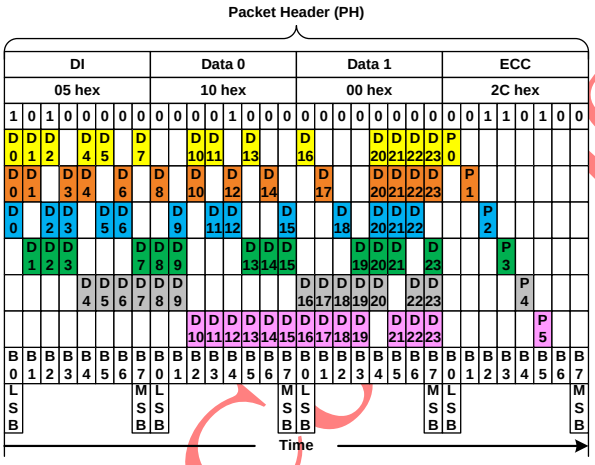
• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

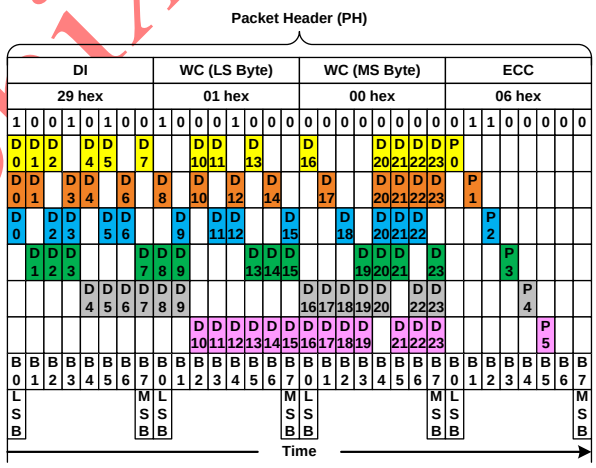
• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

XOR Functionality on the Short Packet (SPa)

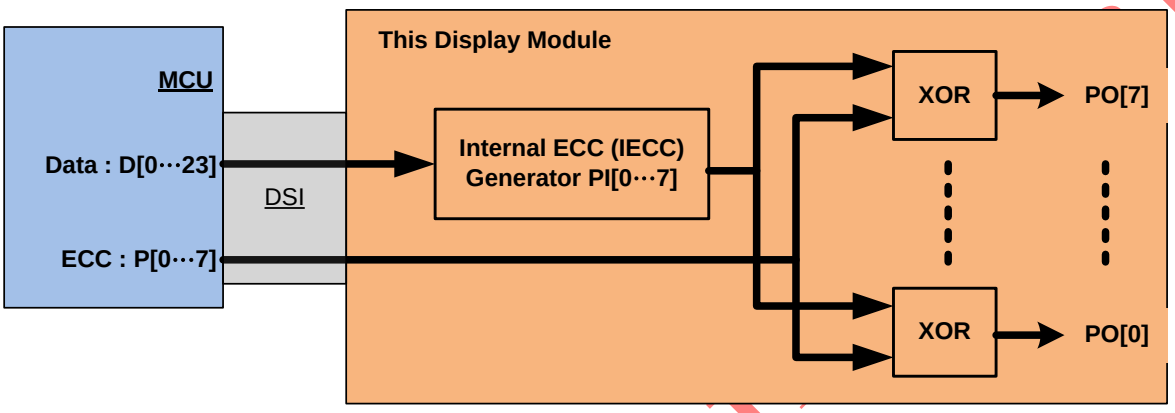


XOR Functionality on the Long Packet (LPa)



The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

Internal Error Correction Code (IECC) on the Display Module (The Receiver)



The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 0 0h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h=>No Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch=> Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

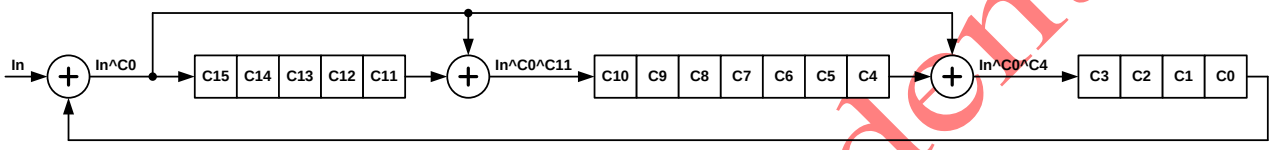
8.5.2.3.1.4 Packet Date (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

8.5.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

16-bit Cyclic Redundancy Check (CRC) Calculation



The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

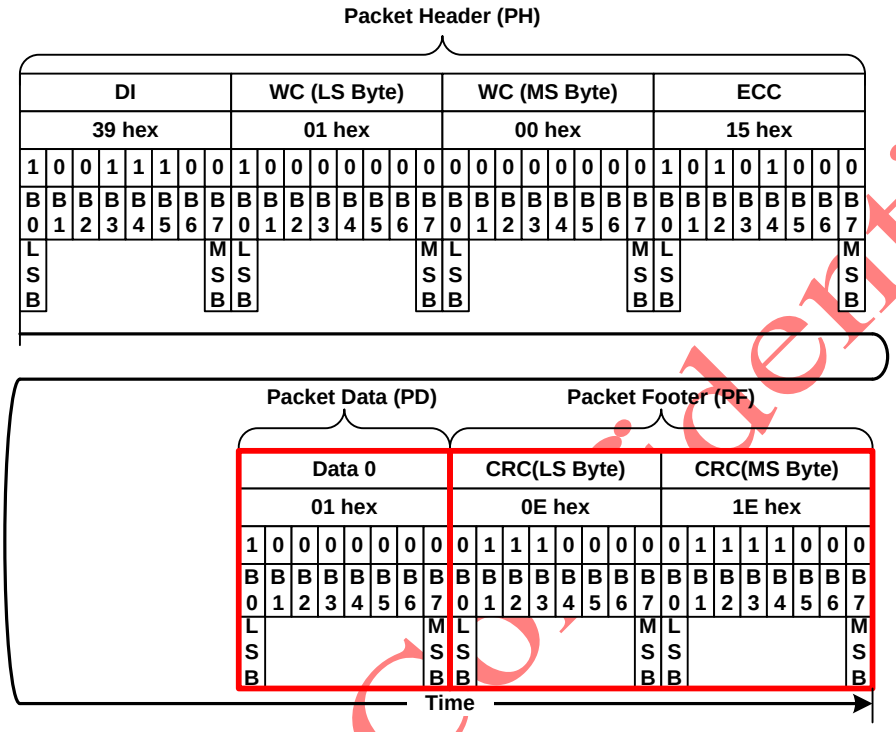
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

CRC Calculation – Packet Data (PD) is 01h

Step	In	In^C0	C15	C14	C13	C12	C11	In^C0^C11	C10	C9	C8	C7	C6	C5	C4	In^C0^C4	C3	C2	C1	C0
0	1(LSB)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1
5	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
6	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
7	0(MSB)	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
8	X	X	0	0	0	1	1	X	1	1	0	0	0	0	0	X	1	1	1	0
CRC Result:			0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0
			MSB																	LSB

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is Illustrated below.

Packet Footer (PF) Example



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

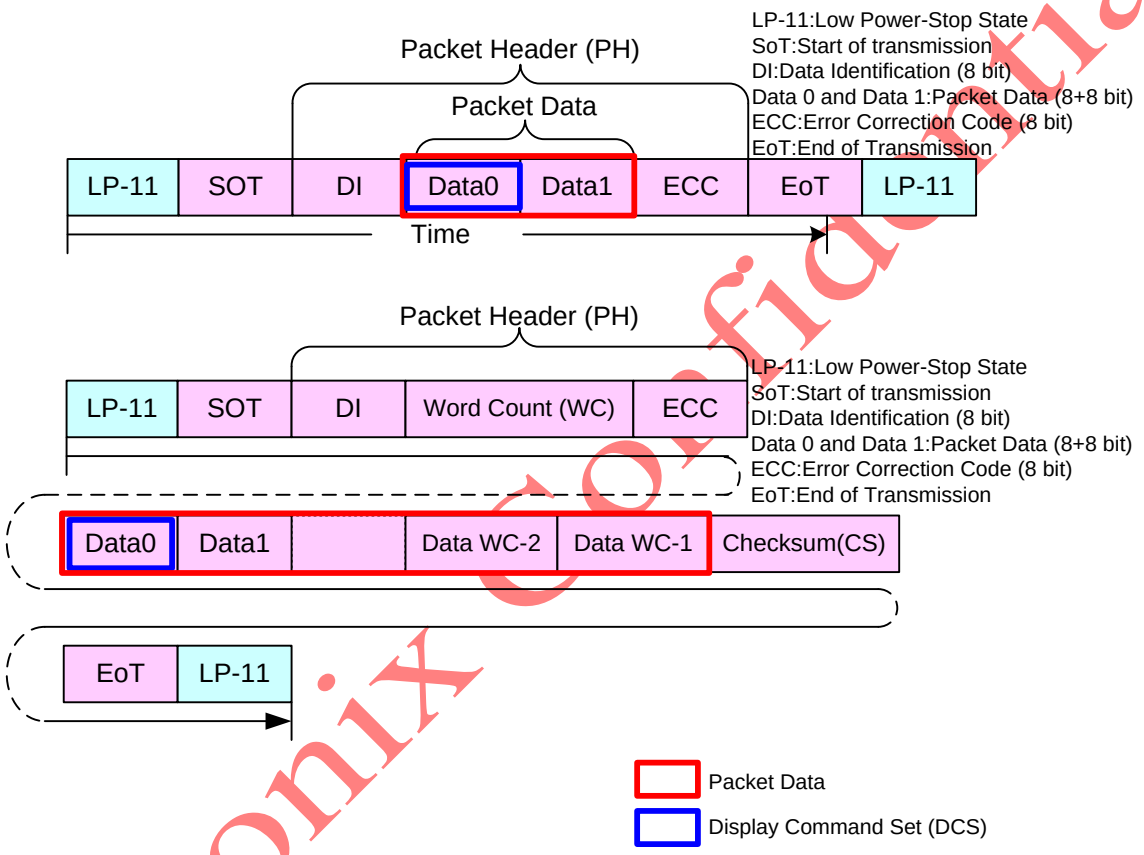
8.5.2.3.2 Packet Transmissions

8.5.2.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD),which is included in Short Packet (SPa) and Long Packet (LPa) as these are illustrated below.

Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)



8.5.2.3.2.2 Packet from the Display Module to the MCU

Used Packet Types

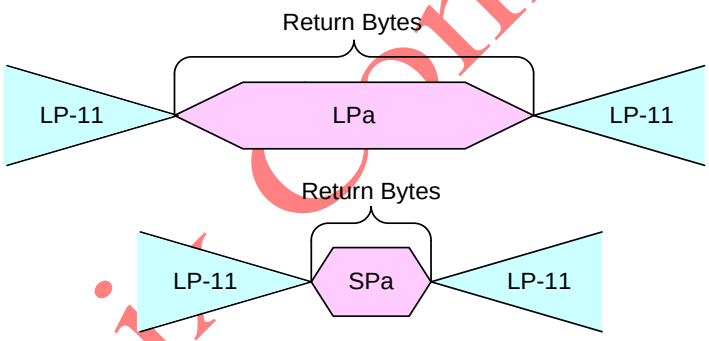
The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report.

The used packet type is defined on Data Type (DT).

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

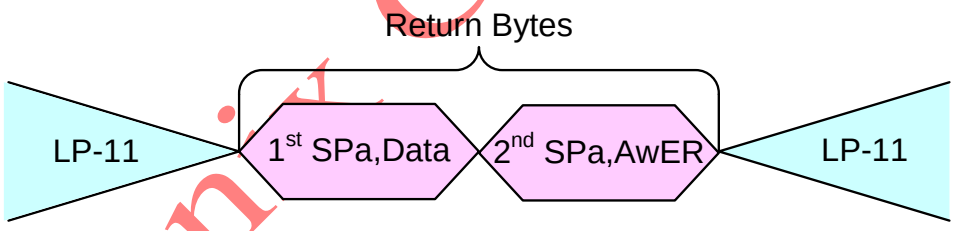
Return Bytes on Signal Packet



From the Display Module (or Other Devices) to the MCU									
Data Type Hex	**B 5**	**B 4**	**B 3**	**B 2**	**B 1**	**B 0**	**Description**	**Packet**	**Abbreviation**
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

The display module is return 2 packets (1st packet: Data, 2nd packet: Acknowledge with Error Report) to the MCU when the display module has received a read command. These return packets are illustrated for reference purpose below.

Exception When Return Bytes on Several Packet



Note:

1. AwER=Acknowledge with Error Report

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’, as they are defined on the following table.

Bit	Description	Sitronix AMOLED Driver Implementation
0	SoT Error	NO
1	SoT Sync Error	NO
2	EoT Sync Error	NO
3	Escape Mode Entry Command Error	YES
4	Low-Power Transmit Sync Error	YES
5	Any Protocol Timer Time-Out	NO
6	False Control Error	YES
7	Contention is Detected on the Display Module	NO
8	ECC Error, single-bit (detected and corrected)	YES
9	ECC Error, multi-bit (detected, not corrected)	YES
10	Set to “0” internally (Only for Long Packet (LP))	YES
11	DSI Data Type (DT) Not Recognized	YES
12	DSI Virtual Channel (VC) ID Invalid	YES
13	Invalid Transmission Length	NO
14	Reserved, Set to ‘0’ internally	NO
15	DSI Protocol Violation	NO

Note

AwER will return1-bit zero if the item is no implementation.

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD):

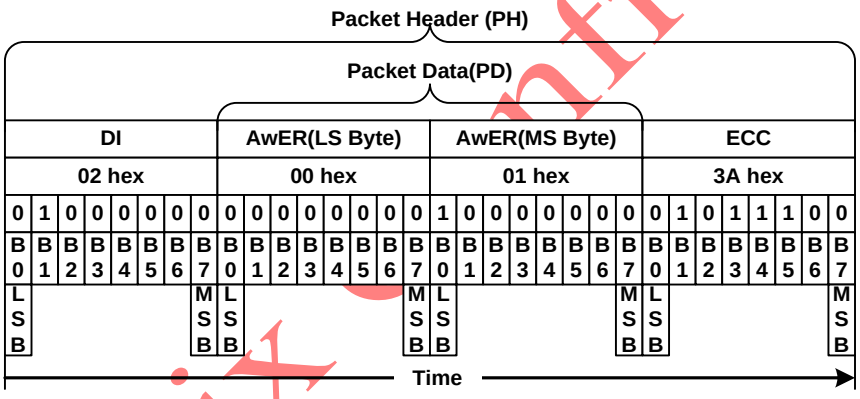
Bit 8: ECC Error, single-bit (detected and corrected)

AwER: 0100h

• Error Correction Code (ECC)

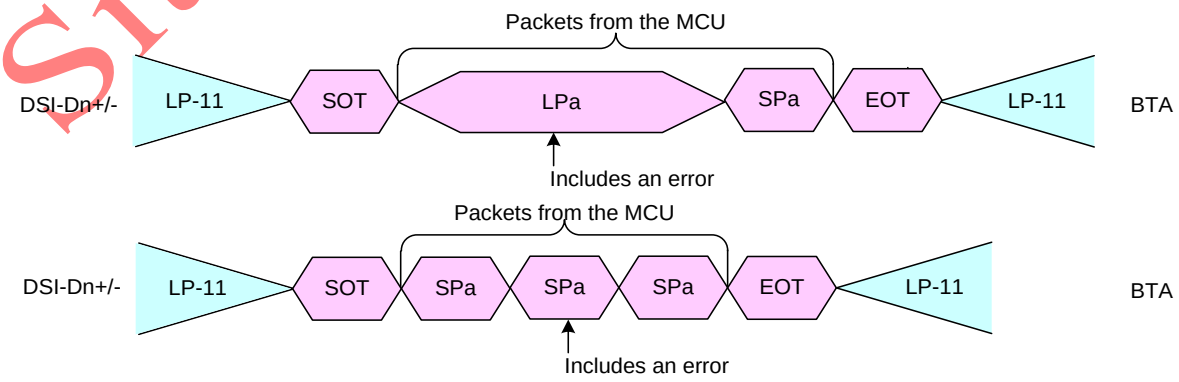
This is defined on the Short Packet (SPa) as follows.

Acknowledge with Error Report (AwER)-Example



It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.

Error Packet



Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Number of the Errors on DSI (05h)" command.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h after the MCU has read the RDNUMED register from the display module.

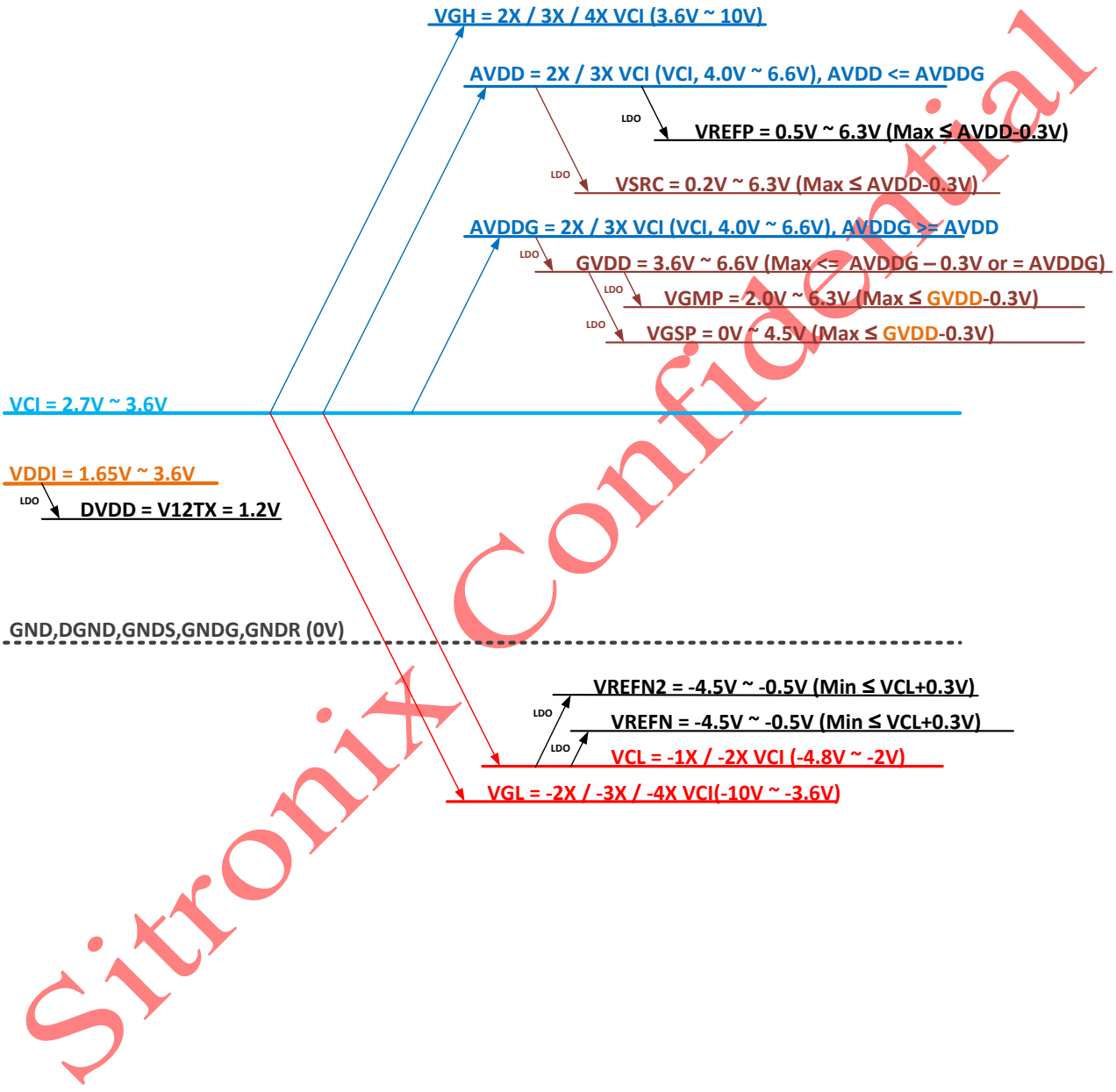
9 POWER GENERATION

9.1 Voltage Generation

Two external power:

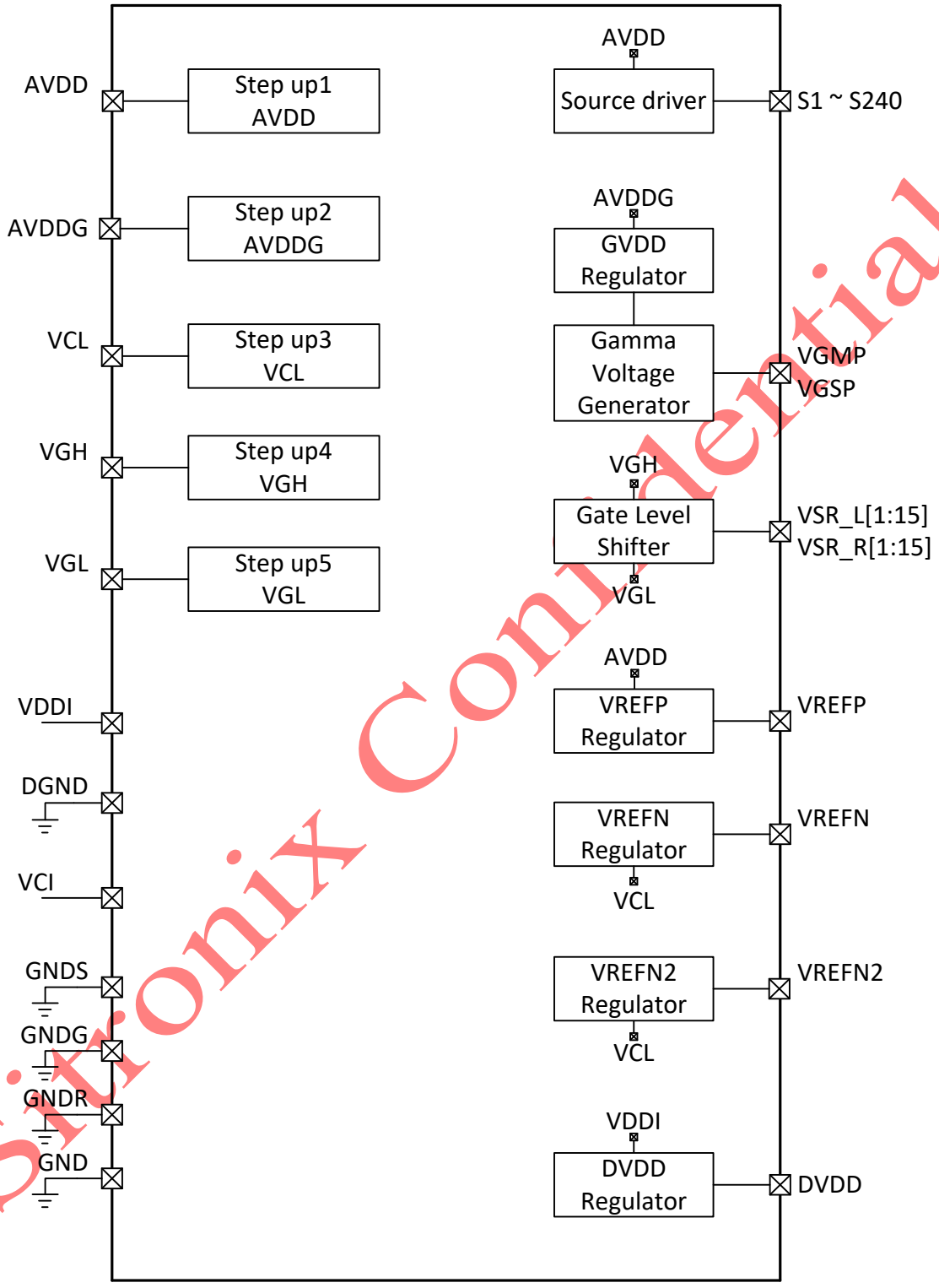
VDDIO = 1.65V ~ 3.6V

VCI = 2.7V ~ 3.6V



9.2 Application Circuit

No external components



9.3 Power Level Definition

Normal display mode on = NORON

Partial mode on = PTLON

Idle mode off = IDMOFF

Idle mode on = IDMON

Sleep out = SLPOUT

Sleep in = SLPIN

Deep standby mode = DSTBON

Definition example:

Seven level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory works with VDDIO power supply. Contents of the memory are safe.

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.

7. Deep Sleep In Mode.

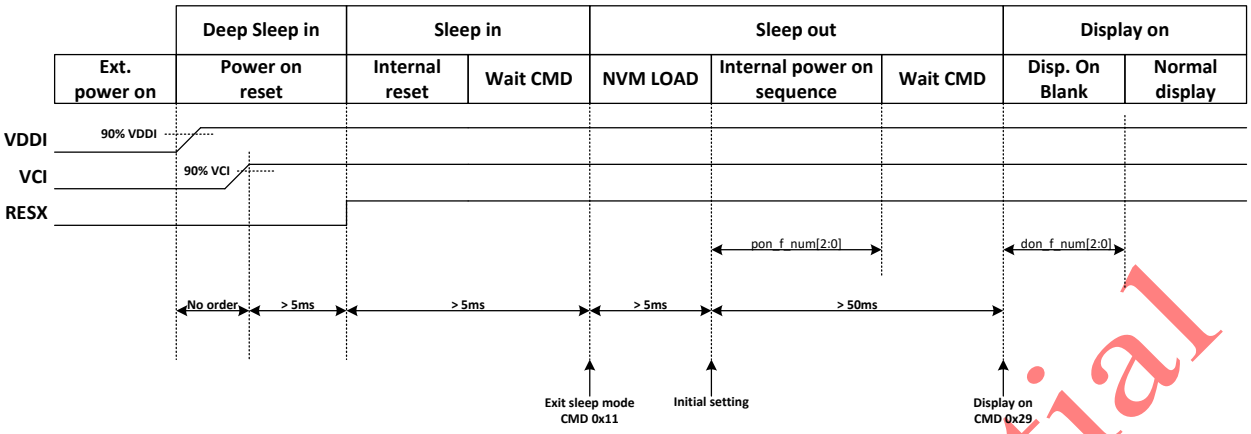
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.

8. Power Off Mode

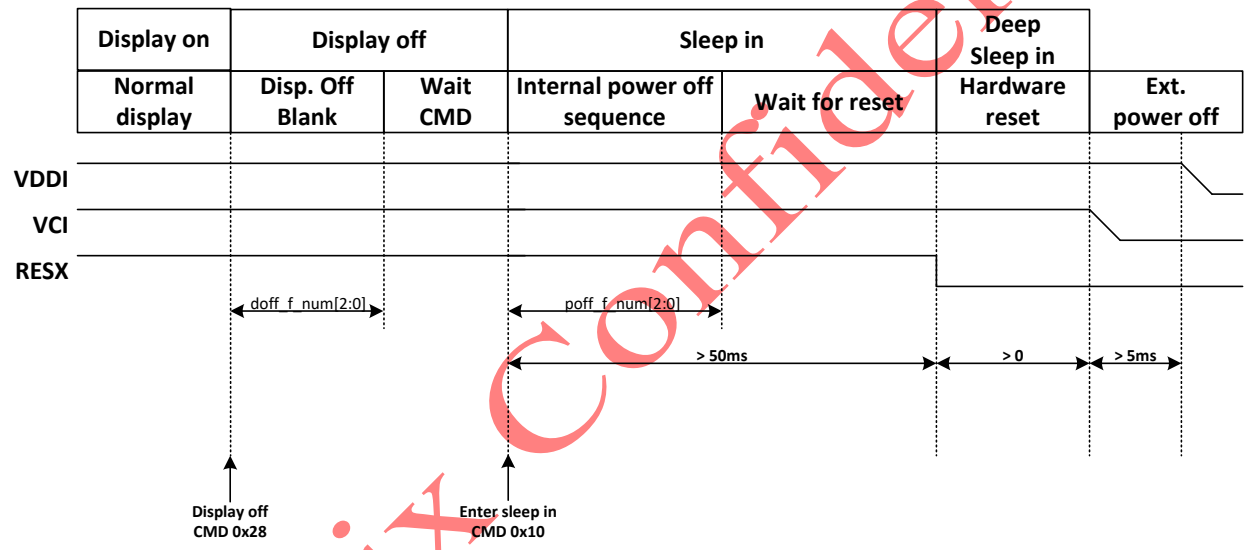
In this mode, VDDIO and VCI are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

9.4 Power on Sequence

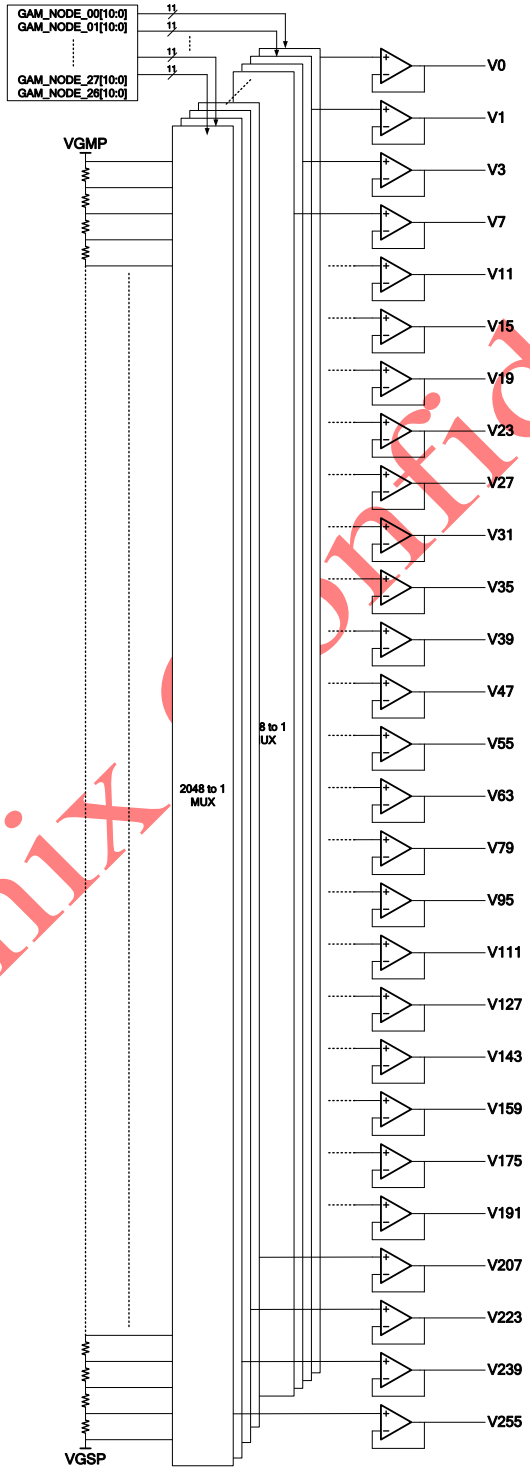


9.5 Power off Sequence



10 GAMMA CORRECTION

ST7802 incorporates the gamma correction function to display 16,777,216 colors for the LTPS AMOLED panel. There are five sets of gamma correction, with three for normal mode, one for idle mode and the last one for HBM. The user also can use the same gamma correction set for different mode. The gamma correction set1 is performed with the following registers.



11 COMMAND

11.1 User Command Set (UCS) List

Command		W/R/C	Function	D7	D6	D5	D4	D3	D2	D1	D0
Add.	Para.										
00h	-	C	No operation	0	0	0	0	0	0	0	0
01h	-	C	Software reset	0	0	0	0	0	0	0	1
04h	1st	R	Read display identification information	ID1[7:0]							
	2nd			ID2[7:0]							
	3rd			ID3[7:0]							
	4th			ID41[7:0]							
	5th			ID42[7:0]							
05h	1st	R	Read Number of Errors on DSI	ERR_OVER_FL	PARITY_ERR_CNT[6:0]						
09h	1st	R	Read display status	MY	MX	MV	0	BGR	0	RSMX	RSMY
	2nd			BSTON	IDMON	PTLON	SLPON	NORON	DISON	0	0
	3rd			0	0	INVON	ALLON	ALLOFF	0	0	0
	4th			TEON	TELOM	0	0	0	0	0	ERR_ON_DSI
0Ah	OKO	R	Read display power mode	BSTON	IDMON	PTLON	SLPON	NORON	DISON	0	0
0Bh	1st	R	Read display MADCTR	MY	MX	MV	0	BGR	0	RSMX	RSMY
0Ch	1st	R	Read display pixel format	SPI_IF_SEL	VIPF[2:0]			0	IFPF[2:0]		
0Dh	1st	R	Read display image mode	0	0	INVON	ALLON	ALLOF	0	0	0
0Eh	1st	R	Read display signal mode	TEON	TELOM	0	0	0	0	0	ERR_ON_DSI
0Fh	1st	R	Read display self-diagnostic result	0	0	0	PCD	0	0	0	CHK_SUM_COMP
10h	-	C	Sleep in	0	0	0	1	0	0	0	0
11h	-	C	Sleep out	0	0	0	1	0	0	0	1
12h	-	C	Partial display mode on	0	0	0	1	0	0	1	0
13h	-	C	Normal display mode on	0	0	0	1	0	0	1	1
20h	-	C	Display inversion off	0	0	1	0	0	0	0	0
21h	-	C	Display inversion on	0	0	1	0	0	0	0	1
22h	-	C	All pixel off	0	0	1	0	0	0	1	0
23h	-	C	All pixel on	0	0	1	0	0	0	1	1
28h	-	C	Display off	0	0	1	0	1	0	0	0
29h	-	C	Display on	0	0	1	0	1	0	0	1
2Ah	1st	W/R	Set column start address	0	0	0	0	0	0	XS[9:8]	
	2nd			XS[7:0]							
	3rd			0	0	0	0	0	0	XE[9:8]	
	4th			XE[7:0]							
2Bh	1st	W/R	Set row start address	0	0	0	0	0	0	YS[9:8]	
	2nd			YS[7:0]							
	3rd			0	0	0	0	0	0	YE[9:8]	
	4th			YE[7:0]							

2Ch	-	C	Memory write	0	0	1	0	1	1	0	0
30h	1st	W/R	Set row partial area	0	0	0	0	0	0	SR[9:8]	
	2nd			SR[7:0]							
	3rd			0	0	0	0	0	0	ER[9:8]	
	4th			ER[7:0]							
31h	1st	W/R	Set column partial area	0	0	0	0	0	0	SC[9:8]	
	2nd			SC[7:0]							
	3rd			0	0	0	0	0	0	EC[9:8]	
	4th			EC[7:0]							
32h	1st	W/R	Horizontal scrolling definition	LFA[15:8]							
	2nd			LFA[7:0]							
	3rd			HSA[15:8]							
	4th			HAS[7:0]							
	5th			RFA[15:8]							
	6th			RFA[7:0]							
33h	1st	W/R	Vertical scrolling definition	TFA[15:8]							
	2nd			TFA[7:0]							
	3rd			VSA[15:8]							
	4th			VSA[7:0]							
	5th			BFA[15:8]							
	6th			BFA[7:0]							
34h	-	C	Tearing effect line off	0	0	1	1	0	1	0	0
35h	1st	W	Tearing effect line on	0	0	0	0	0	0	TE_M	TELOM
36h	1st	W	Scan direction control	MY	MX	MV	RSMY	BGR	0	RSMX	0
37h	1st	W/R	Vertical scrolling start address	VSP[15:8]							
	2nd			VSP[7:0]							
38h	-	C	Idle mode off	0	0	1	1	1	0	0	0
39h	-	C	Enter Idle mode	0	0	1	1	1	0	0	1
3Ah	1st	W	Interface pixel format	SPI_IF_SEL	VIPF[2:0]			0	IFPF[2:0]		
3Bh	1st	W/R	Horizontal scrolling start address	HSP[15:8]							
	2nd			HSP[7:0]							
3Ch	-	C	Memory continuous write	0	0	1	1	1	1	0	0
3Fh	1st	W/R	Gap scrolling definition	SCGAPEN	SCGAP[6:0]						
	2nd			SCGAP_R[7:0]							
	3rd			SCGAP_G[7:0]							
	4th			SCGAP_B[7:0]							
42h	1st	W	SPI read enable	0	0	0	0	0	0	SPI_RD_CAP[1:0]	

44h	1st	W/R	Set tear scanline	0	0	0	0	0	0	STS[9:8]			
	2nd			STS[7:0]									
45h	1st	R	Get tear scanline	0	0	0	0	0	0	GTS[9:8]			
	2nd			GTS[7:0]									
47h	1st	W/R	PCD	0	0	0	0	0	0	0	PCD_EN		
4Ch	-	C	Clean RAM	0	1	0	0	1	1	0	0		
4Dh	1st	W/R	Clean RAM option	CLNRAM_R[7:0]									
	2nd			CLNRAM_G[7:0]									
	3rd			CLNRAM_B[7:0]									
4Fh	1st	W	Deep standby mode on	0	0	0	0	0	0	0	DSTB		
51h	1st	W	Write display brightness	DBV[7:0]									
52h	1st	R	Read display brightness	DBV[7:0]									
53h	1st	W	Write display control	0	0	BCTRL	0	DD	0	0	0		
54h	1st	R	Read display control	0	0	BCTRL	0	DD	0	0	0		
55h	1st	W	Write ACL Control	0	0	0	0	0	0	ACL_EN[1:0]			
56h	1st	R	Read ACL Control	0	0	0	0	0	0	ACL_EN[1:0]			
58h	1st	W	Set color enhance	0	0	0	0	0	SLR_EN	SLR_LEVEL[1:0]			
59h	1st	R	Read color enhance	0	0	0	0	0	SLR_EN	SLR_LEVEL[1:0]			
5Ah	1st	W	Write OPS enable	0	0	0	OPS2_EN	0	OPS_SEL	0	OPS_EN		
5Bh	1st	R	Read OPS enable	0	0	0	OPS2_EN	0	OPS_SEL	0	OPS_EN		
5Ch	1st	W	Write HBM display brightness	DBV_HBM[7:0]									
5Dh	1st	R	Read HBM display brightness	DBV_HBM[7:0]									
5Eh	1st	W	HBM enable	0	0	0	0	0	0	0	HBM_EN		
5Fh	1st	W	Deep idle enable	0	0	0	0	0	0	0	DP_IDLE_EN		
A1h	1st	R	Read DDB	SID[7:0]									
	2nd			SID[15:8]									
	3rd			MID[7:0]									
	4th			MID[15:8]									
	5th			1	1	1	1	1	1	1	1		
A8h	1st	R	Read DDB continuous	SID[7:0]									
	2nd			SID[15:8]									
	3rd			MID[7:0]									
	4th			MID[15:8]									
	5th			1	1	1	1	1	1	1	1		
AAh	1st	R	Read first checksum	FCS[7:0]									
AFh	1st	R	Read continue checksum	CCS[7:0]									
DAh	1st	R	Read display identification information 1	ID1[7:0]									

DBh	1st	R	Read display identification information 2	ID2[7:0]
DCh	1st	R	Read display identification information 3	ID3[7:0]
DDh	1st	R	Read display identification information 4	ID41[7:0]
	2nd			ID42[7:0]

11.2 User Command Set (UCS) Description

11.2.1 NOP (00H) : No Operation

00H	NOP (No Operation)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
NOP	C	0	0	0	0	0	0	0	0	(00H)
Parameter	No Parameter									-
Description	- This command is empty command. It does not have effect on the display module.									
Restriction	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.2 SWRESET (01H) : Software Reset

00H	SWRESET (Software Reset)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SWRESET	C	0	0	0	0	0	0	0	1	(01H)
Parameter	No Parameter									-
Description	- This command is empty command. It does not have effect on the display module.									
Restriction	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.3 RDDID (04H) : Read Display Identification Information

04H	RDDID (Read Display Identification Information)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDID	C	0	0	0	0	0	1	0	0	(04H)
1st Parameter	R	ID1[7:0]								00H
2nd Parameter	R	ID2[7:0]								00H
3rd Parameter	R	ID3[7:0]								00H
4th Parameter	R	ID41[7:0]								00H
5th Parameter	R	ID42[7:0]								00H

Description

- Read Display Identification Information

-ID1[7:0]: AMOLED module's manufacturer ID (00H: not programmed)

-ID2[7:0]: AMOLED module/driver version ID (00H: not programmed)

-ID3[7:0]: AMOLED module/driver ID (00H: not programmed)

-ID41[7:0]: AMOLED module/driver ID (00H: not programmed)

-ID42[7:0]: AMOLED module/driver ID (00H: not programmed)

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.4 RDNUMED (05H) : Read Number of Errors on DSI

05H	RDNUMED (Read Number of Errors on DSI)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDNUMED	C	0	0	0	0	0	1	0	1	(05H)
1st Parameter	R	ERR_OVER_FL	PARITY_ERR_CNT[6:0]							00H
Description	- PARITY_ERR_CNT[6:0]: Number of the parity errors. - ERR_OVER_FL: '1' = If there is overflow with PARITY_ERR_CNT [6..0] bits.									
Restriction	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.5 RDDST (09H) : Read Display Status

09H	RDDST (Read Display Status)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDST	C	0	0	0	0	1	0	0	1	(09H)
1st Parameter	R	MY	MX	MV	0	BGR	0	RSMX	RSMY	00H
2nd Parameter	R	BSTON	IDMON	PTLON	SLPON	NORON	DISON	0	0	08H
3rd Parameter	R	0	0	INVON	ALLON	ALLOFF	0	0	0	00H
4th Parameter	R	TEON	TELOM	0	0	0	0	0	ERR_ON_DSI	00H

Description

Bit	Description	Value
MY	Row Address Increment	'1' = Decreasing in vertical '0' = Increasing in vertical
MX	Column Address Increment	'1' = Decreasing in horizontal '0' = Increasing in horizontal
MV	Row/Column Order	'1' = Row/column exchange '0' = Normal
BGR	RGB/ BGR Order	'1' = BGR Order '0' = RGB Order
RSMX	Horizontal Flip	'1' = Flipped display '0' = Normal display
RSMY	Vertical Flip	'1' = Flipped display '0' = Normal display
BSTON	Booster Voltage Status	'1' = Booster On '0' = Booster Off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial Mode On/Off	'1' = Partial Mode On '0' = Partial Mode Off
SLPON	Sleep In/Out Mode	'1' = Sleep Out Mode '0' = Sleep In Mode
NORON	Display Normal Mode On/Off	'1' = Normal Display '0' = Partial Display
DISON	Display On/Off	'1' = Display On '0' = Display Off,
INVON	Inversion On/Off	'1' = Inversion is On '0' = Inversion is Off
ALLON	All Pixel On	'1' = White display '0' = Normal display
ALLOFF	All Pixel Off	'1' = Black display '0' = Normal display

Bit	Description	Value

	TEON: Tearing Effect Line On/Off — '1' = TE on; '0' = TE off TELOM: Tearing Effect Line Mode — '1' = mode 2; '0' = mode 1 ERR_ON_DSI: Error on DSI — '1' = Error; '0' = No Error
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.6 RDDPM (0AH) : Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDPM	C	0	0	0	0	1	1	0	0	(0AH)
1st Parameter	R	BSTON	IDMON	PTLON	SLPON	NORON	DISON	0	0	08H

Description

Bit	Description	Value
BSTON	Booster Voltage Status	'1' = Booster On '0' = Booster Off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial Mode On/Off	'1' = Partial Mode On '0' = Partial Mode Off
SLPON	Sleep In/Out Mode	'1' = Sleep Out Mode '0' = Sleep In Mode
NORON	Display Normal Mode On/Off	'1' = Normal Display '0' = Partial Display
DISON	Display On/Off	'1' = Display On '0' = Display Off,

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.7 RDDMADCTR (0BH) : Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDMADCTR	C	0	0	0	0	1	0	1	1	(0BH)
1st Parameter	R	MY	MX	MV	0	BGR	0	RSMX	RSMY	00H

Description

Bit	Description	Value
MY	Row Address Increment	'1' = Decreasing in vertical '0' = Increasing in vertical
MX	Column Address Increment	'1' = Decreasing in horizontal '0' = Increasing in horizontal
MV	Row/Column Order	'1' = Row/column exchange '0' = Normal
BGR	RGB/ BGR Order	'1' = BGR Order '0' = RGB Order
RSMX	Horizontal Flip	'1' = Flipped display '0' = Normal display
RSMY	Vertical Flip	'1' = Flipped display '0' = Normal display

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.8 RDDCOLMOD (0CH) : Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDCOLMOD	C	0	0	0	0	1	1	0	0	(0CH)
1st Parameter	R	SPI_IF_SEL	VIPF[2:0]			0	IFPF[2:0]			77H

Description

Pixel format for the RGB image data used by the interface.

SPI_IFPF_SEL: '1' = VIPF[2:0] pixel format used by SPI interface

'0' = IFPF[2:0] pixel format used by SPI/MCU/MIPI interface

VIPF[2:0]/IFPF[2:0] Control Interface Color Format:

'001' = SPI 8bit/pixel(256colors), SPI256Gray

'010' = SPI 8bit/pixel(256colors), SPI332

'011' = SPI 3bit/pixel(8colors), SPI111

'101' = 16bit/pixel

'110' = 18bit/pixel

'111' = 24bit/pixel"

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.9 RDDIM (0DH) : Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDIM	C	0	0	0	0	1	1	0	1	(0DH)
1st Parameter	R	0	0	INVON	ALLON	ALLOFF	0	0	0	00H

Description

Bit	Description	Value
INVON	Inversion On/Off	'1' = Inversion is On '0' = Inversion is Off
ALLON	All Pixel On	'1' = White display '0' = Normal display
ALLOFF	All Pixel Off	'1' = Black display '0' = Normal display

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.10 RDDSM (0EH) : Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDSM	C	0	0	0	0	1	1	1	0	(0EH)
1st Parameter	R	TEON	TELOM	0	0	0	0	0	ERR_ON_DSI	00H

Description

Bit	Description	Value
TEON	Tearing Effect Line On/Off	'1' = TE on '0' = TE off
TELOM	Tearing Effect Line Mode	'1' = mode 2 '0' = mode 1
ERR_ON_DSI	Error on DSI	'1' = Error '0' = No Error

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

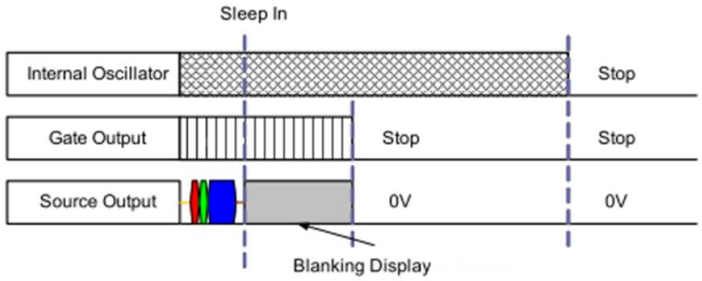
11.2.11 RDDSDR (0FH) : Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDSDR	C	0	0	0	0	1	1	1	1	(0FH)
1st Parameter	R	0	0	0	PCD	0	0	0	CHK_SUM_COMP	00H
Description	PCD: Read panel crack detection result, 0: not crack, 1: crack CHK_SUM_COMP: checksum comparison from UCS, 0: FCS and CCS are same, 1: FCS and CCS are not same									
Restriction	-									

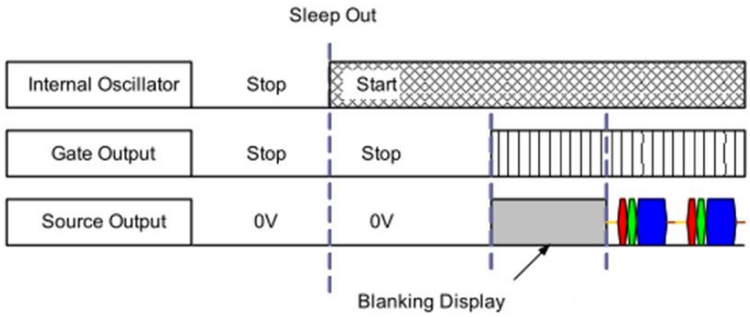
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.12 SLPIN (10H) : Sleep In

10H	SLPIN (Sleep In)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SLPIN	C	0	0	0	1	0	0	0	0	(10H)
Parameter	No Parameter									-
Description	- This command causes the AMOLED module to enter the minimum power consumption mode. - In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. 									
Restriction	This command has no effect when the display module is already in Sleep mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It must wait 5msec before sending next command for the supply voltages and clock circuits to stabilize. It must wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.									
Register Availability	**Status** / **Availability** Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes									

11.2.13 SLPOUT (11H) : Sleep Out

11H	SLPOUT (Sleep Out)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SLPOUT	C	0	0	0	1	0	0	0	1	(11H)
Parameter	No Parameter									-
Description	- This command turns off sleep mode. - In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. 									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H). It will be necessary to wait 5ms before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode. It will be necessary to wait 120ms after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.14 PTLON (12H) : Partial Display Mode On

12H	PTLON (Partial Display Mode On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
PTLON	C	0	0	0	1	0	0	1	0	(12H)
Parameter	No Parameter									-
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command. To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written.									
Restriction	This command has no effect when Partial Display Mode is already active.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

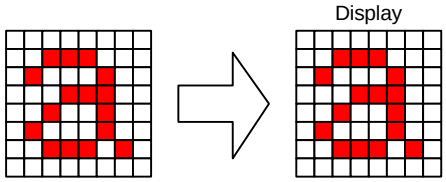
11.2.15 NORON (13H) : Normal Display Mode On

13H	NORON (Normal Display Mode On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
NORON	C	0	0	0	1	0	0	1	1	(13H)
Parameter	No Parameter									-
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h)									
Restriction	This command has no effect when Normal Display mode is active.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

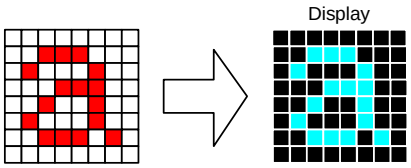
11.2.16 INVOFF (20H) : Display Inversion Off

20H	INVOFF (Display Inversion Off)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
INVOFF	C	0	0	1	0	0	0	0	0	(20H)
Parameter	No Parameter									-
Description	This command is used to recover from display inversion mode. This command does not change any other status. 									
Restriction	This command has no effect when module is already in inversion off mode.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

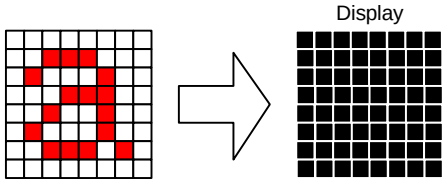
11.2.17 INVON (21H) : Display Inversion On

21H	INVON (Display Inversion On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
INVON	C	0	0	1	0	0	0	0	1	(21H)
Parameter	No Parameter									-
Description	This command is used to enter display inversion mode. This command does not change any other status. 									
Restriction	This command has no effect when module is already in inversion on mode.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

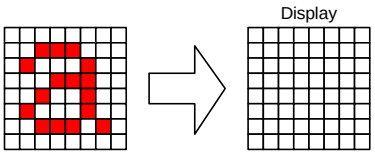
11.2.18 ALLPOFF (22H) : All Pixel Off

22H	ALLPOFF (All Pixel Off)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
ALLPOFF	C	0	0	1	0	0	0	1	0	(22H)
Parameter	No Parameter									-
Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.  "All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the Input Image after "Normal Display On" and "Partial Mode On" commands.									
Restriction	This command has no effect when module is already in all pixel off mode.									

Register Availability

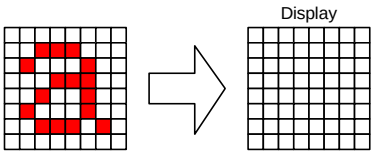
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.19 ALLPON (23H) : All Pixel On

23H	ALLPON (All Pixel On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
ALLPON	C	0	0	1	0	0	0	1	1	(23H)
Parameter	No Parameter									-
Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.  "All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the Input Image after "Normal Display On" and "Partial Mode On" commands.									
Restriction	This command has no effect when module is already in all pixel on mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

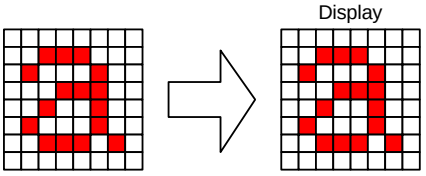
11.2.20 DISPOFF (28H) : Display Off

28H	DISPOFF (Display Off)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
DISPOFF	C	0	0	1	0	1	0	0	0	(28H)
Parameter	No Parameter									-
Description	This command causes the display module to stop displaying the image data on the display device. This command does not change any other status. 									
Restriction	This command has no effect when module is already in display off mode.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.21 DISPON (29H) : Display On

29H	DISPON (Display On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
DISPON	C	0	0	1	0	1	0	0	1	(29H)
Parameter	No Parameter									-
Description	This command causes the display module to start displaying the image data on the display device. This command does not change any other status. 									
Restriction	This command has no effect when module is already in display on mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.22 CASET (2AH) : Set Column Start Address

2AH	CASET (Set Column Start Address)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
CASET	C	0	0	1	0	1	0	1	0	(2AH)
1st Parameter	W/R	0	0	0	0	0	0	XS[9:8]		00H
2nd Parameter	W/R	XS[7:0]								00H
3rd Parameter	W/R	0	0	0	0	0	0	XE[9:8]		01H
4th Parameter	W/R	XE[7:0]								8FH

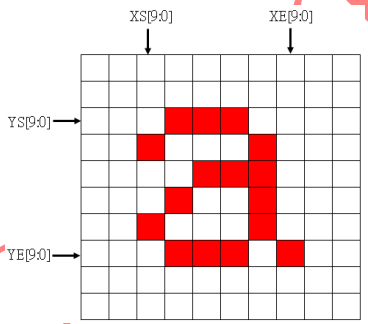
Description

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.

XS[9:0]: Start X address, XE[9:0]: End X Address

(1) XS[9:0] always must be equal to or less than XE[9:0].

(2) The XS[9:0] and XE[9:0]-XS[9:0]+1 must can be divisible by 2.



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.23 RASET (2BH) : Set Row Start Address

2BH	RASET (Set Row Start Address)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RASET	C	0	0	1	0	1	0	1	1	(2BH)
1st Parameter	W/R	0	0	0	0	0	0	YS[9:8]		00H
2nd Parameter	W/R	YS[7:0]								00H
3rd Parameter	W/R	0	0	0	0	0	0	YE[9:8]		01H
4th Parameter	W/R	YE[7:0]								8FH

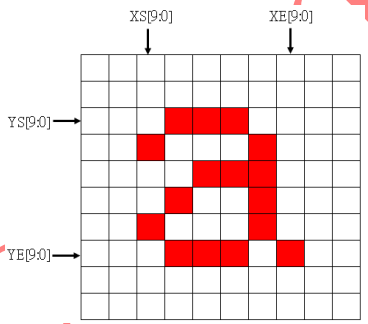
Description

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.

YS[9:0]: Start Y address, YE[9:0]: End Y Address

(1) YS[9:0] always must be equal to or less than YE[9:0].

(2) The YS[9:0] and YE[9:0]-YS[9:0]+1 must can be divisible by 2.



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.24 RAMWR (2CH) : Memory Write

2CH	RAMWR (Memory Write)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RAMWR	C	0	0	1	0	1	1	0	0	(2CH)
1st Parameter	W	D_17	D_16	D_15	D_14	D_13	D_13	D_11	D_10	-
2nd Parameter	W	D_27	D_26	D_25	D_24	D_23	D_23	D_21	D_20	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	-
Nth Parameter	W	D_N7	D_N6	D_N5	D_N4	D_N3	D_N3	D_N1	D_N0	-

Description

This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.

The column and page registers are reset to the Start X Address (XS) and Start Y Address (YS), respectively.
Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End X Address (XE) value. The column register is then reset to XS and the Y address register is incremented.
Pixels are written to the frame memory until the Y address register equals the End Y address (YE) value or the host processor sends another command.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.25 PTLAR1 (30H) : Partial Area

30H	PTLAR1 (Partial Area)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
PTLAR1	C	0	0	1	1	0	0	0	0	(30H)
1st Parameter	W/R	0	0	0	0	0	0	SR[9:8]		00H
2nd Parameter	W/R	SR[7:0]								00H
3rd Parameter	W/R	0	0	0	0	0	0	ER[9:8]		01H
4th Parameter	W/R	ER[7:0]								8FH

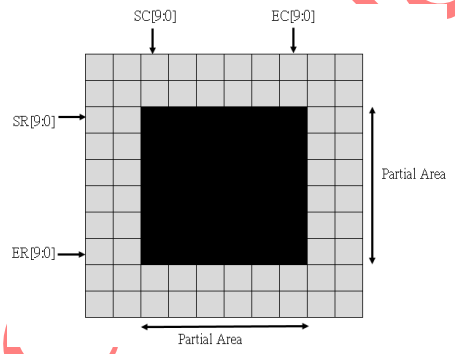
Description

SR[9:0]: Start Row, ER[9:0]: End Row

(1) SR[9:0] and ER[9:0] settings should be within max available Display Area.

(2) The SR[9:0] and (ER[9:0]-SR[9:0]+1) must can be divisible by 2.

Range = 0~399



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.26 PTLAR2 (31H) : Partial Area

31H	PTLAR2 (Partial Area)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
PTLAR2	C	0	0	1	1	0	0	0	1	(31H)
1st Parameter	W/R	0	0	0	0	0	0	SC[9:8]		00H
2nd Parameter	W/R	SC[7:0]								00H
3rd Parameter	W/R	0	0	0	0	0	0	EC[9:8]		01H
4th Parameter	W/R	EC[7:0]								8FH

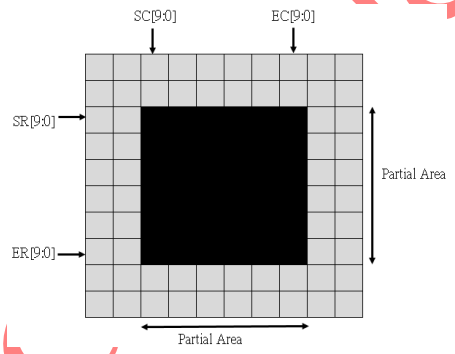
Description

SC[9:0]: Start Column, EC[9:0]: End Column

(1) SC[9:0] always must be equal to or less than EC[9:0].

(2) The SC[9:0] and (EC[9:0]-SC[9:0]+1) must can be divisible by 2.

Range = 0~399



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.27 HSCRDEF (32H) : Horizontal Scrolling Definition

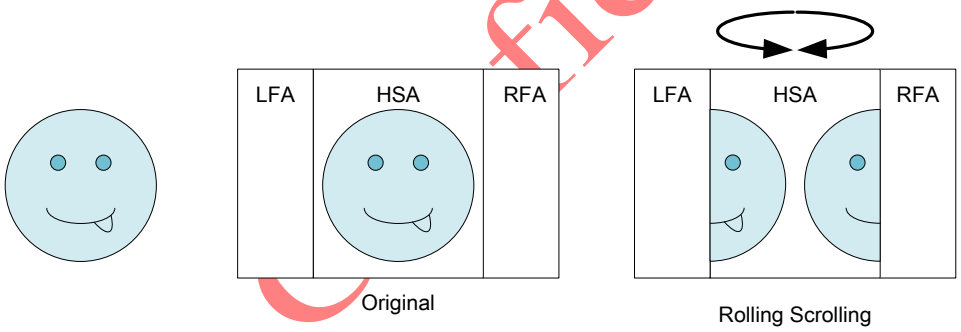
32H	HSCRDEF (Horizontal Scrolling Definition)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
HSCRDEF	C	0	0	1	1	0	0	1	0	(32H)
1st Parameter	W/R	LFA[15:8]								00H
2nd Parameter	W/R	LFA[7:0]								00H
3rd Parameter	W/R	HSA[15:8]								00H
4th Parameter	W/R	HSA[7:0]								00H
5th Parameter	W/R	RFA[15:8]								00H
6th Parameter	W/R	RFA[7:0]								00H

Description

LFA[15:0]: Describe the Left Fixed Area

HSA[15:0]: Describes the width of the Horizontal Scrolling Area

RFA[15:0]: Describes the Right Fixed Area



Restriction

must can be divisible by 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.28 VSCRDEF (33H) : Vertical Scrolling Definition

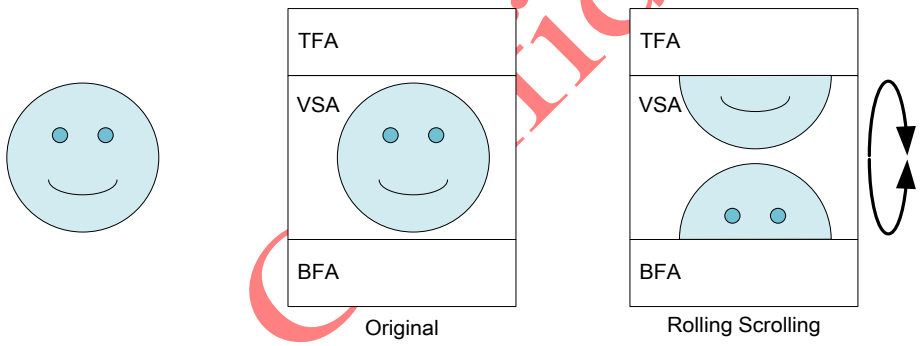
33H	VSCRDEF (Vertical Scrolling Definition)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
VSCRDEF	C	0	0	1	1	0	0	1	1	(33H)
1st Parameter	W/R	TFA[15:8]								00H
2nd Parameter	W/R	TFA[7:0]								00H
3rd Parameter	W/R	VSA[15:8]								00H
4th Parameter	W/R	VSA[7:0]								00H
5th Parameter	W/R	BFA[15:8]								00H
6th Parameter	W/R	BFA[7:0]								00H

Description

TFA[15:0]: Describe the Top Fixed Area

VSA[15:0]: Describes the height of the Vertical Scrolling Area

BFA[15:0]: Describes the Bottom Fixed Area



Restriction

must can be divisible by 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.29 TEOF (34H) : Tearing Effect Line Off

34H	TEOF (Tearing Effect Line Off)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
TEOF	C	0	0	1	1	0	1	0	0	(34H)
Parameter	No Parameter									-
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.									
Restriction	This command has no effect when the Tearing Effect output is already off.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.30 TEON (35H) : Tearing Effect Line On

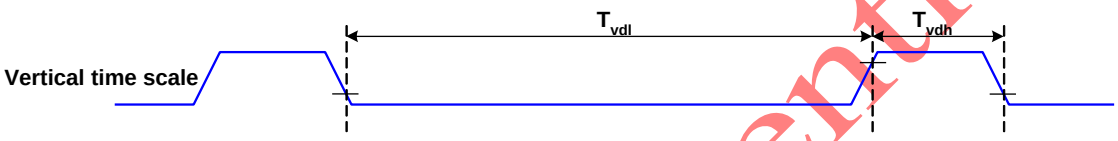
35H	TEON (Tearing Effect Line On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
TEON	C	0	0	1	1	0	1	0	1	(35H)
1st Parameter	W	0	0	0	0	0	0	TE_M	TELOM	00H

Description

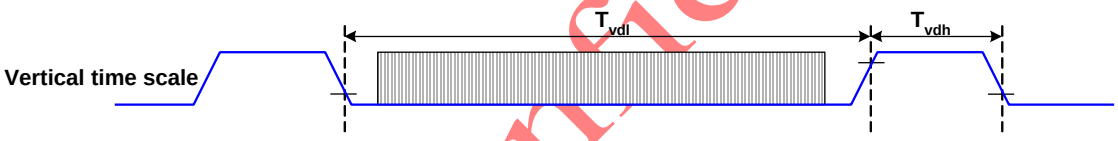
TE_M: Output mode of TE signal set

TELOM: Output mode of TE signal, 0:only V-blanking, 1:V-blanking +H-blanking

When TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only:



When TELOM = 1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During the Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when the Tearing Effect output is already on.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.31 MADCTR (36H) : Scan Direction Control

36H	MADCTR (Scan Direction Control)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
MADCTR	C	0	0	1	1	0	1	1	0	(36H)
1st Parameter	W	MY	MX	MV	RSMY	BGR	0	RSMX	0	00H

Description

Bit	Description	Value
MY	Row Address Increment	'1' = Decreasing in vertical '0' = Increasing in vertical
MX	Column Address Increment	'1' = Decreasing in horizontal '0' = Increasing in horizontal
MV	Row/Column Order	Only support circle or square panel, row pixel = column pixel '1' = Row/column exchange '0' = Normal
BGR	RGB/ BGR Order	'1' = BGR Order '0' = RGB Order
RSMX	Horizontal Flip	'1' = Flipped display '0' = Normal display
RSMY	Vertical Flip	'1' = Flipped display '0' = Normal display

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

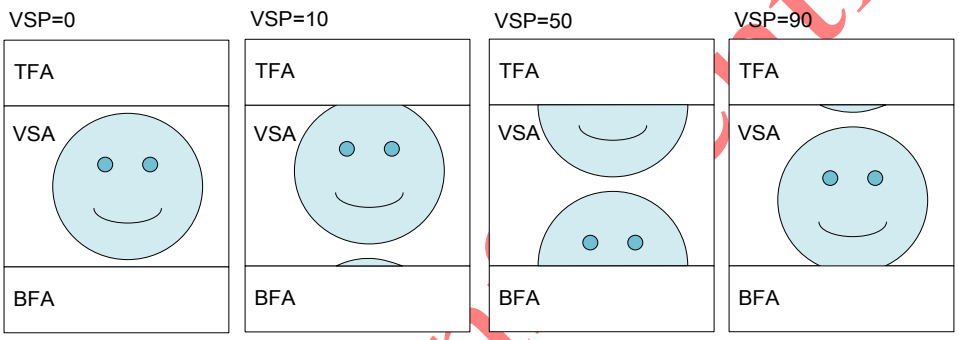
11.2.32 VSCRSADD (37H) : Vertical Scrolling Start Address

37H	VSCRSADD (Vertical Scrolling Start Address)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
VSCRSADD	C	0	0	1	1	0	1	1	1	(37H)
1st Parameter	W/R	VSP[15:8]								00H
2nd Parameter	W/R	VSP[7:0]								00H

Description

VSP[15:0]: Vertical Scrolling Point used with Vertical Scrolling Definition(33h). These two commands describe the scrolling area and the scrolling mode.

Ex: TFA=40, BFA=40, VSA=100



Restriction

must can be divisible by 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

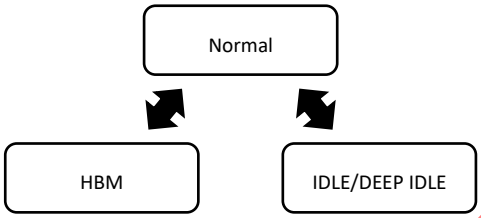
11.2.33 IDMOFF (38H) : Idle Mode Off

38H	IDMOFF (Idle Mode Off)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
IDMOFF	C	0	0	1	1	1	0	0	0	(38H)
Parameter	No Parameter									-
Description	This command causes the display module to enter normal mode(exit HBM, idle and deep idle)									
Restriction	This command has no effect when module is already in normal mode.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.34 IDMON (39H) : Idle Mode On

39H	IDMON (Idle Mode On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
IDMON	C	0	0	1	1	1	0	0	1	(39H)
Parameter	No Parameter									-
Description	This command causes the display module to enter idle mode(exit HBM, normal and deep idle) 									
Restriction	This command has no effect when module is already in idle mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.35 COLMOD (3AH) : Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
COLMOD	C	0	0	1	1	1	0	1	0	(3AH)
1st Parameter	W	SPI_IF_SEL	VIPF[2:0]			0	IFPF[2:0]			77H

Description

This command sets the pixel format for the RGB image data used by the interface.

SPI_IF_SEL: 1: VIPF[2:0] pixel format used by SPI interface

0: IFPF[2:0] pixel format used by SPI/MIPI interface

VIPF[2:0] : SPI interface format in ST7802 when SPI_IFPF_SEL = 1

IFPF[2:0] : MIPI and SPI interface pixel format when SPI_IFPF_SEL = 0

IFPF[2:0]	Value
3'b001	SPI 8bit/pixel, 256 gray colors
3'b010	SPI 8bit/pixel, RGB 3-3-2-bit
3'b011	SPI 3bit/pixel, RGB 1-1-1-bit
3'b101	16bit/pixel, RGB 5-6-5-bit
3'b110	18bit/pixel, RGB 6-6-6-bit
3'b111	24bit/pixel, RGB 8-8-8-bit

Restriction

Register Availability

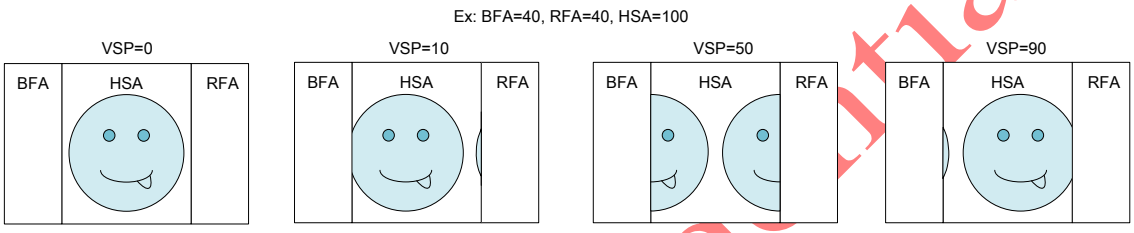
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.36 HSCRSADD (3BH) : Horizontal Scrolling Start Address

3BH	HSCRSADD (Horizontal Scrolling Start Address)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
HSCRSADD	C	0	0	1	1	1	0	1	1	(3BH)
1st Parameter	W/R	HSP[15:8]								00H
2nd Parameter	W/R	HSP[7:0]								00H

Description

HSP[15:0]: Horizontal Scrolling Point used with Horizontal Scrolling Definition(32h). These two commands describe the scrolling area and the scrolling mode.



Restriction

must can be divisible by 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.37 RAMWRC (3CH) : Memory Continuous Write

3CH	RAMWRC (Memory Continuous Write)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RAMWRC	C	0	0	1	1	1	1	0	0	(3CH)
1st Parameter	W	D_17	D_16	D_15	D_14	D_13	D_13	D_11	D_10	-
2nd Parameter	W	D_27	D_26	D_25	D_24	D_23	D_23	D_21	D_20	-
:	:	:	:	:	:	:	:	:	:	-
Nth Parameter	W	D_N7	D_N6	D_N5	D_N4	D_N3	D_N3	D_N1	D_N0	-

Description

This command sets the pixel format for the RGB image data used by the interface.

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

Data is written continuing from the pixel location after the write range of the previous RAMWR (2Ch) or RAMWRC (3Ch). The X Address register is then incremented and pixels are written to the frame memory until the X Address register equals the End X Address (EX) value.

The X Address register is then reset to Start X Address (SX) and the Y Address register is incremented.

Pixels are written to the frame memory until the page register equals the End Y Address (EY) value or the host processor sends another command.

Restriction

A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.38 SCGAPDEF (3FH) : Scrolling Gap Definition

3BH	SCGAPDEF (Scrolling Gap Definition)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SCGAPDEF	C	0	0	1	1	1	1	1	1	(3FH)
1st Parameter	W/R	SCGAPEN	SCGAP[6:0]							00H
2nd Parameter	W/R	SCGAP_R[7:0]								00H
3rd Parameter	W./R	SCGAP_G[7:0]								00H
4th Parameter	W/R	SCGAP_B[7:0]								00H

Description	SCGAPEN: 1: Enable Scrolling Gap Function, 0: Disable SCGAP[6:0]: Scroll Gap Line SCGAP_R[7:0]: Scroll Gap Red Color Definition SCGAP_G[7:0]: Scroll Gap Green Color Definition SCGAP_B[7:0]: Scroll Gap Blue Color Definition
Restriction	

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.39 SPI_RD_EN (42H) : SPI Read Enable

42H	SPI_RD_EN (SPI Read Enable)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SPI_RD_EN	C	0	1	0	0	0	0	1	0	(42H)
1st Parameter	W/R							SPI_RD_CAP[1:0]		00H
Description	SPI_RD_CAP[1:0]: Read/Write CMD read protection in 3-wire SPI or 4-wire SPI. 1: Read mode enable Other: Read mode disable									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.40 STESL (44H) : Set Tear Scanline

44H	STESL (Set Tear Scanline)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
STESL	C	0	1	0	0	0	1	0	0	(44H)
1st parameter	W/R	0	0	0	0	0	0	STS[9:8]		00H
2nd parameter	W/R	STS[7:0]								00H
Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.41 GSL (45H) : Get Scanline

45H	GSL (Get Scanline)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
GSL	C	0	1	0	0	0	1	0	1	(45H)
1st parameter	R	0	0	0	0	0	0	GTS[9:8]		-
2nd parameter	R	GTS[7:0]								-
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.42 PCD (47H) : Panel Crack Detection

47H	PCD (Panel Crack Detection)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
PCD	C	0	1	0	0	0	1	1	1	(47H)
1st parameter	W/R	0	0	0	0	0	0	0	PCD_EN	00H
Description	PCD_EN: 1: Panel Crack Detection enable, 0: Disable									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.43 DSTBON (4FH) : Deep Standby Mode On

4FH	DSTBON (Deep Standby Mode On)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
DSTBON	C	0	1	0	0	1	1	1	1	(4FH)
1st parameter	W	0	0	0	0	0	0	0	DSTB	00H

Description

This command is used to enter deep standby mode.

DSTB=”1”, enter deep standby mode.

Notes:

1. To exit Deep Standby Mode, input low pulse more than 3 ms to pin RESX.
2. For MIPI IF, if deep standby mode is used, please pull HSSI_CLK_P/N & HSSI_D0~D1_P/N to GND after executing deep standby command.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.44 WRDISBV (51H) : Write Display Brightness

51H	WRDISBV (Write Display Brightness)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
WRDISBV	C	0	1	0	1	0	0	0	1	(51H)
1st parameter	W	DBV[7:0]								FFH
Description	This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.45 RDDISBV (52H) : Read Display Brightness

52H	RDDISBV (Read Display Brightness)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDISBV	C	0	1	0	1	0	0	1	0	(52H)
1st parameter	R	DBV[7:0]								FFH
Description	This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.46 WRCTRLD (53H) : Write Display Control

53H	WRCTRLD (Write Display Control)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
WRCTRLD	C	0	1	0	1	0	0	1	1	(53H)
1st parameter	W	0	0	BCTRL	0	DD	0	0	0	00H
Description	BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable									
Restriction	The display supplier cannot use this command for tuning									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.47 RDCTRLD (54H) : Read Display Control

54H	RDCTRLD (Read Display Control)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDCTRLD	C	0	1	0	1	0	1	0	0	(54H)
1st parameter	R	0	0	BCTRL	0	DD	0	0	0	00H
Description	BCTRL: Brightness control ,1=enable DD: Display dimming control ,1=enable									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.48 WRACL (55H) : Write ACL Control

55H	WRACL (Write ACL Control)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
WRACL	C	0	1	0	1	0	1	0	1	(55H)
1st parameter	W	0	0	0	0	0	0	ACL_EN[1:0]		00H
Description	ACL_EN[1:0]: ACL(Active current limit) function enable, 0: Disable, 1: Level1, 2: Level2, 3: Level3									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.49 RDACL (56H) : Read ACL Control

56H	RDACL (Read ACL Control)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDACL	C	0	1	0	1	0	1	1	0	(56H)
1st parameter	R	0	0	0	0	0	0	ACL_EN[1:0]		00H
Description	ACL_EN[1:0]: ACL(Active current limit) function enable, 0: Disable, 1: Level1, 2: Level2, 3: Level3									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.50 SLRWR (58H) : Set color enhance

58H	SLRWR (Set color enhance)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SLRWR	C	0	1	0	1	1	0	0	0	(58H)
1st parameter	W	0	0	0	0	0	SLR_EN	SLR_LEVEL[1:0]		00H
Description	SLR_EN: Sunlight Readable Enhancement Enable, 0: disable, 1: enable SLR_LEVEL[1:0]: Sunlight Readable Enhancement Level, 0~2, low to high									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.51 SLRRD (59H) : Read color enhance

59H	SLRRD (Read color enhance)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
SLRRD	C	0	1	0	1	1	0	0	0	(59H)
1st parameter	R	0	0	0	0	0	SLR_EN	SLR_LEVEL[1:0]		00H
Description	SLR_EN: Sunlight Readable Enhancement Enable, 0: disable, 1: enable SLR_LEVEL[1:0]: Sunlight Readable Enhancement Level, 0~2, low to high									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.52 WROPS (5AH) : Write OPS enable

5AH	WROPS (Write OPS enable)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
WROPS	C	0	1	0	1	1	0	1	0	(5AH)
1st parameter	R	0	0	0	OPS2_EN	0	OPS_SEL	0	OPS_EN	00H
Description	OPS2_EN: OPS function, auto adjust output RGB data weight, 0: disable, 1: enable OPS_EN: OPS function, auto adjust OVSS voltage by SWIREL or SWIRER pulse, 0: disable, 1: enable OPS_SEL: OPS reference select, 0: DBV, 1: RGB data									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.53 RDOPS (5BH) : Read OPS enable

5BH	RDOPS (Read OPS enable)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDOPS	C	0	1	0	1	1	0	1	1	(5BH)
1st parameter	R	0	0	0	OPS2_EN	0	OPS_SEL	0	OPS_EN	00H
Description	OPS2_EN: OPS function, auto adjust output RGB data weight, 0: disable, 1: enable OPS_EN: OPS function, auto adjust OVSS voltage by SWIREL or SWIRER pulse, 0: disable, 1: enable OPS_SEL: OPS reference select, 0: DBV, 1: RGB data									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.54 WRHBMBV (5CH) : Write HBM Display Brightness

5CH	WRHBMBV (Write HBM Display Brightness)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
WRHBMBV	C	0	1	0	1	1	1	0	0	(5CH)
1st parameter	W	DBV_HBM[7:0]								FFH
Description	This command is used to adjust brightness value in HBM mode.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.55 RDHBMBV (5DH) : Read HBM Display Brightness

5DH	RDHBMBV (Read HBM Display Brightness)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDHBMBV	C	0	1	0	1	1	1	0	1	(5DH)
1st parameter	R	DBV_HBM[7:0]								FFH
Description	This command is used to adjust brightness value in HBM mode.									
Restriction										

Register Availability

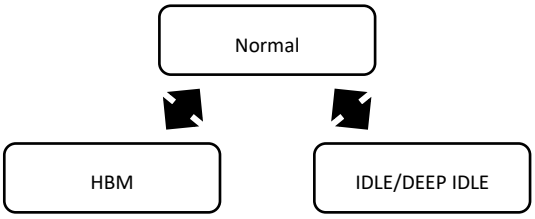
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.56 HBMEN (5EH) : HBM Enable

5EH	HBMEN (HBM Enable)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
HBMEN	C	0	1	0	1	1	1	1	0	(5EH)
1st parameter	W	0	0	0	0	0	0	0	HBM_EN	00H

Description

HBM_EN: 0:exit HBM to Normal mode, 1:enter HBM



Restriction

Register Availability

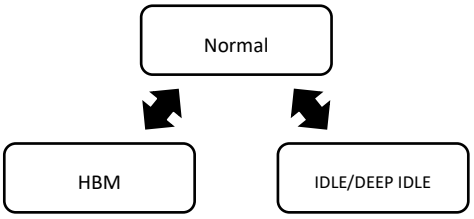
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.57 DPIDLEEN (5FH) : Deep Idle Enable

5FH	DPIDLEEN (Deep Idle Enable)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
DPIDLEEN	C	0	1	0	1	1	1	1	1	(5FH)
1st parameter	W	0	0	0	0	0	0	0	DP_IDLE_EN	00H

Description

DP_IDLE_EN: 0:exit DEEP_IDLE mode to normal mode, 1:enter DEEP_IDLE mode



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.58 RDDDBS (A1H) : Read DDB

A1H	RDDDBS (Read DDB)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDDBS	C	1	0	1	0	0	0	0	1	(A1H)
1st parameter	R	SID[7:0]								00H
2nd parameter	R	SID[15:8]								00H
3rd parameter	R	MID[7:0]								00H
4th parameter	R	MID[15:8]								00H
5th parameter	R	1	1	1	1	1	1	1	1	FFH
Description	SID[15:0]: Supplier ID code MID[15:0]: Module ID code Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.59 RDDDBC (A8H) : Read DDB Continuous

A8H	RDDDBC (Read DDB Continuous)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDDBC	C	1	0	1	0	1	0	0	0	(A8H)
1st parameter	R	SID[7:0]								00H
2nd parameter	R	SID[15:8]								00H
3rd parameter	R	MID[7:0]								00H
4th parameter	R	MID[15:8]								00H
5th parameter	R	1	1	1	1	1	1	1	1	FFH
Description	SID[15:0]: Supplier ID code MID[15:0]: Module ID code Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.									
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.60 RDFCS (AAH) : Read First Checksum

AAH	RDFCS (Read First Checksum)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDFCS	C	1	0	1	0	1	0	1	0	(AAH)
1st parameter	R	FCS[7:0]								00H
Description	This command returns the first checksum what has been calculated from “User Command Set” area registers (not include “Manufacture Command Set”) after the write access to those registers has been done.									
Restriction	It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.61 RDCCS (AFH) : Read Continue Checksum

AFH	RDCCS (Read Continue Checksum)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDCCS	C	1	0	1	0	1	1	1	1	(AFH)
1st parameter	R	CCS[7:0]								00H
Description	This command returns the continuous checksum what has been calculated from “User Command Set” area registers after 150ms.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.62 RDID1 (DAH) : Read Display Identification Information 1

DAH	RDID1 (Read Display Identification Information 1)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDID1	C	1	1	0	1	1	0	1	0	(DAH)
1st parameter	R	ID1[7:0]								00H
Description	This read byte identifies the AMOLED module's manufacturer.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.63 RDID2 (DBH) : Read Display Identification Information 2

DBH	RDID2 (Read Display Identification Information 2)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDID2	C	1	1	0	1	1	0	1	1	(DBH)
1st parameter	R	ID2[7:0]								00H
Description	This read byte identifies the AMOLED module's manufacturer.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.64 RDID3 (DCH) : Read Display Identification Information 3

DCH	RDID3 (Read Display Identification Information 3)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDID3	C	1	1	0	1	1	1	0	0	(DCH)
1st parameter	R	ID3[7:0]								00H
Description	This read byte identifies the AMOLED module's manufacturer.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

11.2.65 RDID4 (DDH) : Read Display Identification Information 4

DDH	RDID4 (Read Display Identification Information 4)									
Inst / Para	W/R/C	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDID4	C	1	1	0	1	1	1	0	0	(DDH)
1st parameter	R	ID41[7:0]								00H
2nd parameter	R	ID42[7:0]								00H
Description	This read byte identifies the AMOLED module's manufacturer.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

12 REVISION HISTORY

Version	Date	Description