ST7312

128 x 64 Dot Matrix OLED/PLED

Segment/Common Driver with Controller

Datasheet

Version 0.3
2023/06

Hazardous Substance Free
RoHS/ REACH Compliant

Sitronix Technology Corporation

LIST OF CONTENT

1. GENERAL DESCRIPTION

ST7312 is a single-chip dot matrix OLED/PLED driver which incorporates controller and common/segment drivers. It contains 128-segment and 64-common driver circuit. This chip can be connected directly to a microprocessor with 8-bit parallel interface, 4-line serial interface (SPI-4), 3-line serial interface (SPI-3) and I2C serial interface. Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 128x64 bits. It performs the display data read/write operation without external operating clock, and the power consumption can be minimized. In addition, since all necessary oscillation circuit and low power consumption circuit for OLED/PLED system are built-in, ST7312 constructs an OLED/PLED display system with the fewest components.

2. FEATURES

- Display Maximum Resolution:
  - Capacity: 128-segment * 64-common
- Microprocessor Interface
  - 8-bit 8080 and 6800 interface support
  - 3-wire SPI and 4-wire SPI serial interface
  - I^2C interface
- On-Chip Power System
  - VDD: 2.4V ~ 3.3V (TYP)
  - VBAT: 3.3V ~ 4.2V (TYP)
- Wide Supply Voltage Range
  - VOLED (Internal Power): 6.0V~ 10.0V (VBAT=3.0V~4.5V)
  - VOLED (External Power): 6.0V~16.5V (VBAT=Floating)
  - VCOMH: 0.65*VOLED ~ 0.83*VOLED
  - Segment maximum source current: 480uA
  - Common maximum sink current: 61.5mA
- On Chip Build-In Circuits
  - Charge pump power circuit
  - Timing controller
  - Internal OSC
  - Power on reset (POR)
- Internal or external I_{REF} selection
- Crosstalk compensation
- Built-in Multi-OTP Programming Circuit
  - Internal VPP power supply
  - Contrast Adjustment
  - ID program
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Screen saving infinite content scrolling function
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Portrait Addressing Mode
- Temperature Range: -40℃ to 85℃
- Package: COG
- ST7312 is designed for consumer applications; this product is not designed for use in cars, motorcycles, marine equipment, aircraft equipment, military equipment and other applications in extreme environment.

3. COMMUNICATION INTERFACE

3.1 Microprocessor Interface

3.1.1 CSB Select Input

CSB pin is s used for chip selection. ST7312 can interface with an MPU when CSB is "L". If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In serial interface (3-Line, 4-Line SPI and I^2C), the internal shift register and serial counter are reset when CSB is “H”.

3.1.2 Parallel / Serial Interface

ST7312 has five types of interface for kinds of MPU. The MPU interface is selected by IF[2:0] pins as shown in Table1.

Table 1 Parallel/Serial Interface Mode

Type	IF2	IF1	IF0	Interface mode
Serial	L	L	L	4-line serial interface
	L	L	H	3-line serial interface
	L	H	L	I^2C serial interface
Parallel	H	H	L	8bit 8080-series MPU mode
	H	L	L	8bit 6800-series MPU mode

3.1.3 Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IF[2:0] as shown in Table 2. The data transfer type is determined by signals of A0, ERD and RWR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

IF1	IF0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
H	L	CSB	A0	E	R/W	D[7:0]	6800-series
H	H			/RD	/WR		8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

3.1.4 Serial Interface

Interface	CSB	A0	ERD	RWR	D[7:0]
3-Line SPI	CSB	--	--	--	D[0]=SCL,D[2:1]=SDA,D[7:3]=GND
4-Line SPI	CSB	A0	--	--	D[0]=SCL,D[2:1]=SDA,D[7:3]=GND
I^2C interface	L	H/ L	--	--	D[0]=SCL,D[2:1]=SDA,D[7:3]=GND, A0=SA[0]. Refer to I2C Interface

Note:

1. The un-used pins are marked as "--" and should be fixed to "H" by VDD.
2. The option setting to be "H" should connect to VDD.
3. The option setting to be "L" should connect to DGND.

3.1.5 3-Line Serial Interface

The 3-Line SPI (9-bit) uses 3 pins (CSB, SDA & SCL) to communicate with MPU. When CSB is "L", IC is active and the SDA and SCL pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9^{th}) clock. After CSB returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit at the 1^{st} bit of each 9-bit serial data.

In 3-Line interface, A0 pin is not available. The 1^{st} output bit defines command byte or parameter byte.

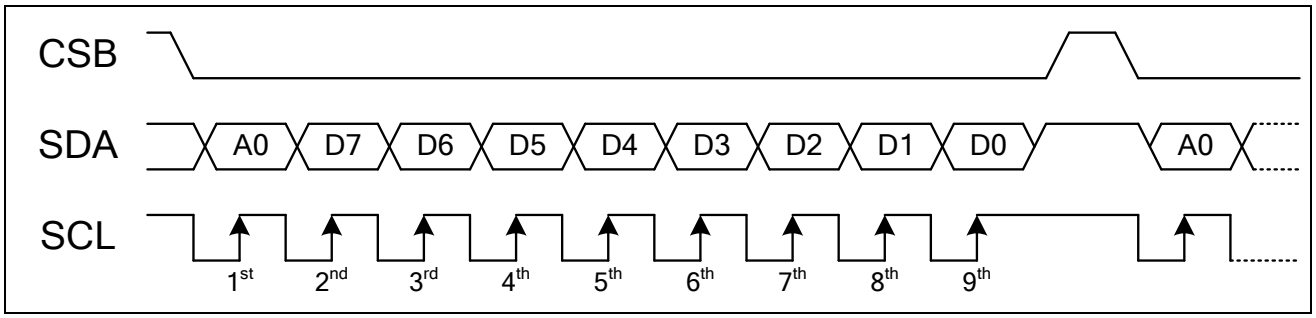


Figure 1 Write Operation of 3-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

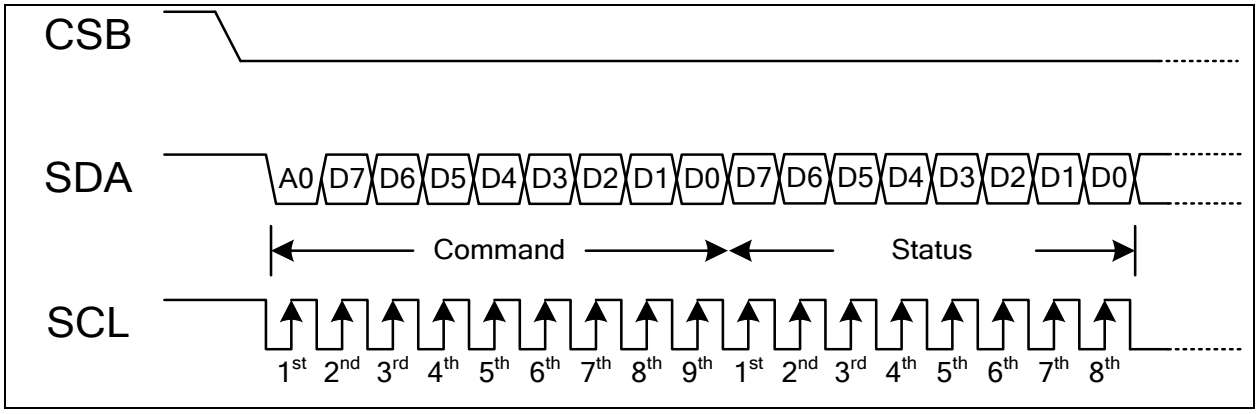


Figure 2 Read Operation of 3-Line SPI

3.1.6 4-Line Serial Interface

ST7312 is active when CSB is “L”, and serial data (SDA) and serial clock (SCL) inputs are enabled. When CSB is “H”, ST7312 is not active, and the internal 8-bit shift register and 3-bit counter are reset. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

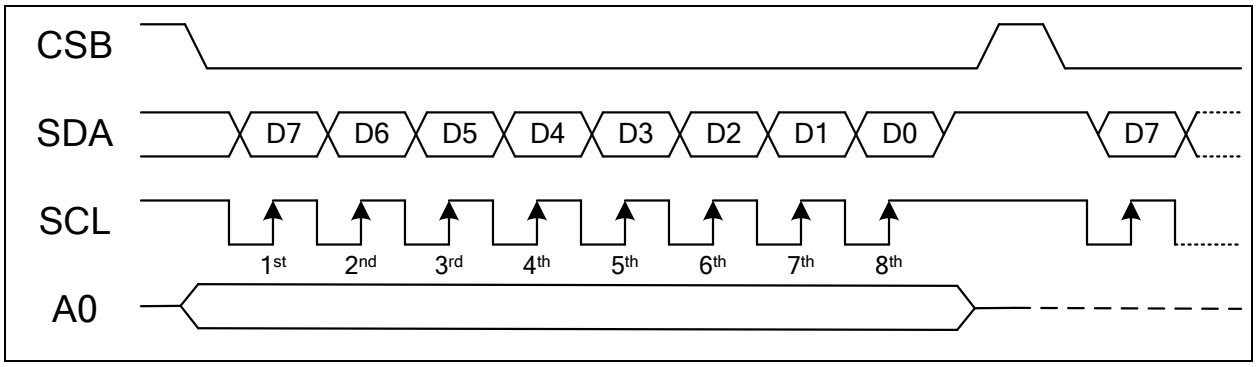


Figure 3 Write Operation of 4-Line SPI

After entering the “Read Mode” to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

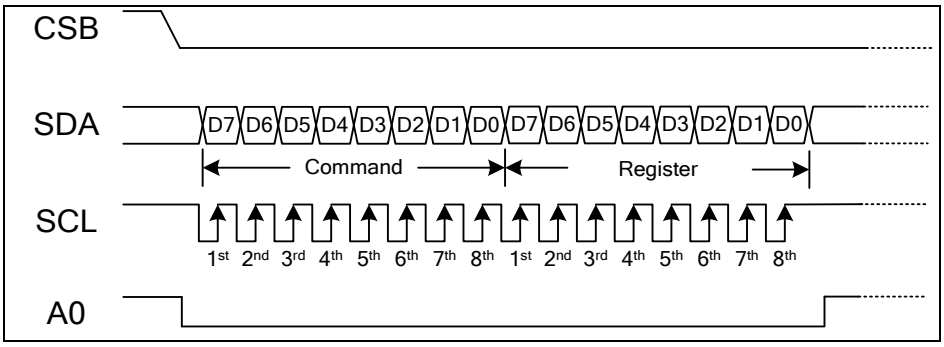


Figure 4 Read Operation of 4-Line SPI

3.1.7 I²C Serial Interface

The I²C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

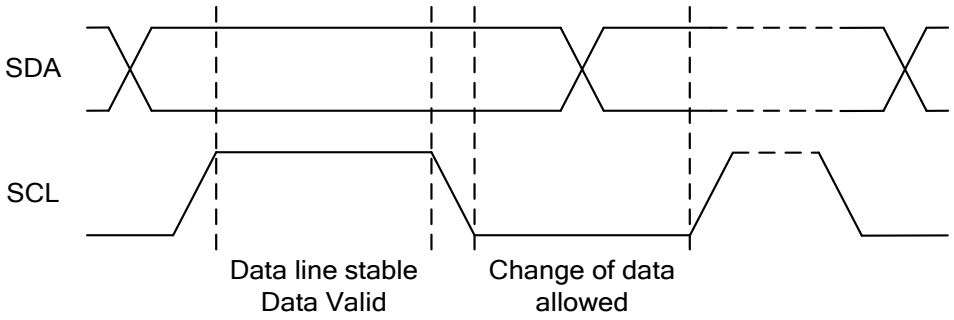


Figure 5 Bit Transfer

START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.

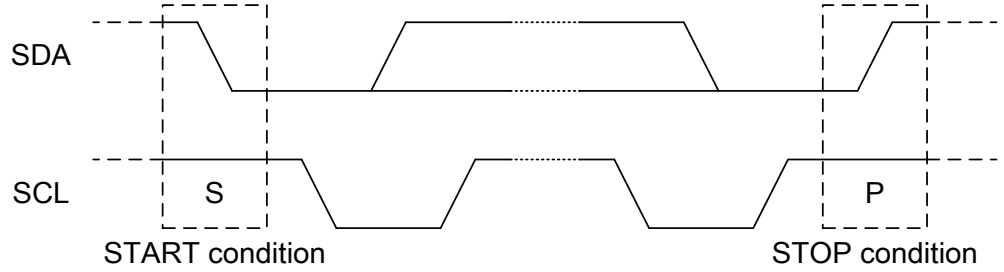


Figure 6 Definitions of START and STOP Condition

System Configuration

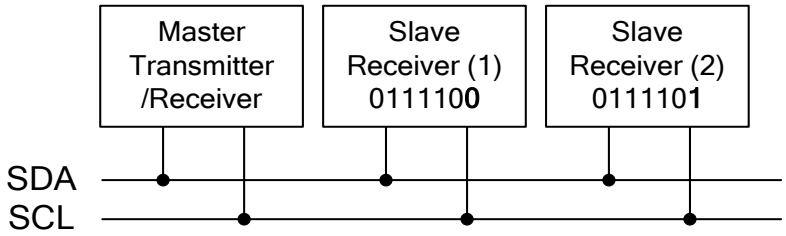


Figure 7 System Configuration

The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated as follows.

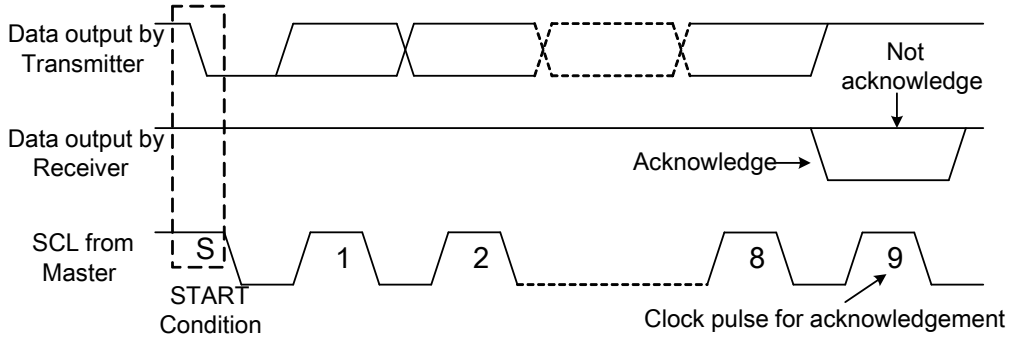
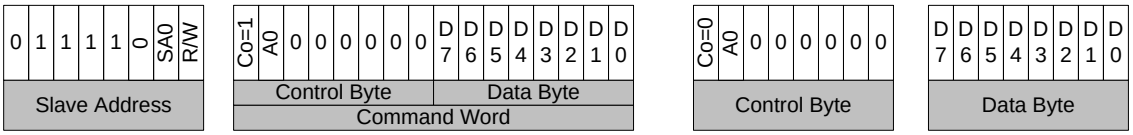


Figure 8 Acknowledgement of I²C Interface

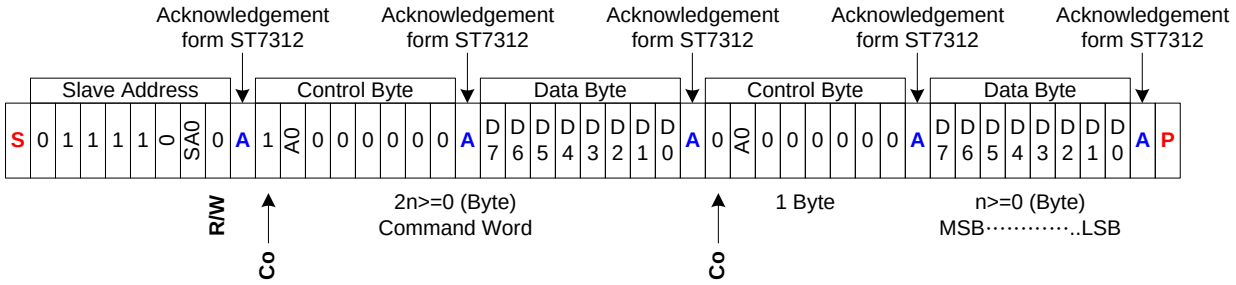
I2C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.



Write Mode (R/W="0")



Read Mode (R/W="1")

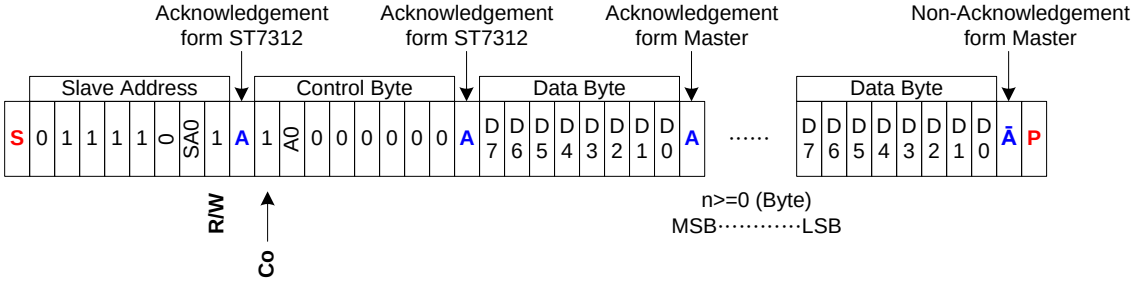


Figure 9 I²C Interface Protocol

3.2 Data Transfer

ST7312 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in **Figure 10** And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in **Figure 11**. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

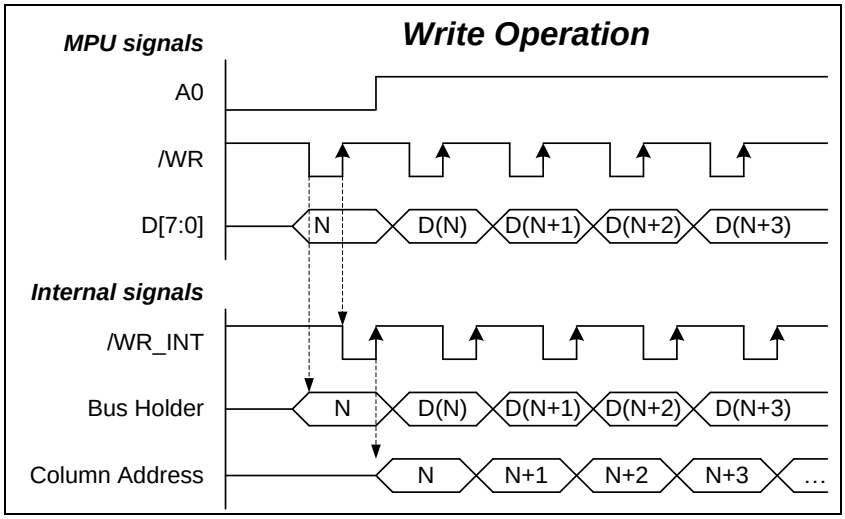


Figure 10 Data Transfer: Write

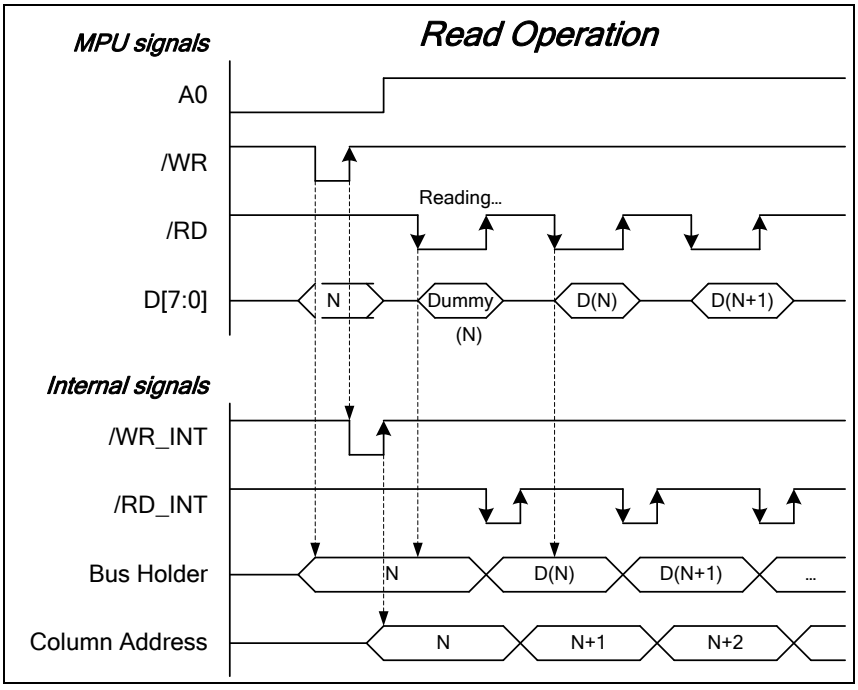


Figure 11 Data Transfer: Read

3.3 Display Data RAM (DDRAM)

ST7312 is built-in a RAM with 128X64 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the panel. It is an addressable array with 128 columns by 64 rows (8-page). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Figure 12 for detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63). The display data (D7~D0) corresponds to the panel common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly. Refer to Figure 13 for detailed illustration. The microprocessor can write to and read from DDRAM by the I/O buffer. Since the OLED controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the screen flicker or data-conflict.

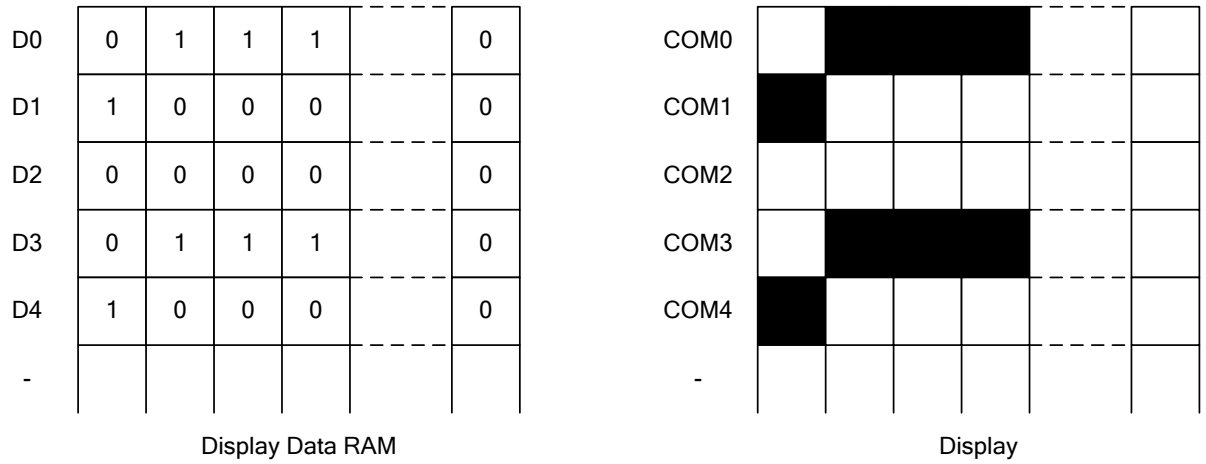


Figure 12 DDRAM Mapping Modes

Figure 13 DDRAM Format

3.3.1 Addressing

Data is downloaded into the Display Data RAM matrix in ST7312 as byte-format. The Display Data RAM has a matrix of 128 by 64 bits. The address ranges are: Y=0~127 (column address), X=0~7 (page address). Addresses outside these ranges are not allowed.

3.3.2 Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 3-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content.

3.3.3 Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. Column Address Circuit has 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). This allows MPU accessing DDRAM content continuously. The column address is automatically incremented from the start up to the end column. During auto-increment, the column address returns to the column start address as the end column is reached.
Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG).

3.4 DDRAM SEG Output Mapping

3.5 Partial Display

ST7312 realizes the Partial Display function with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on panel, driving duty is programmable via the instruction. Moreover, built-in power supply circuits are controlled by the instruction for adjusting the driving voltages.

3.6 Power System

The built-in power circuits generate the voltage and current which are necessary to drive the OLED. It consumes low power with the fewest external component.

I_{SEG} Driving Current

This is used to derive the incoming power sources into the different levels of internal use voltage and current.

1. VOLED is the most positive voltage supply.
2. VCOMH is the common deselected level. It is internally regulated.
3. PGND is the ground path of the analog and panel current.
4. IREF is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current is:

I_{SEG} = Contrast / 256 x IREF x scale factor in which the contrast (0~255) is set by Set Contrast command 81h; and the scale factor is 48 by default.

When external IREF is used, the magnitude of IREF is controlled by the value of resistor, which is connected between IREF pin and VSS. It is recommended to set IREF to 10±2uA so as to achieve I_{SEG} = 480uA at maximum contrast 255

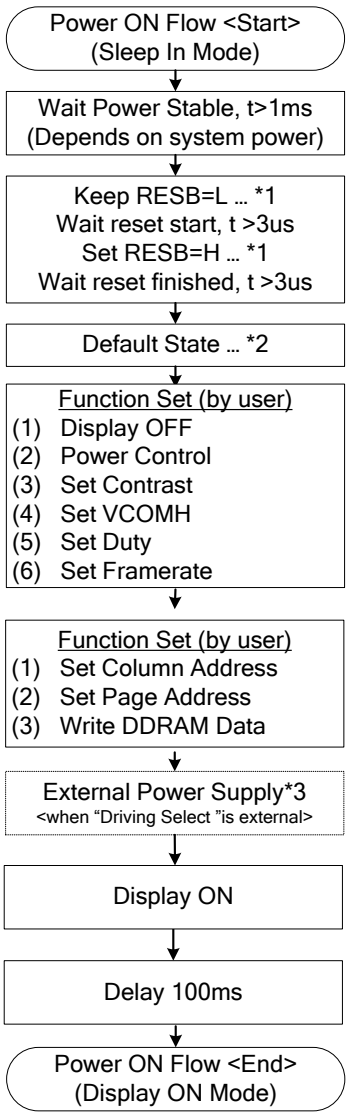
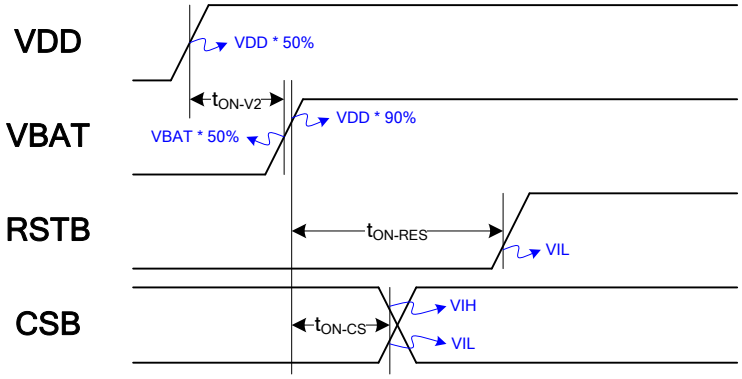
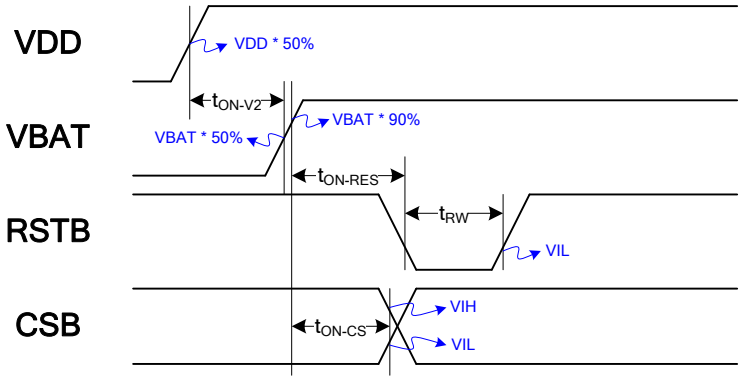
4. RESET CIRCUIT

Setting RSTB pin to “L” can initialize internal function. While RSTB is “L”, no instruction can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON.

The default values of registers are listed below:

5. OPERATION FLOW

5.1 Power ON

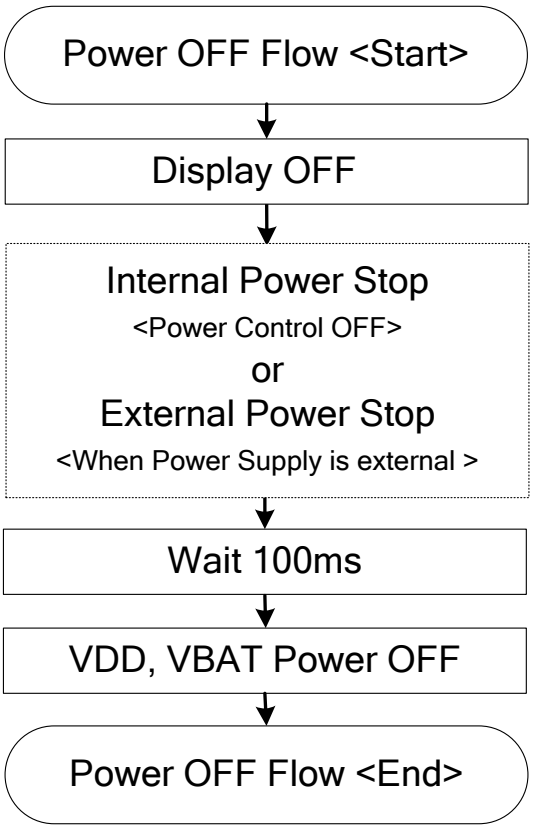
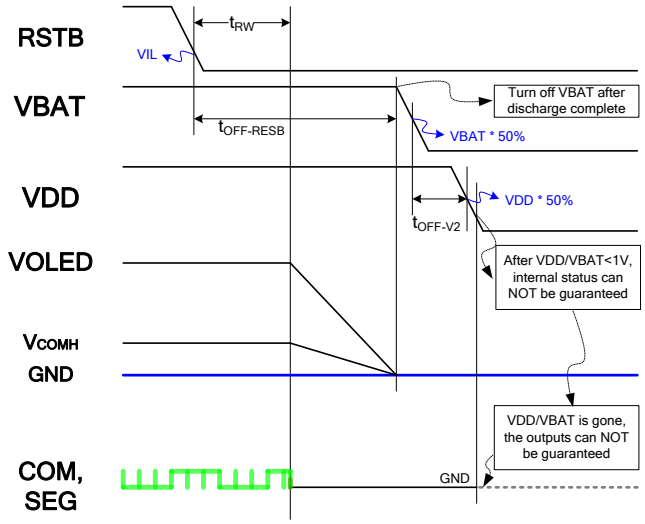
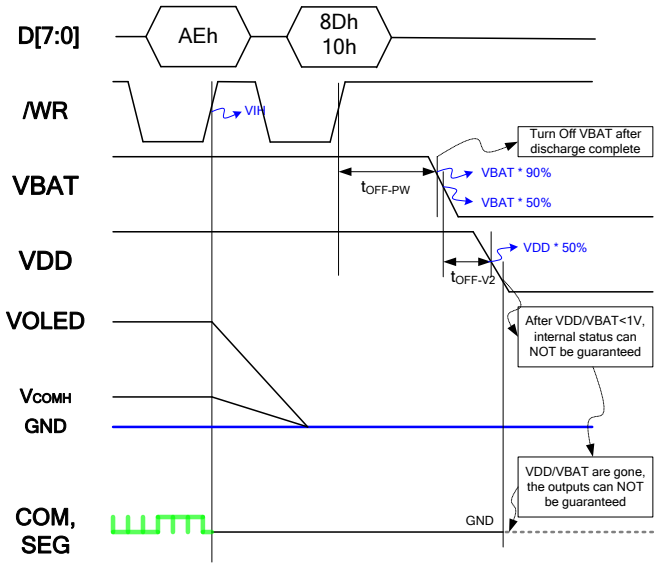
Referential Operation Flow	Operation Sequence
	Case-1: RSTB=L while Power ON  Case-2: RSTB=H while Power ON 

Note

1. Please refer to the specification of tRW and tR.
2. Refer to the section of RESET CIRCUIT
3. The detail instruction functionality is described in Power Control instruction.
4. The power stable is defined as the time that the later power (VDD or VBAT) reaches 90% of its rated voltage.

Item	Symbol	Requirement	Description
VBAT power ON delay	t_{ON-V2}	No Limitation	VDD and VBAT can be applied in any order. IC will NOT be damaged when one of VDD and VBAT is ON but another is OFF. Power stable is defined as the time that the later power (VDD or VBAT) reaches 90% of its rated voltage. Recommend Setting: -50ms ≤ t_{ON-V2} ≤ No Limitation.
RSTB input time	t_{ON-RES}	Case-1 $t_{RW} \leq t_{ON-RES}$ Case-2 No Limitation	RSTB=L can be input at any time after power is stable. t_{RW} & t_R should match the timing specification of RSTB. RSTB has priority over CSB. Recommend Setting: 0 ≤ t_{ON-RES} ≤ 50 ms.
CSB input time	t_{ON-CS}	No Limitation	CSB can be input at any time after power is stable.

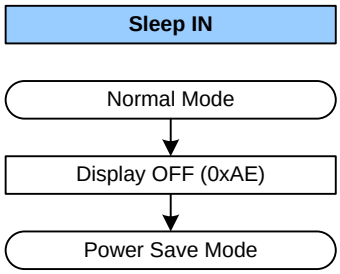
5.2 Power OFF

Referential Operation Flow	Operation Sequence
Case-2  	Case-1: Use RSTB  Case-2: Power OFF at Sleep State 

Item		Symbol	Requirement	Description
Power OFF Time	Case-1	$t_{OFF-RESB}$	200ms ≤$t_{OFF-RESB}$	Power can be turned OFF after built-in power becomes GND.
	Case-2	t_{OFF-PW}	100ms ≤ t_{OFF-PW}	
VBAT power ON delay		t_{OFF-V2}	No Limitation	VDD and VBAT can be powered down in any order. IC will NOT be damaged when one of VDD and VBAT is ON but another is OFF. Recommend Setting: 0 ≤ t_{OFF-V2} ≤ 5ms

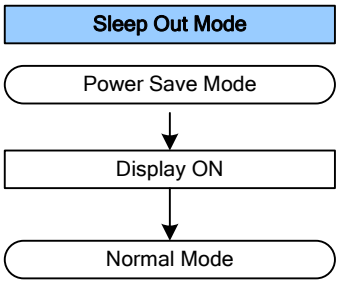
Note: In Case-2, RSTB can fall to GND at the same time as VDD.

5.3 Sleep In



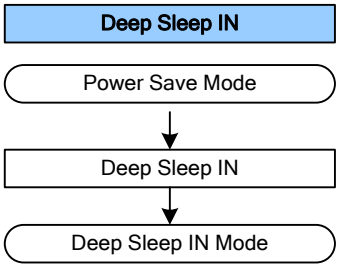
Reference C Code	
WriteCommand (0xAE);	//Display OFF

5.4 Sleep Out



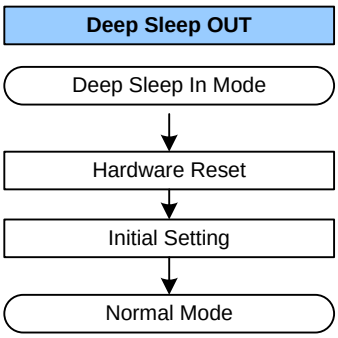
Reference C Code	
WriteCommand(0xAF);	//Display ON

5.5 Deep Sleep In

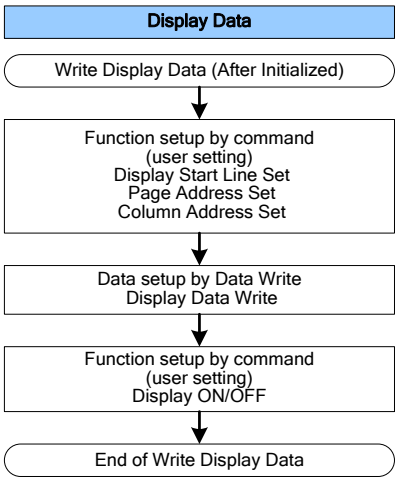


Reference C Code	
WriteCommand(0xAE); WriteCommand(0x94); WriteCommand(0x5A); WriteCommand(0x82); WriteCommand(0x55); WriteCommand(0x55); WriteCommand(0xAA); WriteCommand(0xAA);	//Enter Deep Sleep In Mode

5.6 Deep Sleep Out



5.7 Display Data



Reference C Code

```
Extern unsigned char picture[8][128];                    //Picture must be set
Void WriteDisplayData(void)
{
    int page=0, column=0;                                //Picture data
    int pageAddr=0xB0;                                   //Set page=page0

    WriteCommand(0x40);                                  //Set start line address=0x00

    for( page=0; page<8; page++)                         //Send picture data
    {                                                   //From page 0 to page 8
        WriteCommand(pageAddr);                          //Set Page
        WriteCommand(0x10);                              //Set MSB Column address
        WriteCommand(0x00);                              //Set LSB Column address
        for( column=0; column<128; column++)             //Send picture data
        {                                               //From column 0 to column 128
            WriteData(picture[page][column]);            //Write picture data
        }
        pageAddr++;                                     //Set page= next page
    }
}
    WriteCommand(0xAF);                                  //Display ON(0xAF)
```

6. HANDING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
IO Supply Voltage	VDD	-0.3 to +5.5	V
Power Supply Voltage	VBAT	-0.3 to +5.5	V
VOLED Supply Voltage	VOLED	0 to 18	V
SEG output Voltage	VSEG	0 to VOLED	V
COM output Voltage	VCOM	0 to 0.9*VOLED	V
Input Voltage	Vin	GND-0.5 to VDD+0.5	V
Operating Temperature Range	TA	-40 to +85	℃
Storage Temperature Range	TSTG	-65 to +150	℃

Notes

1. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

2. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/Timing Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.

3. Insure the voltage levels of VBAT, VOLED and VCOMH always match the correct relation: VOLED > VCOMH > VBAT > VSS

4. VIN should be less than or equal to 5.5V. (VIN ≤ 5.5V)

7.2 DC Characteristics

DC Electrical Characteristics (VDD= 3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Power Supply	VDD	1.65	-	3.5	V	
Analog Power Supply	VBAT	3.0	-	4.5	V	
Charge Pump Regulator Supply (Charge Pump Output Voltage ITO resistance < 3Ω for charge pump related pins)	VOLED 6V Mode	5.5	6	-	V	
	VOLED 7.5V Mode	7	7.5	-	V	
	VOLED 8.5V Mode	8	8.5	-	V	
	VOLED 9V Mode	8.5	9	-	V	
	VOLED 10V Mode	9.5	10		V	
Sleep Mode Current	I_{DD}	-	-	10	uA	VDD = 1.65V~3.5V VOLED = 6.0V~16.5V Display OFF
	I_{BAT}	-	-	10	uA	VDD = 1.65V~3.5V VBAT = 3.0V~4.5V Display OFF
	I_{OLED}	-	-	10	uA	VDD = 1.65V~3.6V VOLED = 6.0V~16.5V Display OFF
Display ON Current (Pattern: All ON)	I_{OLED}	-	700	900	uA	VDD = 2.8V VOLED = 12V IREF = 10uA Contrast=FFh
	I_{DD}	-	305	375	uA	VDD = 2.8V VOLED = 12V IREF = 10uA Contrast=FFh

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Segment Output Current (Display ON)	I_{SEG}	-	480	-	uA	VDD=2.8V, VOLED=12V, IREF=10uA Contrast=FFh
		-	330	-	uA	VDD=2.8V, VOLED=12V, IREF=10uA Contrast=AFh
		-	120	-	uA	VDD=2.8V, VOLED=12V, IREF=10uA Contrast=3Fh
Segment Output Current Uniformity	Dev	-3	-	+3	%	Dev = (I_{SEG} – IMID)/IMID IMID = (IMAX + IMIN)/2 I_{SEG} [0:127] = Segment current at contrast=FFh
Adjacent Pin Output Current Uniformity (Contrast = FF)	Adj. Dev	-2	-	+2	%	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])
Logic-High Input Voltage	V_{IH}	0.8 x VDD	-	-	V	
Logic-Low Input Voltage	V_{IL}	-	-	0.2 x VDD	V	
Logic-High Output Voltage	V_{OH}	0.9 x VDD	-	-	V	
Logic-Low Output Voltage	V_{OL}	-	-	0.1 x VDD	V	

7.3 AC Characteristics

AC Electrical Characteristics (VDD= 2.8V, GND= 0V, TA=25°C, Bare Chip)

8.3.1 System Operation AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Frequency of Display Timing Generator	FOSC(1)	620	688	755	KHz	VDD=2.8V
Frame Frequency	FRM	-	Foscx1 / (DxKx64)(2)	-	Hz	128x64 Normal Mode, Display ON, Internal Oscillator Enabled
Reset Low Pulse Width		3			us	

Note :

1. FOSC stands for the frequency value of the internal oscillator and the value is measured when command D5h is in default value.

2. D: divide ratio (default value = 1)

   K: number of display clocks per row period (default value = 103)

8. REVISION HISTORY

Version	Date	Description
V0.1	2022/12/27	First Edition
V0.2	2023/06/09	Type Error Edition
V0.3	2023/06/27	Add Interface Setting