ST7257

720x544 System-On-Chip Driver

for 480RGBx272 TFT LCD

Datasheet

Version 1.1
2018/06

Sitronix Technology Corporation

LIST OF CONTENT

1. GENERAL DESCRIPTION

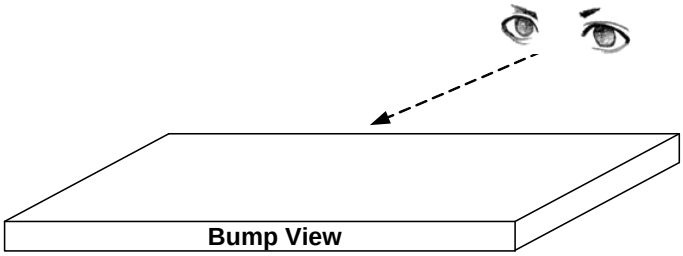
ST7257 offers all-in-one chip solution of 480RGBx272 for color TFT-LCD panel. This chip incorporated with digital timing generator, source and gate driver, power supply circuit, embedded serial communication interface for function setting. The source output support real 8-bit resolution and 256-gray scale with small output deviation are designed to support higher color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

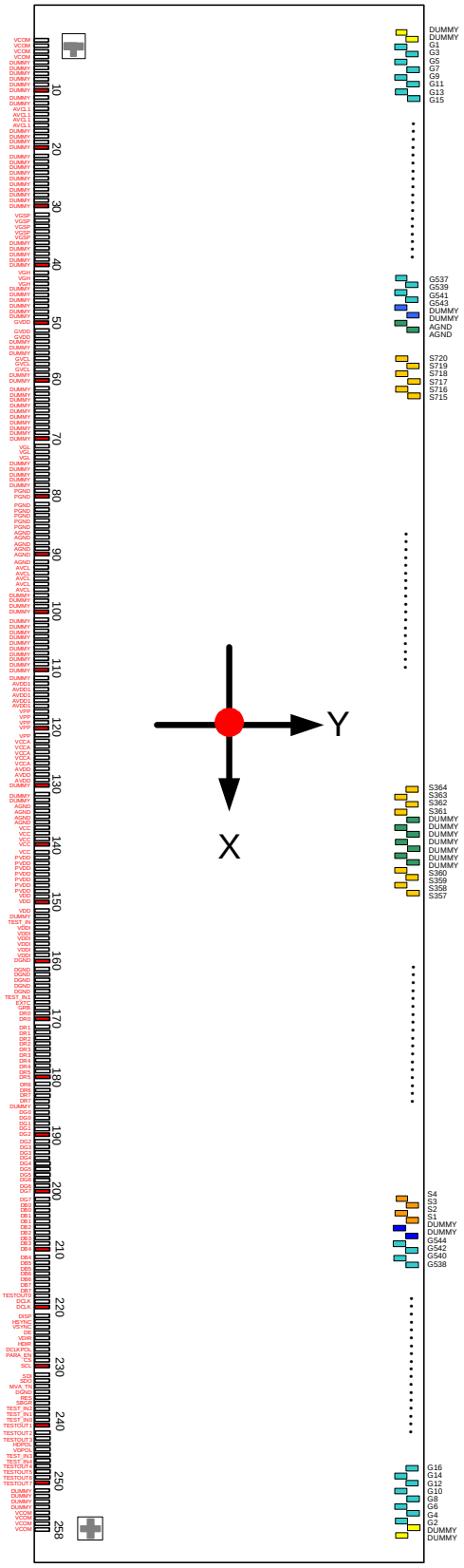
2. FEATURES

- Display Resolution: 480*RGB (H) *272(V)
- LCD Driver Output Circuits
  - Source Outputs: 720 Channels
  - Gate Outputs: 544 Channels
  - Common Electrode Output
- 256 gray scale with true 8 bit DAC
- Support SYNC, SYNC-DE and DE mode RGB interface input timing
- Support 24-bit parallel and 8-bit serial RGB interface
- Support 3- wire Serial Peripheral Interface to config and control display
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory to store initial Register setting and factory default value
  - Timing Controller
- Driving Algorithm.
  - Dot Inversion.
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ VDD
  - Analog Voltage (VDD to AGND): 3.0V ~ 3.6V
  - Charge pump Voltage (PVDD to PGND): 3.0V ~ 3.6V
- On-Chip Power System
  - GVDD: +4.9600V ~ +5.9680V
  - GVCL: - 4.4800V ~ - 2.9600V
  - Gate driver HIGH level (VGH to AGND): +12V ~ +16V
  - Gate driver LOW level (VGL to AGND): -12V ~ -7V
- Optimized layout for COG Assembly
- Non-Volatile Memory (OTP) can only program one time for LCD VCOM calibration
- This driver does not have embedded temperature sensor circuit and can not support LCD output voltage temperature compensation function. The display quality would vary with temperature.
- **Design for Consumer and Industrial Applications; Automotive Related Products are Excluded**

3. PAD ARRANGEMENT

3.1 Output Bump Dimension



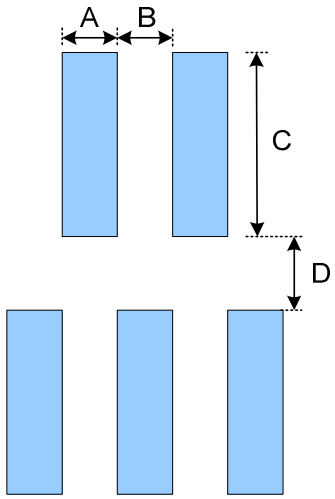


3.2 Bump Dimension

Output Pads

S1~S720、G1~G544、VCOM、DUMMY

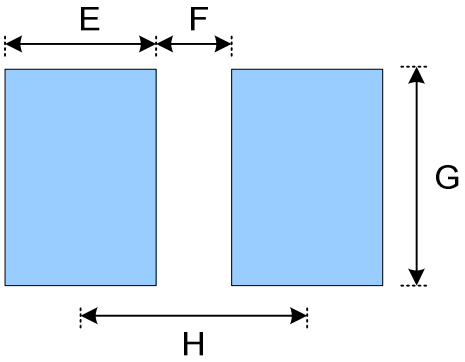
(No.259~1547)



Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	15 um
C	Bump Height	92 um
D	Bump Gap 2 (Vertical)	38 um
A x C	Bump Area	1380 um^2

Input Pads

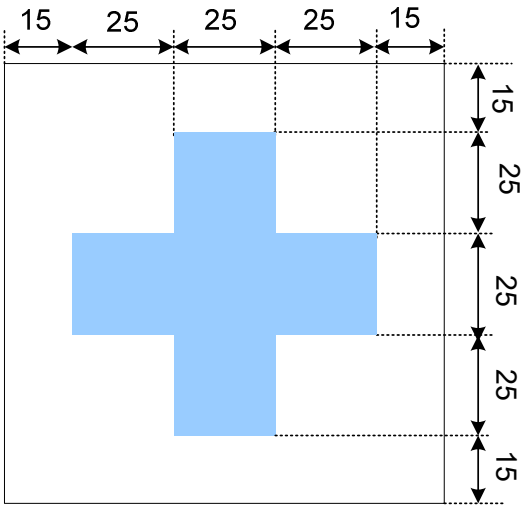
(No.1~258)



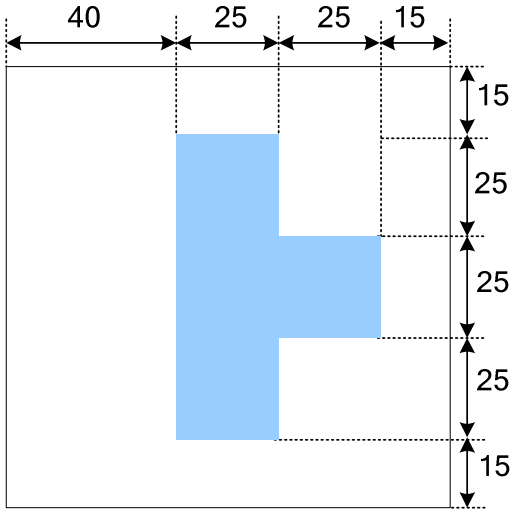
Symbol	Item	Size
E	Bump Width	50 um
F	Bump Gap	25 um
G	Bump Height	90 um
H	Bump Pitch	110 um
E x G	Bump Area	4500 um^2

3.3 Alignment Mark Dimension

Alignment Mark: A1(X,Y)=(9605,-142.5)



Alignment Mark: A2(X,Y)=(-9605,-142.5)



3.4 Chip Information

Chip size	19665μm x720μm
Chip thickness	300μm± 15um
Pad Location	Pad center
Coordinate Origin	Chip center
Au bump height	9um± 2um

*Remark: Chip dimension include scribe line

4. PAD CENTER COORDINATES

No.	PIN Name	X	Y	No.	PIN Name	X	Y	No.	PIN Name	X	Y
1	VCOM	-9637.5	-270	35	VGSP	-7087.5	-270	69	DUMMY	-4537.5	-270
2	VCOM	-9562.5	-270	36	DUMMY	-7012.5	-270	70	DUMMY	-4462.5	-270
3	VCOM	-9487.5	-270	37	DUMMY	-6937.5	-270	71	VGL	-4387.5	-270
4	VCOM	-9412.5	-270	38	DUMMY	-6862.5	-270	72	VGL	-4312.5	-270
5	DUMMY	-9337.5	-270	39	DUMMY	-6787.5	-270	73	VGL	-4237.5	-270
6	DUMMY	-9262.5	-270	40	DUMMY	-6712.5	-270	74	DUMMY	-4162.5	-270
7	DUMMY	-9187.5	-270	41	VGH	-6637.5	-270	75	DUMMY	-4087.5	-270
8	DUMMY	-9112.5	-270	42	VGH	-6562.5	-270	76	DUMMY	-4012.5	-270
9	DUMMY	-9037.5	-270	43	VGH	-6487.5	-270	77	DUMMY	-3937.5	-270
10	DUMMY	-8962.5	-270	44	DUMMY	-6412.5	-270	78	DUMMY	-3862.5	-270
11	DUMMY	-8887.5	-270	45	DUMMY	-6337.5	-270	79	PGND	-3787.5	-270
12	DUMMY	-8812.5	-270	46	DUMMY	-6262.5	-270	80	PGND	-3712.5	-270
13	AVCL1	-8737.5	-270	47	DUMMY	-6187.5	-270	81	PGND	-3637.5	-270
14	AVCL1	-8662.5	-270	48	DUMMY	-6112.5	-270	82	PGND	-3562.5	-270
15	AVCL1	-8587.5	-270	49	DUMMY	-6037.5	-270	83	PGND	-3487.5	-270
16	AVCL1	-8512.5	-270	50	GVDD	-5962.5	-270	84	PGND	-3412.5	-270
17	DUMMY	-8437.5	-270	51	GVDD	-5887.5	-270	85	PGND	-3337.5	-270
18	DUMMY	-8362.5	-270	52	GVDD	-5812.5	-270	86	AGND	-3262.5	-270
19	DUMMY	-8287.5	-270	53	DUMMY	-5737.5	-270	87	AGND	-3187.5	-270
20	DUMMY	-8212.5	-270	54	DUMMY	-5662.5	-270	88	AGND	-3112.5	-270
21	DUMMY	-8137.5	-270	55	DUMMY	-5587.5	-270	89	AGND	-3037.5	-270
22	DUMMY	-8062.5	-270	56	GVCL	-5512.5	-270	90	AGND	-2962.5	-270
23	DUMMY	-7987.5	-270	57	GVCL	-5437.5	-270	91	AGND	-2887.5	-270
24	DUMMY	-7912.5	-270	58	GVCL	-5362.5	-270	92	AVCL	-2812.5	-270
25	DUMMY	-7837.5	-270	59	DUMMY	-5287.5	-270	93	AVCL	-2737.5	-270
26	DUMMY	-7762.5	-270	60	DUMMY	-5212.5	-270	94	AVCL	-2662.5	-270
27	DUMMY	-7687.5	-270	61	DUMMY	-5137.5	-270	95	AVCL	-2587.5	-270
28	DUMMY	-7612.5	-270	62	DUMMY	-5062.5	-270	96	AVCL	-2512.5	-270
29	DUMMY	-7537.5	-270	63	DUMMY	-4987.5	-270	97	DUMMY	-2437.5	-270
30	DUMMY	-7462.5	-270	64	DUMMY	-4912.5	-270	98	DUMMY	-2362.5	-270
31	VGSP	-7387.5	-270	65	DUMMY	-4837.5	-270	99	DUMMY	-2287.5	-270
32	VGSP	-7312.5	-270	66	DUMMY	-4762.5	-270	100	DUMMY	-2212.5	-270
33	VGSP	-7237.5	-270	67	DUMMY	-4687.5	-270	101	DUMMY	-2137.5	-270
34	VGSP	-7162.5	-270	68	DUMMY	-4612.5	-270	102	DUMMY	-2062.5	-270

No.	PIN Name	X	Y
103	DUMMY	-1987.5	-270
104	DUMMY	-1912.5	-270
105	DUMMY	-1837.5	-270
106	DUMMY	-1762.5	-270
107	DUMMY	-1687.5	-270
108	DUMMY	-1612.5	-270
109	DUMMY	-1537.5	-270
110	DUMMY	-1462.5	-270
111	DUMMY	-1387.5	-270
112	AVDD1	-1312.5	-270
113	AVDD1	-1237.5	-270
114	AVDD1	-1162.5	-270
115	AVDD1	-1087.5	-270
116	AVDD1	-1012.5	-270
117	VPP	-937.5	-270
118	VPP	-862.5	-270
119	VPP	-787.5	-270
120	VPP	-712.5	-270
121	VPP	-637.5	-270
122	VCCA	-562.5	-270
123	VCCA	-487.5	-270
124	VCCA	-412.5	-270
125	VCCA	-337.5	-270
126	VCCA	-262.5	-270
127	AVDD	-187.5	-270
128	AVDD	-112.5	-270
129	AVDD	-37.5	-270
130	DUMMY	37.5	-270
131	DUMMY	112.5	-270
132	DUMMY	187.5	-270
133	AGND	262.5	-270
134	AGND	337.5	-270
135	AGND	412.5	-270
136	AGND	487.5	-270
137	VCC	562.5	-270
138	VCC	637.5	-270
139	VCC	712.5	-270
140	VCC	787.5	-270
141	VCC	862.5	-270
142	PVDD	937.5	-270
143	PVDD	1012.5	-270
144	PVDD	1087.5	-270
145	PVDD	1162.5	-270
146	PVDD	1237.5	-270
147	PVDD	1312.5	-270
148	PVDD	1387.5	-270
149	VDD	1462.5	-270
150	VDD	1537.5	-270
151	VDD	1612.5	-270
152	DUMMY	1687.5	-270
153	TEST_IN5	1762.5	-270
154	VDDI	1837.5	-270
155	VDDI	1912.5	-270
156	VDDI	1987.5	-270
157	VDDI	2062.5	-270
158	VDDI	2137.5	-270
159	VDDI	2212.5	-270
160	DGND	2287.5	-270
161	DGND	2362.5	-270
162	DGND	2437.5	-270
163	DGND	2512.5	-270
164	DGND	2587.5	-270
165	DGND	2662.5	-270
166	TEST_IN3	2737.5	-270
167	EXTC	2812.5	-270
168	GRB	2887.5	-270
169	DR0	2962.5	-270
170	DR0	3037.5	-270
171	DR1	3112.5	-270
172	DR1	3187.5	-270
173	DR2	3262.5	-270
174	DR2	3337.5	-270
175	DR3	3412.5	-270
176	DR3	3487.5	-270
177	DR4	3562.5	-270
178	DR4	3637.5	-270
179	DR5	3712.5	-270
180	DR5	3787.5	-270
181	DR6	3862.5	-270
182	DR6	3937.5	-270
183	DR7	4012.5	-270
184	DR7	4087.5	-270
185	DUMMY	4162.5	-270
186	DG0	4237.5	-270
187	DG0	4312.5	-270
188	DG1	4387.5	-270
189	DG1	4462.5	-270
190	DG2	4537.5	-270
191	DG2	4612.5	-270
192	DG3	4687.5	-270
193	DG3	4762.5	-270
194	DG4	4837.5	-270
195	DG4	4912.5	-270
196	DG5	4987.5	-270
197	DG5	5062.5	-270
198	DG6	5137.5	-270
199	DG6	5212.5	-270
200	DG7	5287.5	-270
201	DG7	5362.5	-270
202	DB0	5437.5	-270
203	DB0	5512.5	-270
204	DB1	5587.5	-270

No.	PIN Name	X	Y
205	DB1	5662.5	-270
206	DB2	5737.5	-270
207	DB2	5812.5	-270
208	DB3	5887.5	-270
209	DB3	5962.5	-270
210	DB4	6037.5	-270
211	DB4	6112.5	-270
212	DB5	6187.5	-270
213	DB5	6262.5	-270
214	DB6	6337.5	-270
215	DB6	6412.5	-270
216	DB7	6487.5	-270
217	DB7	6562.5	-270
218	TESTOUT0	6637.5	-270
219	DCLK	6712.5	-270
220	DCLK	6787.5	-270
221	DISP	6862.5	-270
222	HSYNC	6937.5	-270
223	VSYNC	7012.5	-270
224	DE	7087.5	-270
225	VDIR	7162.5	-270
226	HDIR	7237.5	-270
227	DCLKPOL	7312.5	-270
228	PARA_SERI	7387.5	-270
229	CS	7462.5	-270
230	SCL	7537.5	-270
231	SDI	7612.5	-270
232	SDO	7687.5	-270
233	MVA_TN	7762.5	-270
234	DGND	7837.5	-270
235	RES	7912.5	-270
236	SBGR	7987.5	-270
237	TEST_IN2	8062.5	-270
238	TEST_IN1	8137.5	-270
239	TEST_IN0	8212.5	-270
240	TESTOUT1	8287.5	-270
241	TESTOUT2	8362.5	-270
242	TESTOUT3	8437.5	-270
243	HDPOL	8512.5	-270
244	VDPOL	8587.5	-270
245	TEST_IN6	8662.5	-270
246	TEST_IN4	8737.5	-270
247	TESTOUT4	8812.5	-270
248	TESTOUT5	8887.5	-270
249	TESTOUT6	8962.5	-270
250	TESTOUT7	9037.5	-270
251	DUMMY	9112.5	-270
252	DUMMY	9187.5	-270
253	DUMMY	9262.5	-270
254	DUMMY	9337.5	-270
255	VCOM	9412.5	-270
256	VCOM	9487.5	-270
257	VCOM	9562.5	-270
258	VCOM	9637.5	-270
259	DUMMY	9660	269
260	DUMMY	9645	139
261	DUMMY	9630	269
262	DUMMY	9615	139
263	G2	9600	269
264	G4	9585	139
265	G6	9570	269
266	G8	9555	139
267	G10	9540	269
268	G12	9525	139
269	G14	9510	269
270	G16	9495	139
271	G18	9480	269
272	G20	9465	139
273	G22	9450	269
274	G24	9435	139
275	G26	9420	269
276	G28	9405	139
277	G30	9390	269
278	G32	9375	139
279	G34	9360	269
280	G36	9345	139
281	G38	9330	269
282	G40	9315	139
283	G42	9300	269
284	G44	9285	139
285	G46	9270	269
286	G48	9255	139
287	G50	9240	269
288	G52	9225	139
289	G54	9210	269
290	G56	9195	139
291	G58	9180	269
292	G60	9165	139
293	G62	9150	269
294	G64	9135	139
295	G66	9120	269
296	G68	9105	139
297	G70	9090	269
298	G72	9075	139
299	G74	9060	269
300	G76	9045	139
301	G78	9030	269
302	G80	9015	139
303	G82	9000	269
304	G84	8985	139
305	G86	8970	269
306	G88	8955	139

No.	PIN Name	X	Y
307	G90	8940	269
308	G92	8925	139
309	G94	8910	269
310	G96	8895	139
311	G98	8880	269
312	G100	8865	139
313	G102	8850	269
314	G104	8835	139
315	G106	8820	269
316	G108	8805	139
317	G110	8790	269
318	G112	8775	139
319	G114	8760	269
320	G116	8745	139
321	G118	8730	269
322	G120	8715	139
323	G122	8700	269
324	G124	8685	139
325	G126	8670	269
326	G128	8655	139
327	G130	8640	269
328	G132	8625	139
329	G134	8610	269
330	G136	8595	139
331	G138	8580	269
332	G140	8565	139
333	G142	8550	269
334	G144	8535	139
335	G146	8520	269
336	G148	8505	139
337	G150	8490	269
338	G152	8475	139
339	G154	8460	269
340	G156	8445	139
341	G158	8430	269
342	G160	8415	139
343	G162	8400	269
344	G164	8385	139
345	G166	8370	269
346	G168	8355	139
347	G170	8340	269
348	G172	8325	139
349	G174	8310	269
350	G176	8295	139
351	G178	8280	269
352	G180	8265	139
353	G182	8250	269
354	G184	8235	139
355	G186	8220	269
356	G188	8205	139
357	G190	8190	269
358	G192	8175	139
359	G194	8160	269
360	G196	8145	139
361	G198	8130	269
362	G200	8115	139
363	G202	8100	269
364	G204	8085	139
365	G206	8070	269
366	G208	8055	139
367	G210	8040	269
368	G212	8025	139
369	G214	8010	269
370	G216	7995	139
371	G218	7980	269
372	G220	7965	139
373	G222	7950	269
374	G224	7935	139
375	G226	7920	269
376	G228	7905	139
377	G230	7890	269
378	G232	7875	139
379	G234	7860	269
380	G236	7845	139
381	G238	7830	269
382	G240	7815	139
383	G242	7800	269
384	G244	7785	139
385	G246	7770	269
386	G248	7755	139
387	G250	7740	269
388	G252	7725	139
389	G254	7710	269
390	G256	7695	139
391	G258	7680	269
392	G260	7665	139
393	G262	7650	269
394	G264	7635	139
395	G266	7620	269
396	G268	7605	139
397	G270	7590	269
398	G272	7575	139
399	G274	7560	269
400	G276	7545	139
401	G278	7530	269
402	G280	7515	139
403	G282	7500	269
404	G284	7485	139
405	G286	7470	269
406	G288	7455	139
407	G290	7440	269
408	G292	7425	139

No.	PIN Name	X	Y
409	G294	7410	269
410	G296	7395	139
411	G298	7380	269
412	G300	7365	139
413	G302	7350	269
414	G304	7335	139
415	G306	7320	269
416	G308	7305	139
417	G310	7290	269
418	G312	7275	139
419	G314	7260	269
420	G316	7245	139
421	G318	7230	269
422	G320	7215	139
423	G322	7200	269
424	G324	7185	139
425	G326	7170	269
426	G328	7155	139
427	G330	7140	269
428	G332	7125	139
429	G334	7110	269
430	G336	7095	139
431	G338	7080	269
432	G340	7065	139
433	G342	7050	269
434	G344	7035	139
435	G346	7020	269
436	G348	7005	139
437	G350	6990	269
438	G352	6975	139
439	G354	6960	269
440	G356	6945	139
441	G358	6930	269
442	G360	6915	139
443	G362	6900	269
444	G364	6885	139
445	G366	6870	269
446	G368	6855	139
447	G370	6840	269
448	G372	6825	139
449	G374	6810	269
450	G376	6795	139
451	G378	6780	269
452	G380	6765	139
453	G382	6750	269
454	G384	6735	139
455	G386	6720	269
456	G388	6705	139
457	G390	6690	269
458	G392	6675	139
459	G394	6660	269
460	G396	6645	139
461	G398	6630	269
462	G400	6615	139
463	G402	6600	269
464	G404	6585	139
465	G406	6570	269
466	G408	6555	139
467	G410	6540	269
468	G412	6525	139
469	G414	6510	269
470	G416	6495	139
471	G418	6480	269
472	G420	6465	139
473	G422	6450	269
474	G424	6435	139
475	G426	6420	269
476	G428	6405	139
477	G430	6390	269
478	G432	6375	139
479	G434	6360	269
480	G436	6345	139
481	G438	6330	269
482	G440	6315	139
483	G442	6300	269
484	G444	6285	139
485	G446	6270	269
486	G448	6255	139
487	G450	6240	269
488	G452	6225	139
489	G454	6210	269
490	G456	6195	139
491	G458	6180	269
492	G460	6165	139
493	G462	6150	269
494	G464	6135	139
495	G466	6120	269
496	G468	6105	139
497	G470	6090	269
498	G472	6075	139
499	G474	6060	269
500	G476	6045	139
501	G478	6030	269
502	G480	6015	139
503	G482	6000	269
504	G484	5985	139
505	G486	5970	269
506	G488	5955	139
507	G490	5940	269
508	G492	5925	139
509	G494	5910	269
510	G496	5895	139

No.	PIN Name	X	Y
511	G498	5880	269
512	G500	5865	139
513	G502	5850	269
514	G504	5835	139
515	G506	5820	269
516	G508	5805	139
517	G510	5790	269
518	G512	5775	139
519	G514	5760	269
520	G516	5745	139
521	G518	5730	269
522	G520	5715	139
523	G522	5700	269
524	G524	5685	139
525	G526	5670	269
526	G528	5655	139
527	G530	5640	269
528	G532	5625	139
529	G534	5610	269
530	G536	5595	139
531	G538	5580	269
532	G540	5565	139
533	G542	5550	269
534	G544	5535	139
535	DUMMY	5520	269
536	DUMMY	5505	139
537	DUMMY	5490	269
538	DUMMY	5475	139
539	DUMMY	5460	269
540	DUMMY	5445	139
541	S1	5430	269
542	S2	5415	139
543	S3	5400	269
544	S4	5385	139
545	S5	5370	269
546	S6	5355	139
547	S7	5340	269
548	S8	5325	139
549	S9	5310	269
550	S10	5295	139
551	S11	5280	269
552	S12	5265	139
553	S13	5250	269
554	S14	5235	139
555	S15	5220	269
556	S16	5205	139
557	S17	5190	269
558	S18	5175	139
559	S19	5160	269
560	S20	5145	139
561	S21	5130	269
562	S22	5115	139
563	S23	5100	269
564	S24	5085	139
565	S25	5070	269
566	S26	5055	139
567	S27	5040	269
568	S28	5025	139
569	S29	5010	269
570	S30	4995	139
571	S31	4980	269
572	S32	4965	139
573	S33	4950	269
574	S34	4935	139
575	S35	4920	269
576	S36	4905	139
577	S37	4890	269
578	S38	4875	139
579	S39	4860	269
580	S40	4845	139
581	S41	4830	269
582	S42	4815	139
583	S43	4800	269
584	S44	4785	139
585	S45	4770	269
586	S46	4755	139
587	S47	4740	269
588	S48	4725	139
589	S49	4710	269
590	S50	4695	139
591	S51	4680	269
592	S52	4665	139
593	S53	4650	269
594	S54	4635	139
595	S55	4620	269
596	S56	4605	139
597	S57	4590	269
598	S58	4575	139
599	S59	4560	269
600	S60	4545	139
601	S61	4530	269
602	S62	4515	139
603	S63	4500	269
604	S64	4485	139
605	S65	4470	269
606	S66	4455	139
607	S67	4440	269
608	S68	4425	139
609	S69	4410	269
610	S70	4395	139
611	S71	4380	269
612	S72	4365	139

No.	PIN Name	X	Y
613	S73	4350	269
614	S74	4335	139
615	S75	4320	269
616	S76	4305	139
617	S77	4290	269
618	S78	4275	139
619	S79	4260	269
620	S80	4245	139
621	S81	4230	269
622	S82	4215	139
623	S83	4200	269
624	S84	4185	139
625	S85	4170	269
626	S86	4155	139
627	S87	4140	269
628	S88	4125	139
629	S89	4110	269
630	S90	4095	139
631	S91	4080	269
632	S92	4065	139
633	S93	4050	269
634	S94	4530	269
635	S95	4515	139
636	S96	4500	269
637	S97	4485	139
638	S98	4470	269
639	S99	4455	139
640	S100	4440	269
641	S101	4425	139
642	S102	4410	269
643	S103	4395	139
644	S104	4380	269
645	S105	4365	139
646	S106	4350	269
647	S107	4335	139
648	S108	4320	269
649	S109	4305	139
650	S110	4290	269
651	S111	4275	139
652	S112	4260	269
653	S113	4245	139
654	S114	4230	269
655	S115	4215	139
656	S116	4200	269
657	S117	4185	139
658	S118	4170	269
659	S119	4155	139
660	S120	4140	269
661	S121	4125	139
662	S122	4110	269
663	S123	4095	139
664	S124	4080	269
665	S125	4065	139
666	S126	4050	269
667	S127	3540	269
668	S128	3525	139
669	S129	3510	269
670	S130	3495	139
671	S131	3480	269
672	S132	3465	139
673	S133	3450	269
674	S134	3435	139
675	S135	3420	269
676	S136	3405	139
677	S137	3390	269
678	S138	3375	139
679	S139	3360	269
680	S140	3345	139
681	S141	3330	269
682	S142	3315	139
683	S143	3300	269
684	S144	3285	139
685	S145	3270	269
686	S146	3255	139
687	S147	3240	269
688	S148	3225	139
689	S149	3210	269
690	S150	3195	139
691	S151	3180	269
692	S152	3165	139
693	S153	3150	269
694	S154	3135	139
695	S155	3120	269
696	S156	3105	139
697	S157	3090	269
698	S158	3075	139
699	S159	3060	269
700	S160	3045	139
701	S161	3030	269
702	S162	3015	139
703	S163	3000	269
704	S164	2985	139
705	S165	2970	269
706	S166	2955	139
707	S167	2940	269
708	S168	2925	139
709	S169	2910	269
710	S170	2895	139
711	S171	2880	269
712	S172	2865	139
713	S173	2850	269
714	S174	2835	139

No.	PIN Name	X	Y	No.	PIN Name	X	Y	No.	PIN Name	X	Y
715	S175	2820	269	750	S210	2295	139	785	S245	1770	269
716	S176	2805	139	751	S211	2280	269	786	S246	1755	139
717	S177	2790	269	752	S212	2265	139	787	S247	1740	269
718	S178	2775	139	753	S213	2250	269	788	S248	1725	139
719	S179	2760	269	754	S214	2235	139	789	S249	1710	269
720	S180	2745	139	755	S215	2220	269	790	S250	1695	139
721	S181	2730	269	756	S216	2205	139	791	S251	1680	269
722	S182	2715	139	757	S217	2190	269	792	S252	1665	139
723	S183	2700	269	758	S218	2175	139	793	S253	1650	269
724	S184	2685	139	759	S219	2160	269	794	S254	1635	139
725	S185	2670	269	760	S220	2145	139	795	S255	1620	269
726	S186	2655	139	761	S221	2130	269	796	S256	1605	139
727	S187	2640	269	762	S222	2115	139	797	S257	1590	269
728	S188	2625	139	763	S223	2100	269	798	S258	1575	139
729	S189	2610	269	764	S224	2085	139	799	S259	1560	269
730	S190	2595	139	765	S225	2070	269	800	S260	1545	139
731	S191	2580	269	766	S226	2055	139	801	S261	1530	269
732	S192	2565	139	767	S227	2040	269	802	S262	1515	139
733	S193	2550	269	768	S228	2025	139	803	S263	1500	269
734	S194	2535	139	769	S229	2010	269	804	S264	1485	139
735	S195	2520	269	770	S230	1995	139	805	S265	1470	269
736	S196	2505	139	771	S231	1980	269	806	S266	1455	139
737	S197	2490	269	772	S232	1965	139	807	S267	1440	269
738	S198	2475	139	773	S233	1950	269	808	S268	1425	139
739	S199	2460	269	774	S234	1935	139	809	S269	1410	269
740	S200	2445	139	775	S235	1920	269	810	S270	1395	139
741	S201	2430	269	776	S236	1905	139	811	S271	1380	269
742	S202	2415	139	777	S237	1890	269	812	S272	1365	139
743	S203	2400	269	778	S238	1875	139	813	S273	1350	269
744	S204	2385	139	779	S239	1860	269	814	S274	1335	139
745	S205	2370	269	780	S240	1845	139	815	S275	1320	269
746	S206	2355	139	781	S241	1830	269	816	S276	1305	139
747	S207	2340	269	782	S242	1815	139	817	S277	1290	269
748	S208	2325	139	783	S243	1800	269	818	S278	1275	139
749	S209	2310	269	784	S244	1785	139	819	S279	1260	269

No.	PIN Name	X	Y
820	S280	1245	139
821	S281	1230	269
822	S282	1215	139
823	S283	1200	269
824	S284	1185	139
825	S285	1170	269
826	S286	1155	139
827	S287	1140	269
828	S288	1125	139
829	S289	1110	269
830	S290	1095	139
831	S291	1080	269
832	S292	1065	139
833	S293	1050	269
834	S294	1035	139
835	S295	1020	269
836	S296	1005	139
837	S297	990	269
838	S298	975	139
839	S299	960	269
840	S300	945	139
841	S301	930	269
842	S302	915	139
843	S303	900	269
844	S304	885	139
845	S305	870	269
846	S306	855	139
847	S307	840	269
848	S308	825	139
849	S309	810	269
850	S310	795	139
851	S311	780	269
852	S312	765	139
853	S313	750	269
854	S314	735	139
855	S315	720	269
856	S316	705	139
857	S317	690	269
858	S318	675	139
859	S319	660	269
860	S320	645	139
861	S321	630	269
862	S322	615	139
863	S323	600	269
864	S324	585	139
865	S325	570	269
866	S326	555	139
867	S327	540	269
868	S328	525	139
869	S329	510	269
870	S330	495	139
871	S331	480	269
872	S332	465	139
873	S333	450	269
874	S334	435	139
875	S335	420	269
876	S336	405	139
877	S337	390	269
878	S338	375	139
879	S339	360	269
880	S340	345	139
881	S341	330	269
882	S342	315	139
883	S343	300	269
884	S344	285	139
885	S345	270	269
886	S346	255	139
887	S347	240	269
888	S348	225	139
889	S349	210	269
890	S350	195	139
891	S351	180	269
892	S352	165	139
893	S353	150	269
894	S354	135	139
895	S355	120	269
896	S356	105	139
897	S357	90	269
898	S358	75	139
899	S359	60	269
900	S360	45	139
901	DUMMY	30	269
902	DUMMY	15	139
903	DUMMY	0	269
904	DUMMY	-15	139
905	DUMMY	-30	269
906	S361	-45	139
907	S362	-60	269
908	S363	-75	139
909	S364	-90	269
910	S365	-105	139
911	S366	-120	269
912	S367	-135	139
913	S368	-150	269
914	S369	-165	139
915	S370	-180	269
916	S371	-195	139
917	S372	-210	269
918	S373	-225	139
919	S374	-240	269
920	S375	-255	139
921	S376	-270	269

No.	PIN Name	X	Y
922	S377	-285	139
923	S378	-300	269
924	S379	-315	139
925	S380	-330	269
926	S381	-345	139
927	S382	-360	269
928	S383	-375	139
929	S384	-390	269
930	S385	-405	139
931	S386	-420	269
932	S387	-435	139
933	S388	-450	269
934	S389	-465	139
935	S390	-480	269
936	S391	-495	139
937	S392	-510	269
938	S393	-525	139
939	S394	-540	269
940	S395	-555	139
941	S396	-570	269
942	S397	-585	139
943	S398	-600	269
944	S399	-615	139
945	S400	-630	269
946	S401	-645	139
947	S402	-660	269
948	S403	-675	139
949	S404	-690	269
950	S405	-705	139
951	S406	-720	269
952	S407	-735	139
953	S408	-750	269
954	S409	-765	139
955	S410	-780	269
956	S411	-795	139
957	S412	-810	269
958	S413	-825	139
959	S414	-840	269
960	S415	-855	139
961	S416	-870	269
962	S417	-885	139
963	S418	-900	269
964	S419	-915	139
965	S420	-930	269
966	S421	-945	139
967	S422	-960	269
968	S423	-975	139
969	S424	-990	269
970	S425	-1005	139
971	S426	-1020	269
972	S427	-1035	139
973	S428	-1050	269
974	S429	-1065	139
975	S430	-1080	269
976	S431	-1095	139
977	S432	-1110	269
978	S433	-1125	139
979	S434	-1140	269
980	S435	-1155	139
981	S436	-1170	269
982	S437	-1185	139
983	S438	-1200	269
984	S439	-1215	139
985	S440	-1230	269
986	S441	-1245	139
987	S442	-1260	269
988	S443	-1275	139
989	S444	-1290	269
990	S445	-1305	139
991	S446	-1320	269
992	S447	-1335	139
993	S448	-1350	269
994	S449	-1365	139
995	S450	-1380	269
996	S451	-1395	139
997	S452	-1410	269
998	S453	-1425	139
999	S454	-1440	269
1000	S455	-1455	139
1001	S456	-1470	269
1002	S457	-1485	139
1003	S458	-1500	269
1004	S459	-1515	139
1005	S460	-1530	269
1006	S461	-1545	139
1007	S462	-1560	269
1008	S463	-1575	139
1009	S464	-1590	269
1010	S465	-1605	139
1011	S466	-1620	269
1012	S467	-1635	139
1013	S468	-1650	269
1014	S469	-1665	139
1015	S470	-1680	269
1016	S471	-1695	139
1017	S472	-1710	269
1018	S473	-1725	139
1019	S474	-1740	269
1020	S475	-1755	139
1021	S476	-1770	269
1022	S477	-1785	139
1023	S478	-1800	269

No.	PIN Name	X	Y
1024	S479	-1815	139
1025	S480	-1830	269
1026	S481	-1845	139
1027	S482	-1860	269
1028	S483	-1875	139
1029	S484	-1890	269
1030	S485	-1905	139
1031	S486	-1920	269
1032	S487	-1935	139
1033	S488	-1950	269
1034	S489	-1965	139
1035	S490	-1980	269
1036	S491	-1995	139
1037	S492	-2010	269
1038	S493	-2025	139
1039	S494	-2040	269
1040	S495	-2055	139
1041	S496	-2070	269
1042	S497	-2085	139
1043	S498	-2100	269
1044	S499	-2115	139
1045	S500	-2130	269
1046	S501	-2145	139
1047	S502	-2160	269
1048	S503	-2175	139
1049	S504	-2190	269
1050	S505	-2205	139
1051	S506	-2220	269
1052	S507	-2235	139
1053	S508	-2250	269
1054	S509	-2265	139
1055	S510	-2280	269
1056	S510	-2295	139
1057	S512	-2310	269
1058	S513	-2325	139
1059	S514	-2340	269
1060	S515	-2355	139
1061	S516	-2370	269
1062	S517	-2385	139
1063	S518	-2400	269
1064	S519	-2415	139
1065	S520	-2430	269
1066	S521	-2445	139
1067	S522	-2460	269
1068	S523	-2475	139
1069	S524	-2490	269
1070	S525	-2505	139
1071	S526	-2520	269
1072	S527	-2535	139
1073	S528	-2550	269
1074	S529	-2565	139
1075	S530	-2580	269
1076	S531	-2595	139
1077	S532	-2610	269
1078	S533	-2625	139
1079	S534	-2640	269
1080	S535	-2655	139
1081	S536	-2670	269
1082	S537	-2685	139
1083	S538	-2700	269
1084	S539	-2715	139
1085	S540	-2730	269
1086	S541	-2745	139
1087	S542	-2760	269
1088	S543	-2775	139
1089	S544	-2790	269
1090	S545	-2805	139
1091	S546	-2820	269
1092	S547	-2835	139
1093	S548	-2850	269
1094	S549	-2865	139
1095	S550	-2880	269
1096	S551	-2895	139
1097	S552	-2910	269
1098	S553	-2925	139
1099	S554	-2940	269
1100	S555	-2955	139
1101	S556	-2970	269
1102	S557	-2985	139
1103	S558	-3000	269
1104	S559	-3015	139
1105	S560	-3030	269
1106	S561	-3045	139
1107	S562	-3060	269
1108	S563	-3075	139
1109	S564	-3090	269
1110	S565	-3105	139
1111	S566	-3120	269
1112	S567	-3135	139
1113	S568	-3150	269
1114	S569	-3165	139
1115	S570	-3180	269
1116	S571	-3195	139
1117	S572	-3210	269
1118	S573	-3225	139
1119	S574	-3240	269
1120	S575	-3255	139
1121	S576	-3270	269
1122	S577	-3285	139
1123	S578	-3300	269
1124	S579	-3315	139
1125	S580	-3330	269

No.	PIN Name	X	Y
1126	S581	-3345	139
1127	S582	-3360	269
1128	S583	-3375	139
1129	S584	-3390	269
1130	S585	-3405	139
1131	S586	-3420	269
1132	S587	-3435	139
1133	S588	-3450	269
1134	S589	-3465	139
1135	S590	-3480	269
1136	S591	-3495	139
1137	S592	-3510	269
1138	S593	-3525	139
1139	S594	-3540	269
1140	S595	-3555	139
1141	S596	-3570	269
1142	S597	-3585	139
1143	S598	-3600	269
1144	S599	-3615	139
1145	S600	-3630	269
1146	S601	-3645	139
1147	S602	-3660	269
1148	S603	-3675	139
1149	S604	-3690	269
1150	S605	-3705	139
1151	S606	-3720	269
1152	S607	-3735	139
1153	S608	-3750	269
1154	S609	-3765	139
1155	S610	-3780	269
1156	S611	-3795	139
1157	S612	-3810	269
1158	S613	-3825	139
1159	S614	-3840	269
1160	S615	-3855	139
1161	S616	-3870	269
1162	S617	-3885	139
1163	S618	-3900	269
1164	S619	-3915	139
1165	S620	-3930	269
1166	S621	-3945	139
1167	S622	-3960	269
1168	S623	-3975	139
1169	S624	-3990	269
1170	S625	-4005	139
1171	S626	-4020	269
1172	S627	-4035	139
1173	S628	-4050	269
1174	S629	-4065	139
1175	S630	-4080	269
1176	S631	-4095	139
1177	S632	-4110	269
1178	S633	-4125	139
1179	S634	-4140	269
1180	S635	-4155	139
1181	S636	-4170	269
1182	S637	-4185	139
1183	S638	-4200	269
1184	S639	-4215	139
1185	S640	-4230	269
1186	S641	-4245	139
1187	S642	-4260	269
1188	S643	-4275	139
1189	S644	-4290	269
1190	S645	-4305	139
1191	S646	-4320	269
1192	S647	-4335	139
1193	S648	-4350	269
1194	S649	-4365	139
1195	S650	-4380	269
1196	S651	-4395	139
1197	S652	-4410	269
1198	S653	-4425	139
1199	S654	-4440	269
1200	S655	-4455	139
1201	S656	-4470	269
1202	S657	-4485	139
1203	S658	-4500	269
1204	S659	-4515	139
1205	S660	-4530	269
1206	S661	-4545	139
1207	S662	-4560	269
1208	S663	-4575	139
1209	S664	-4590	269
1210	S665	-4605	139
1211	S666	-4620	269
1212	S667	-4635	139
1213	S668	-4650	269
1214	S669	-4665	139
1215	S670	-4680	269
1216	S671	-4695	139
1217	S672	-4710	269
1218	S673	-4725	139
1219	S674	-4740	269
1220	S675	-4755	139
1221	S676	-4770	269
1222	S677	-4785	139
1223	S678	-4800	269
1224	S679	-4815	139
1225	S680	-4830	269
1226	S681	-4845	139
1227	S682	-4860	269

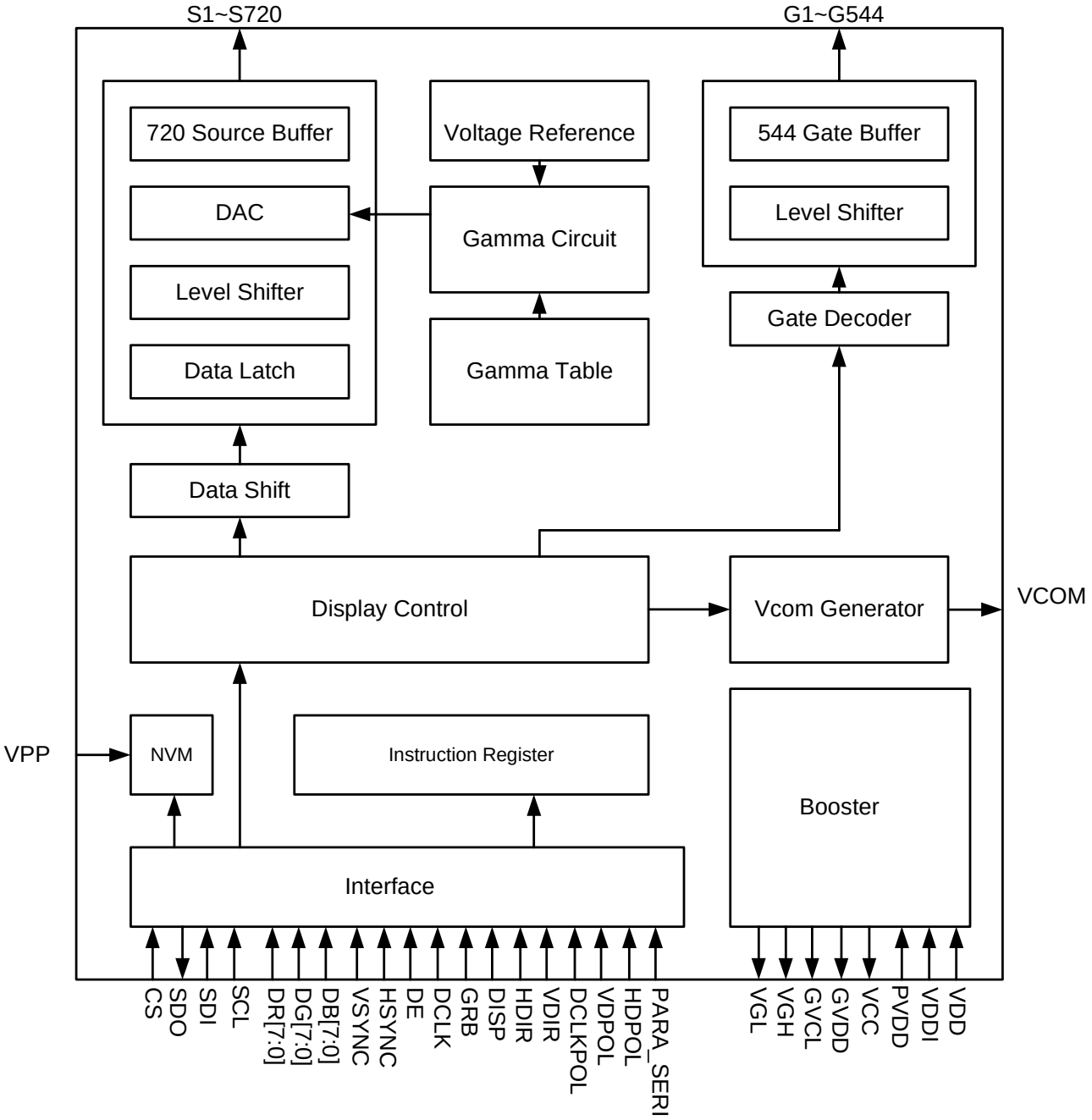
No.	PIN Name	X	Y
1228	S683	-4875	139
1229	S684	-4890	269
1230	S685	-4905	139
1231	S686	-4920	269
1232	S687	-4935	139
1233	S688	-4950	269
1234	S689	-4965	139
1235	S690	-4980	269
1236	S691	-4995	139
1237	S692	-5010	269
1238	S693	-5025	139
1239	S694	-5040	269
1240	S695	-5055	139
1241	S696	-5070	269
1242	S697	-5085	139
1243	S698	-5100	269
1244	S699	-5115	139
1245	S700	-5130	269
1246	S701	-5145	139
1247	S702	-5160	269
1248	S703	-5175	139
1249	S704	-5190	269
1250	S705	-5205	139
1251	S706	-5220	269
1252	S707	-5235	139
1253	S708	-5250	269
1254	S709	-5265	139
1255	S710	-5280	269
1256	S711	-5295	139
1257	S712	-5310	269
1258	S713	-5325	139
1259	S714	-5340	269
1260	S715	-5355	139
1261	S716	-5370	269
1262	S717	-5385	139
1263	S718	-5400	269
1264	S719	-5415	139
1265	S720	-5430	269
1266	DUMMY	-5445	139
1267	DUMMY	-5460	269
1268	DUMMY	-5475	139
1269	DUMMY	-5490	269
1270	DUMMY	-5505	139
1271	DUMMY	-5520	269
1272	G543	-5535	139
1273	G541	-5550	269
1274	G539	-5565	139
1275	G537	-5580	269
1276	G535	-5595	139
1277	G533	-5610	269
1278	G531	-5625	139
1279	G529	-5640	269
1280	G527	-5655	139
1281	G525	-5670	269
1282	G523	-5685	139
1283	G521	-5700	269
1284	G519	-5715	139
1285	G517	-5730	269
1286	G515	-5745	139
1287	G513	-5760	269
1288	G511	-5775	139
1289	G509	-5790	269
1290	G507	-5805	139
1291	G505	-5820	269
1292	G503	-5835	139
1293	G501	-5850	269
1294	G499	-5865	139
1295	G497	-5880	269
1296	G495	-5895	139
1297	G493	-5910	269
1298	G491	-5925	139
1299	G489	-5940	269
1300	G487	-5955	139
1301	G485	-5970	269
1302	G483	-5985	139
1303	G481	-6000	269
1304	G479	-6015	139
1305	G477	-6030	269
1306	G475	-6045	139
1307	G473	-6060	269
1308	G471	-6075	139
1309	G469	-6090	269
1310	G467	-6105	139
1311	G465	-6120	269
1312	G463	-6135	139
1313	G461	-6150	269
1314	G459	-6165	139
1315	G457	-6180	269
1316	G455	-6195	139
1317	G453	-6210	269
1318	G451	-6225	139
1319	G449	-6240	269
1320	G447	-6255	139
1321	G445	-6270	269
1322	G443	-6285	139
1323	G441	-6300	269
1324	G439	-6315	139
1325	G437	-6330	269
1326	G435	-6345	139
1327	G433	-6360	269
1328	G431	-6375	139
1329	G429	-6390	269

No.	PIN Name	X	Y
1330	G427	-6405	139
1331	G425	-6420	269
1332	G423	-6435	139
1333	G421	-6450	269
1334	G419	-6465	139
1335	G417	-6480	269
1336	G415	-6495	139
1337	G413	-6510	269
1338	G411	-6525	139
1339	G409	-6540	269
1340	G407	-6555	139
1341	G405	-6570	269
1342	G403	-6585	139
1343	G401	-6600	269
1344	G399	-6615	139
1345	G397	-6630	269
1346	G395	-6645	139
1347	G393	-6660	269
1348	G391	-6675	139
1349	G389	-6690	269
1350	G387	-6705	139
1351	G385	-6720	269
1352	G383	-6735	139
1353	G381	-6750	269
1354	G379	-6765	139
1355	G377	-6780	269
1356	G375	-6795	139
1357	G373	-6810	269
1358	G371	-6825	139
1359	G369	-6840	269
1360	G367	-6855	139
1361	G365	-6870	269
1362	G363	-6885	139
1363	G361	-6900	269
1364	G359	-6915	139
1365	G357	-6930	269
1366	G355	-6945	139
1367	G353	-6960	269
1368	G351	-6975	139
1369	G349	-6990	269
1370	G347	-7005	139
1371	G345	-7020	269
1372	G343	-7035	139
1373	G341	-7050	269
1374	G339	-7065	139
1375	G337	-7080	269
1376	G335	-7095	139
1377	G333	-7110	269
1378	G331	-7125	139
1379	G329	-7140	269
1380	G327	-7155	139
1381	G325	-7170	269
1382	G323	-7185	139
1383	G321	-7200	269
1384	G319	-7215	139
1385	G317	-7230	269
1386	G315	-7245	139
1387	G313	-7260	269
1388	G311	-7275	139
1389	G309	-7290	269
1390	G307	-7305	139
1391	G305	-7320	269
1392	G303	-7335	139
1393	G301	-7350	269
1394	G299	-7365	139
1395	G297	-7380	269
1396	G295	-7395	139
1397	G293	-7410	269
1398	G291	-7425	139
1399	G289	-7440	269
1400	G287	-7455	139
1401	G285	-7470	269
1402	G283	-7485	139
1403	G281	-7500	269
1404	G279	-7515	139
1405	G277	-7530	269
1406	G275	-7545	139
1407	G273	-7560	269
1408	G271	-7575	139
1409	G269	-7590	269
1410	G267	-7605	139
1411	G265	-7620	269
1412	G263	-7635	139
1413	G261	-7650	269
1414	G259	-7665	139
1415	G257	-7680	269
1416	G255	-7695	139
1417	G253	-7710	269
1418	G251	-7725	139
1419	G249	-7740	269
1420	G247	-7755	139
1421	G245	-7770	269
1422	G243	-7785	139
1423	G241	-7800	269
1424	G239	-7815	139
1425	G237	-7830	269
1426	G235	-7845	139
1427	G233	-7860	269
1428	G231	-7875	139
1429	G229	-7890	269
1430	G227	-7905	139
1431	G225	-7920	269

No.	PIN Name	X	Y
1432	G223	-7935	139
1433	G221	-7950	269
1434	G219	-7965	139
1435	G217	-7980	269
1436	G215	-7995	139
1437	G213	-8010	269
1438	G211	-8025	139
1439	G209	-8040	269
1440	G207	-8055	139
1441	G205	-8070	269
1442	G203	-8085	139
1443	G201	-8100	269
1444	G199	-8115	139
1445	G197	-8130	269
1446	G195	-8145	139
1447	G193	-8160	269
1448	G191	-8175	139
1449	G189	-8190	269
1450	G187	-8205	139
1451	G185	-8220	269
1452	G183	-8235	139
1453	G181	-8250	269
1454	G179	-8265	139
1455	G177	-8280	269
1456	G175	-8295	139
1457	G173	-8310	269
1458	G171	-8325	139
1459	G169	-8340	269
1460	G167	-8355	139
1461	G165	-8370	269
1462	G163	-8385	139
1463	G161	-8400	269
1464	G159	-8415	139
1465	G157	-8430	269
1466	G155	-8445	139
1467	G153	-8460	269
1468	G151	-8475	139
1469	G149	-8490	269
1470	G147	-8505	139
1471	G145	-8520	269
1472	G143	-8535	139
1473	G141	-8550	269
1474	G139	-8565	139
1475	G137	-8580	269
1476	G135	-8595	139
1477	G133	-8610	269
1478	G131	-8625	139
1479	G129	-8640	269
1480	G127	-8655	139
1481	G125	-8670	269
1482	G123	-8685	139
1483	G121	-8700	269
1484	G119	-8715	139
1485	G117	-8730	269
1486	G115	-8745	139
1487	G113	-8760	269
1488	G111	-8775	139
1489	G109	-8790	269
1490	G107	-8805	139
1491	G105	-8820	269
1492	G103	-8835	139
1493	G101	-8850	269
1494	G99	-8865	139
1495	G97	-8880	269
1496	G95	-8895	139
1497	G93	-8910	269
1498	G91	-8925	139
1499	G89	-8940	269
1500	G87	-8955	139
1501	G85	-8970	269
1502	G83	-8985	139
1503	G81	-9000	269
1504	G79	-9015	139
1505	G77	-9030	269
1506	G75	-9045	139
1507	G73	-9060	269
1508	G71	-9075	139
1509	G69	-9090	269
1510	G67	-9105	139
1511	G65	-9120	269
1512	G63	-9135	139
1513	G61	-9150	269
1514	G59	-9165	139
1515	G57	-9180	269
1516	G55	-9195	139
1517	G53	-9210	269
1518	G51	-9225	139
1519	G49	-9240	269
1520	G47	-9255	139
1521	G45	-9270	269
1522	G43	-9285	139
1523	G41	-9300	269
1524	G39	-9315	139
1525	G37	-9330	269
1526	G35	-9345	139
1527	G33	-9360	269
1528	G31	-9375	139
1529	G29	-9390	269
1530	G27	-9405	139
1531	G25	-9420	269
1532	G23	-9435	139
1533	G21	-9450	269

No.	PIN Name	X	Y
1534	G19	-9465	139
1535	G17	-9480	269
1536	G15	-9495	139
1537	G13	-9510	269
1538	G11	-9525	139
1539	G9	-9540	269
1540	G7	-9555	139
1541	G5	-9570	269
1542	G3	-9585	139
1543	G1	-9600	269
1544	DUMMY	-9615	139
1545	DUMMY	-9630	269
1546	DUMMY	-9645	139
1547	DUMMY	-9660	269
	L_MARK	-9605	-142.5
	R_MARK	9605	-142.5

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 Pin Function

Name	Type	Description
CS	I	Serial communication chip select, Internal pull-low.
SDI	I	Serial communication data input, Internal pull-high.
SDO	O	Serial communication data output.
SCL	I	Serial communication clock input, Internal pull-high.
PARA_SERI	I	PARA_SERI=”Low”: Serial 8-bit RGB input through DR0~DR7. PARA_SERI=”High”: Parallel 24-bit RGB input through DR0~DR7, DB0~DB7, DG0~DG7
DR0~DR7	I	8-bit digital Red data input.
DG0~DG7	I	8-bit digital GREEN data input
DB0~DB7	I	8-bit digital BLUE data input.
DCLK	I	Clock signal, latching data at falling.
HSYNC	I	Horizontal sync signal. Default negative polarity. When not used in DE mode, user should connect it to “Low”.
VSYNC	I	Vertical sync signal. Default negative polarity. When not used in DE mode, user should connect it to “Low”.
DE	I	Data input enable. Default active high to enable the data input When not used in SYNC mode, user should connect it to “Low”.
HDIR	I	Horizontal scan direction control. HDIR = “Low” : Shift from right to left. HDIR = “High”: Shift from left to right. When not used, user should connect it to “High” (Please refer to the register setting : HDIR)
VDIR	I	Vertical scan direction control. VDIR = “Low”: Shift from down to up. VDIR = “High”: Shift from up to down. When not used, user should connect it to “High” (Please refer to the register setting : VDIR)
DCLKPOL	I	DCLK polarity control. DCLKPOL=”Low”, positive polarity DCLKPOL=” High”, negative polarity When not used, user should connect it to “High” (Please refer to the register setting : DCLKPOL)

Name	Type	Description
VDPOL	I	VSYNC polarity control. VDPOL="Low", positive polarity VDPOL="High", negative polarity When not used, user should connect it to "High" (Please refer to the register setting : VDPOL)
HDPOL	I	HSYNC polarity control. HDPOL="Low", positive polarity HDPOL=" High", negative polarity When not used, user should connect it to "High" (Please refer to the register setting : HDPOL)
SBGR	I	Data R[7:0] & B[7:0] exchanged internally. SBGR="0" R[7:0]→R[7:0] B[7:0]→B[7:0]. SBGR="1" R[7:0]→B[7:0] B[7:0]→R[7:0].
GRB	I	Global reset. Active low. Internal pull-high
DISP	I	Display control / standby mode selection. Internal pull-high. DISP = "Low" : Standby; DISP = "High" : Normal display
MVA_TN	I	LC type selection. MVA_TN = "Low": Panel display is normally white MVA_TN = "High": Panel display is normally black (Please refer to the register setting : MVA_TN)
RES	I	Resolution select signal. Internal pull-high. RES="Low": 480RGB x 240 RES="High": 480RGB x 272
EXTC	I	OTP trim function control. Internal pull-low. This pin should be floating for enabling the function of auto-refresh register. EXTC = "Low": Disable OTP trim function and enable register refresh automatically. EXTC = "High": Enable OTP trim function and disable register refresh automatically.
Source / Gate Driver		
S1~S720	O	Source driver output signals
G1~G544	O	Gate driver output signals
VCOM Generator		
VCOM	O	A power supply for the TFT-LCD common electrode. Frame polarity output for VCOM.

Power Supply		
VDD	P	Power supply for digital circuit
VDDI	P	Power supply for digital interface I/O pins
VCCA	P	Power supply for analog circuit
PVDD	P	Power supply for charge pump circuit
DGND	P	Ground pin for digital circuit
AGND	P	Ground pin for analog circuit
PGND	P	Ground pin for charge pump circuit
VPP	P	Power input pin for OTP. When writing OTP, it needs external power supply voltage (7.5V). If not used, let this pin open.
AVDD	C	A power supply pin for generating Source positive voltage. Connect a capacitor for stabilization. (Default NC).
AVDD1	C	A power supply pin for generating GVDD and positive Gamma reference voltage. Connect a capacitor for stabilization. (Default NC).
AVCL	C	A power supply pin for generating Source negative voltage. Connect a capacitor for stabilization. (Default NC).
AVCL1	C	A power supply pin for generating GVCL and positive Gamma reference voltage. Connect a capacitor for stabilization. (Default NC).
VCC	PO	Monitoring pin of internal digital power
VGH	C	Positive power supply for gate driver output. Connect a capacitor for stabilization. (default NC)
VGL	C	Negative power supply for gate driver output. Connect a capacitor for stabilization. (default NC)
GVDD	PO	A reference positive voltage of grayscale voltage generator.
GVCL	PO	A reference negative voltage of grayscale voltage generator.
Others		
VGSP	T	Internal VCOM offset monitor pin for feed-through voltage. The detail of driver output voltage relations refer to chapter 17.2
TEST_IN5 TEST_IN6	T	Test pins for internal testing only. User should leave it open or connect it to “high”.
TEST_IN[0:4]	T	Test pins for internal testing only. User should leave it open or connect it to “low”.
TESTOUT [0:7]	T	Test pins for internal testing only. User should leave it open.
DUMMY	D	Dummy pin. User should leave it open.

Note. 1. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, S: short pin, T: test pin, M: mark, C: capacitor pin

2. If unused pin don’t floating, the pin fix to VDDI or DGND.

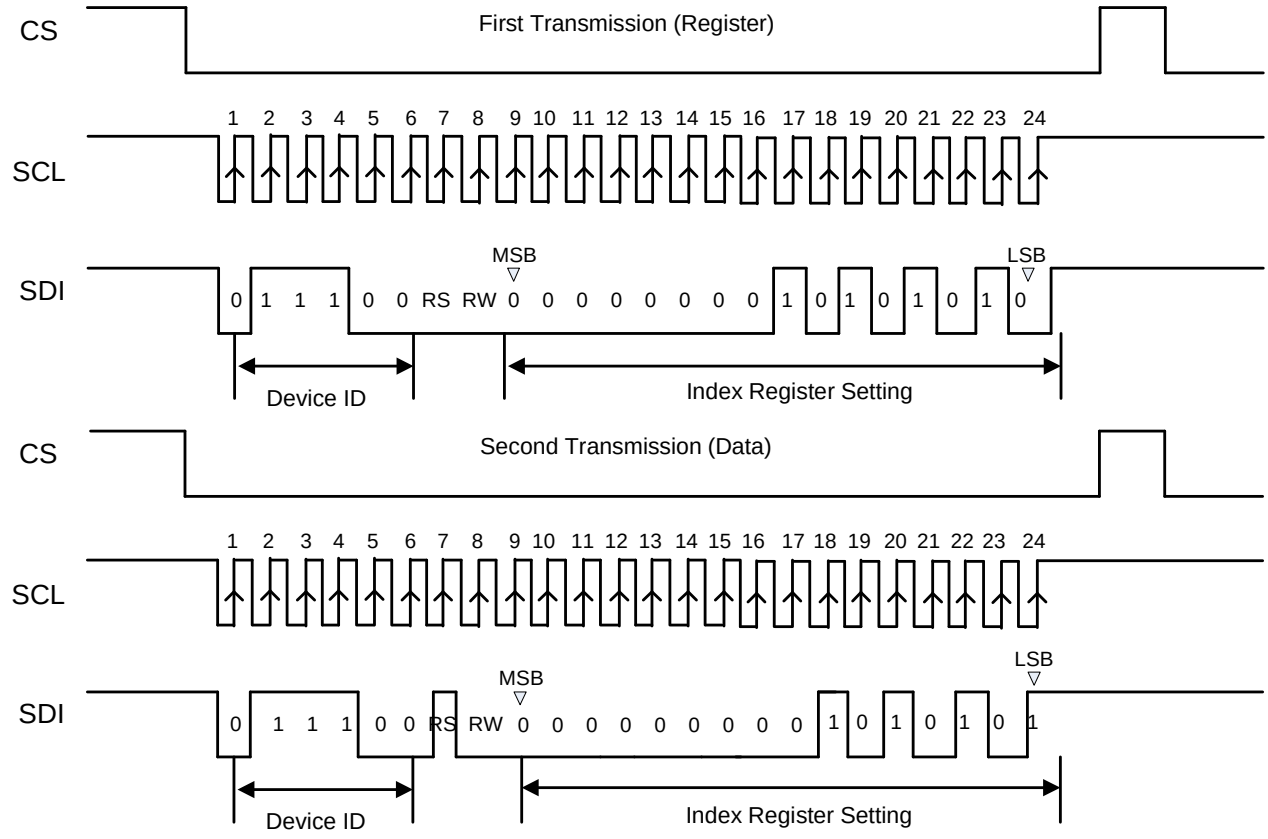
7. 3-WIRE SERIAL INTERFACE

7.1 3-wire Serial Interface

ST7257 supports 24-bit serial bus interface. 24-bit data are latched by SCL's rising edge step-by-step. Serial bus interface is active while CS=L (from CS falling to CS rising). After CS has transmitted 24 units of CLK, it has to change into high.

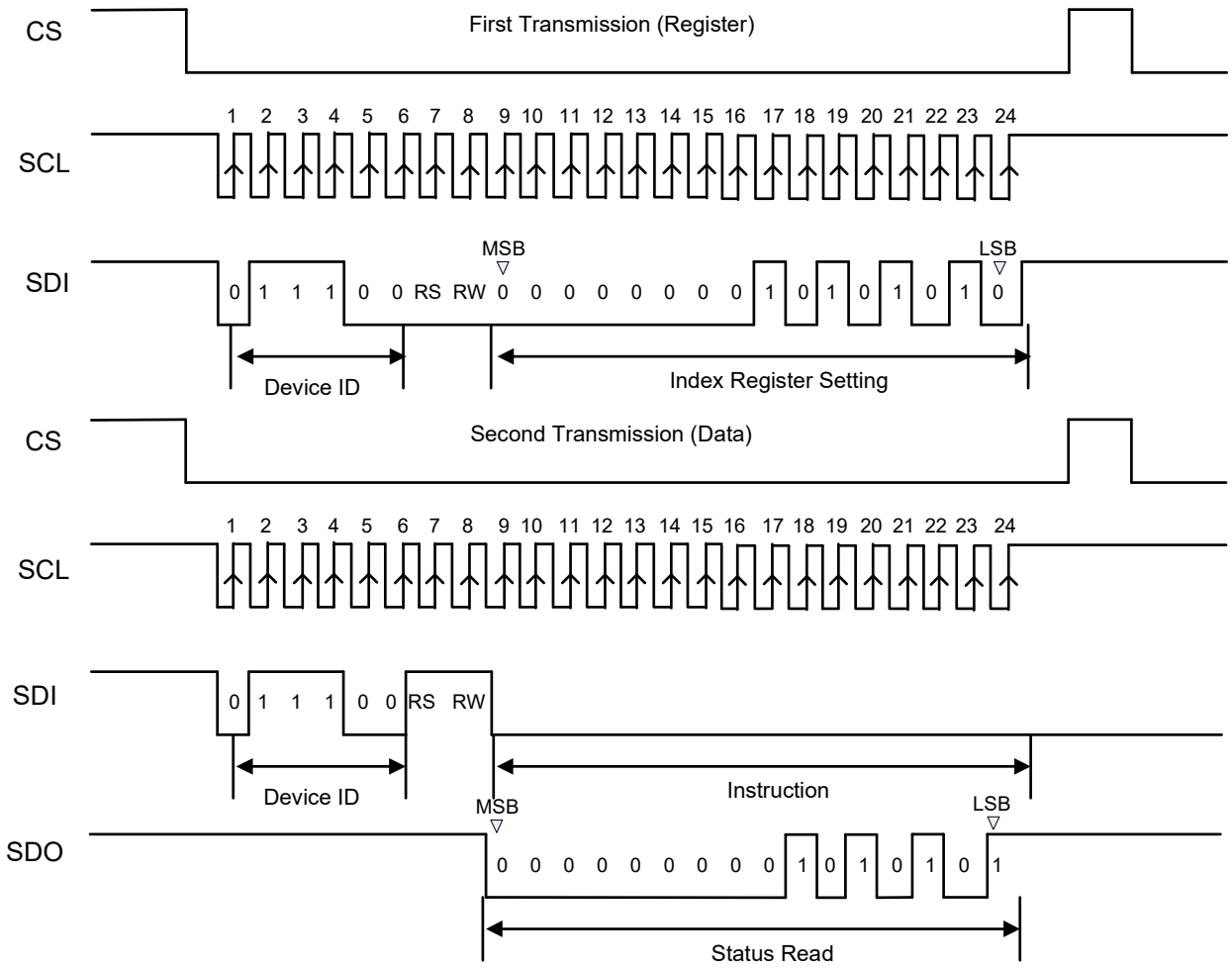
Under the standard condition, the number of SCL is 24 units. While CS=L, if SCL<24 cycles is input, then the input data won't be latched and will become invalid data. While CS=L, if SCL>24 cycles is input, the 24-bit data in front of CS rising edge will become valid.

Write Mode



Note: The example writes "0x0055h" to register 0x00AAh

Read Mode



Note: The example reads "0x0055h" from register 0x00AAh

8. REGISTER LIST

8.1 Register Summary

COMMAND TABLE1										
No.	TYP	B7	B6	B5	B4	B3	B2	B1	B0	Default
R0	R/W	-	VDIR	HDIR	-	-	-	-	-	60h
R1	R/W	-	-	-	-	GRB	-	-	DISP	08h
R2	R/W	CONTRAST								40h
R3	R/W	-	SUB_CONTRAST_R							40h
R4	R/W	-	SUB_CONTRAST_B							40h
R5	R/W	BRIGHTNESS								40h
R6	R/W	-	SUB_BRIGHTNESS_R							40h
R7	R/W	-	SUB_BRIGHTNESS_B							40h
R8	R/W	H_BLANKING								2Bh
R9	R/W	VDPOL	HDPOL	VBLANKING						CCh
R10	R/W	-	DCLKPOL	-	-	-	-	-	-	40h
R15	R/W	-	-	-	PARA_SERI	DE_POL	1	MVA_TN	BGR	1Ch
R69	R/W	1	1	1	1	ENABLE	SPARE[2]	SPARE[1]	SPARE[0]	FCh
R7F	W	-	-	-	-	-	-	-	CMD2_EN	00h
COMMAND TABLE2										
No.	TYP	B7	B6	B5	B4	B3	B2	B1	B0	Default
R20	R/W	PKP7[4]	PKP6[4]	PKP5[4]	PKP4[4]	PKP3[4]	PKP2[4]	PKP1[4]	PKP0[4]	--
R21	R/W	PKP15[1]	PKP15[0]	PKP14[1]	PKP14[0]	VOS0P[4]	VRF0P[4]	PKP9[4]	PKP8[4]	--
R22	R/W	PKP1[3:0]				PKP0[3:0]				--
R23	R/W	PKP3[3:0]				PKP2[3:0]				--
R24	R/W	PKP5[3:0]				PKP4[3:0]				--
R25	R/W	PKP7[3:0]				PKP6[3:0]				--
R26	R/W	PKP9[3:0]				PKP8[3:0]				--
R27	R/W	VOS0P[3:0]				VRF0P[3:0]				--
R28	R/W	-	PKP11[2]	PKP11[1]	PKP11[0]	-	PKP10[2]	PKP10[1]	PKP10[0]	--
R29	R/W	-	PKP13[2]	PKP13[1]	PKP13[0]	-	PKP12[2]	PKP12[1]	PKP12[0]	--
R30	R/W	PKN7[4]	PKN6[4]	PKN5[4]	PKN4[4]	PKN3[4]	PKN2[4]	PKN1[4]	PKN0[4]	--
R31	R/W	PKN15[1]	PKN15[0]	PKN14[1]	PKN14[0]	VOS0N[4]	VRF0N[4]	PKN9[4]	PKN8[4]	--
R32	R/W	PKN1[3:0]				PKN0[3:0]				--
R33	R/W	PKN3[3:0]				PKN2[3:0]				--
R34	R/W	PKN5[3:0]				PKN4[3:0]				--
R35	R/W	PKN7[3:0]				PKN6[3:0]				--
R36	R/W	PKN9[3:0]				PKN8[3:0]				--
R37	R/W	VOS0N[3:0]				VRF0N[3:0]				--

R38	R/W	-	PKN11[2]	PKN11[1]	PKN11[0]	-	PKN10[2]	PKN10[1]	PKN10[0]	--
R39	R/W	-	PKN13[2]	PKN13[1]	PKN13[0]	-	PKN12[2]	PKN12[1]	PKN12[0]	--
R40	R/W	VMF_SET	VMF[6:0]							--
R46	R/W	-	Parallel I/F GATE_WIDTH[2:0]			-	Serial I/F GATE_WIDTH[2:0]			--
R4A	W	0	0	0	0	0	0	OTP_EN	0	00h
R4B	W	0	OTP_ADDR[6:0]							00h
R4C	W	OTP_DATA[7:0]								00h
R4D	W	OTP_CONTROL[7:0]								00h
R50	R/W	-	1	VRHP[5:0]						--
R51	R/W	-	VRHN[6:0]							--
R52	R/W	1	VGSP [6:0]							--
R53	R/W	0	1	DETVDDS[1:0]		1	0	1	0	--
R54	R/W	0	0	NO[1:0]		VGLSEL[1:0]		VGHSEL[1:0]		--
R55	R/W	1	0	1	0	1	SOURCE_AP[2:0]			--
R5B	R/W	T4[1:0]		T3[1:0]		T2[1:0]		T1[1:0]		--

Note:

1.Only R40 can OTP (One Time Programmable) for adjusting flicker.

2. When GRB is low, all registers reset to default values.

3. All commands will be executed at next VSYNC.

4. Symbol "--" means this value is OTP programming setting according to the system application, panel loading and display quality.

8.2 Register Description

8.2.1 R0: Direction setting

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R0	R/W	-	VDIR	HDIR	-	-	-	-	-	60h

<table>
<tr><th>Designation</th><th>Address</th><th>Description</th></tr>
<tr><td>VDIR</td><td>R0[6]</td><td>Vertical shift direction setting
VDIR=0: Shift from down to up, last line=L1← L2…L543←L544=first line
VDIR=1: Shift from up to down, first line=L1→ L2…L543→L544=last line (default)
* Hardware pin setting (VDIR) with R0[6] interaction
<table>
<tr><th>HW PIN</th><th>SW-R0[6]</th><th>Vertical shift direction</th></tr>
<tr><td>0</td><td>0</td><td>Shift from up to down</td></tr>
<tr><td>0</td><td>1</td><td>Shift from down to up</td></tr>
<tr><td>1</td><td>0</td><td>Shift from down to up</td></tr>
<tr><td>1</td><td>1</td><td>Shift from up to down</td></tr>
</table></td></tr>
<tr><td>HDIR</td><td>R0[5]</td><td>Horizontal shift direction setting
HDIR=0: Shift from right to left, last data=Y1← Y2…Y719←Y720=first data
HDIR=1: Shift from left to right, first data=Y1→ Y2…Y719→Y720=last data (default)
* Hardware pin setting (HDIR) with R0[5] interaction
<table>
<tr><th>HW PIN</th><th>SW-R0[5]</th><th>Horizontal shift direction</th></tr>
<tr><td>0</td><td>0</td><td>Shift from left to right</td></tr>
<tr><td>0</td><td>1</td><td>Shift from right to left</td></tr>
<tr><td>1</td><td>0</td><td>Shift from right to left</td></tr>
<tr><td>1</td><td>1</td><td>Shift from left to right</td></tr>
</table></td></tr>
</table>

8.2.2 R1: GRB、DISP

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R1	R/W	-	-	-	-	GRB	-	-	DISP	08h

Designation	Address	Description
GRB	R1[3]	Register reset setting GRB=0: Reset all registers to default value GRB=1: Normal operation(default)
DISP	R1[0]	Standby(power saving) mode setting DISP=0: Standby, timing control, DAC and DC/DC converter are off. Register data should be kept (default)

		DISP=1: Normal operation with power on/off sequence

8.2.3 R2: CONTRAST

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R2	R/W	CONTRAST								40h

Designation	Address	Description
CONTRAST	R2[7:0]	RGB contrast level setting, the gain changes (1/64)/ bit CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 (default) CONTRAST=FFh: contrast gain=3.984

8.2.4 R3: SUB-CONTRAST_R

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R3	R/W	-	SUB_CONTRAST_R							40h

Designation	Address	Description
SUB_CONT RAST_R	R3[6:0]	R sub-contrast level setting, the gain changes (1/256) / bit Sub_CONTRAST_R=00h: contrast gain=0.75 Sub_CONTRAST_R=40h: contrast gain=1 (default) Sub_CONTRAST_R=7Fh: contrast gain=1.246

8.2.5 R4: SUB-CONTRAST_B

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4	R/W	-	SUB_CONTRAST_B							40h

Designation	Address	Description
SUB_CONT RAST_B	R4[6:0]	B sub-contrast level setting, the gain changes (1/256) / bit Sub_CONTRAST_B=00h: contrast gain=0.75 Sub_CONTRAST_B=40h: contrast gain=1 (default) Sub_CONTRAST_B=7Fh: contrast gain=1.246

8.2.6 R5: BRIGHTNESS

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R5	R/W	BRIGHTNESS								40h

Designation	Address	Description
BRIGHTNESS	R5[7:0]	RGB brightness level setting, the accuracy 1 step/ bit. brightness=00h: -64 brightness=40h: 0 (default) brightness=FFh: +191

8.2.7 R6: SUB-BRIGHTNESS_R

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R6	R/W	-	SUB_BRIGHTNESS_R							40h

Designation	Address	Description
SUB_BRIG HTNESS_R	R6[6:0]	R sub-brightness level setting, the accuracy 1 step / bit. SUB_BRIGHTNESS_R=00h: -64 SUB_BRIGHTNESS_R=40h: 0 (default) SUB_BRIGHTNESS_R=7Fh: +63

8.2.8 R7: SUB-BRIGHTNESS_B

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R7	R/W	-	SUB_BRIGHTNESS_B							40h

Designation	Address	Description
SUB_BRIG HTNESS_B	R7[6:0]	B sub-brightness level setting, the accuracy 1 step / bit. SUB_BRIGHTNESS_B=00h: -64 SUB_BRIGHTNESS_B=40h: 0 (default) SUB_BRIGHTNESS_B=7Fh: +63

8.2.9 R8: H_BLANKING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R8	R/W	H_BLANKING								2Bh

Designation	Address	Description
H_BLANKING	R8[7:0]	HSYNC back porch setting (unit: DCLK) H_BLANKING=00h: 0 H_BLANKING=2Bh: 43(default) H_BLANKING=FFh: 255

8.2.10 R9: VDPOL、HDPOL、V_BLANKING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R9	R/W	VDPOL	HDPOL	V_BLANKING						CCh

<table>
<tr><th>Designation</th><th>Address</th><th>Description</th></tr>
<tr><td>VDPOL</td><td>R9[7]</td><td>VSYNC polarity selection
VDPOL=0: Positive polarity
VDPOL=1: Negative polarity (default)
* The VSYNC interaction of hardware pin with software register.
<table>
<tr><th>VDPOL
(HW PIN)</th><th>VDPOL-R9[7]
(SW register)</th><th>VSYNC Polarity</th></tr>
<tr><td>0</td><td>0</td><td>Negative</td></tr>
<tr><td>0</td><td>1</td><td>Positive</td></tr>
<tr><td>1</td><td>0</td><td>Positive</td></tr>
<tr><td>1</td><td>1</td><td>Negative</td></tr>
</table></td></tr>
<tr><td>HDPOL</td><td>R9[6]</td><td>HSYNC polarity selection
HDPOL=0: Positive polarity
HDPOL=1: Negative polarity (default)
* The HSYNC interaction of hardware pin with software register
<table>
<tr><th>VDPOL
(HW PIN)</th><th>VDPOL-R9[6]
(SW register)</th><th>HSYNC Polarity</th></tr>
<tr><td>0</td><td>0</td><td>Negative</td></tr>
<tr><td>0</td><td>1</td><td>Positive</td></tr>
<tr><td>1</td><td>0</td><td>Positive</td></tr>
<tr><td>1</td><td>1</td><td>Negative</td></tr>
</table></td></tr>
<tr><td>V_BLANKING</td><td>R9[5:0]</td><td>VSYNC back porch setting (unit: HSYNC)
V_BLANKING=00h: 0
V_BLANKING=0Ch: 12(default)</td></tr>
</table>

		V_BLANKING=3Fh: 63

8.2.11 R10: DCLKPOL

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R10	R/W	-	DCLKPOL	-	-	-	-	-	-	40h

Designation	Address	Description
DCLKPOL	R10[6]	DCLK polarity selection DCLKPOL=0: Positive Polarity DCLKPOL=1: Negative Polarity(default) * The DCLK interaction of hardware pin with software register

DCLKPOL (HW PIN)	DCLKPOL-R10[6] (SW register)	DCLK Polarity
0	0	Negative
0	1	Positive
1	0	Positive
1	1	Negative

8.2.12 R15: DISPLAY MODE SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R15	R/W	-	-	-	PARA_SERI	DE_POL	1	MVA_TN	BGR	1Ch

Designation	Address	Description
BGR	R15[0]	Data R[7:0] & B[7:0] exchanged internally BGR="0" R[7:0]→R[7:0]B[7:0]→B[7:0] (Default) BGR="1" R[7:0]→B[7:0] B[7:0]→R[7:0]
MVA_TN	R15[1]	Set the TN or VA mode. MVA_TN=0: Panel display is normally white (Default) MVA_TN=1: Panel display is normally black * The TN or VA mode interaction of hardware pin with software register.

MVA_TN (HW PIN)	MVA_TN -R15[1] (SW register)	Panel Display Mode
0	0	TN (Normally white)
0	1	VA (Normally black)
1	0	VA (Normally black)
1	1	TN (Normally white)

DE_POL	R15[3]	DE polarity control. DE_POL="0", positive polarity

		DE_POL=”1”, negative polarity (Default)
PARA_SERI	R15[4]	PARA_SERI=”1”, Parallel 24-bit RGB input through DR0~DR7, DB0~DB7, DG0~DG7(Default) PARA_SERI=”0”, Serial 8-bit RGB input through DR0~DR7.

8.2.13 R69: SOURCE HOLD TIME SETTING

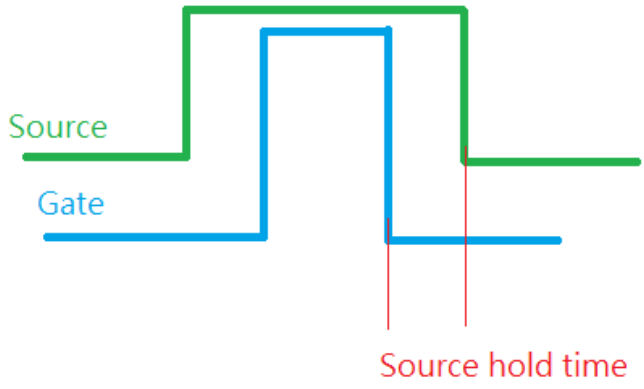
Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R69	R/W	1	1	1	1	ENABLE	SPARE[2]	SPARE[1]	SPARE[0]	FCh

Designation	Address	Description
ENABLE	R69[3]	ENABLE =1: Enable SOURCE HOLD TIME SETTING function.
SPARE[2:0]	R69[2:0]	In parallel Interface, the SOURCE HOLD TIME SETTING is below:

ENABLE	SPARE[2]	SPARE[1]	SPARE[0]	dclk duration
1	1	0	0	30 dclk
1	1	0	1	70 dclk
1	1	1	0	80 dclk
1	1	1	1	90 dclk

In serial interface, the SOURCE HOLD TIME SETTING is below:

ENABLE	SPARE[2]	SPARE[1]	SPARE[0]	dclk duration
1	1	0	0	50 dclk
1	1	0	1	60 dclk
1	1	1	0	70 dclk
1	1	1	1	80 dclk



8.3 Command Table 2 Register Description

8.3.1 R7F: COMMAND2_ENABLE

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R7F	R/W	-	-	-	-	-	-	-	CMD2_EN	00h

Designation	Address	Description
CMD2_EN	R7F[0]	Command 1 table and Command 2 table switch CMD2_EN = 0: Command 1 table enable (Default) CMD2_EN = 1: Command 2 table enable

8.3.2 R20~R39: GAMMA SELECTION

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R20	R/W	PKP7[4]	PKP6[4]	PKP5[4]	PKP4[4]	PKP3[4]	PKP2[4]	PKP1[4]	PKP0[4]	--
R21	R/W	PKP15[1]	PKP15[0]	PKP14[1]	PKP14[0]	VOS0P[4]	VRF0P[4]	PKP9[4]	PKP8[4]	--
R22	R/W	PKP1[3:0]				PKP0[3:0]				--
R23	R/W	PKP3[3:0]				PKP2[3:0]				--
R24	R/W	-				PKP4[3:0]				--
R25	R/W	PKP7[3:0]				PKP6[3:0]				--
R26	R/W	PKP9[3:0]				PKP8[3:0]				--
R27	R/W	VOS0P[3:0]				VRF0P[3:0]				--
R28	R/W	-	PKP11[2]	PKP11[1]	PKP11[0]	-	PKP10[2]	PKP10[1]	PKP10[0]	--
R29	R/W	-	PKP13[2]	PKP13[1]	PKP13[0]	-	PKP12[2]	PKP12[1]	PKP12[0]	--
R30	R/W	PKN7[4]	PKN6[4]	PKN5[4]	PKN4[4]	PKN3[4]	PKN2[4]	PKN1[4]	PKN0[4]	--
R31	R/W	PKN15[1]	PKN15[0]	PKN14[1]	PKN14[0]	VOS0N[4]	VRF0N[4]	PKN9[4]	PKN8[4]	--
R32	R/W	PKN1[3:0]				PKN0[3:0]				--
R33	R/W	PKN3[3:0]				PKN2[3:0]				--
R34	R/W	-				PKN4[3:0]				--
R35	R/W	PKN7[3:0]				PKN6[3:0]				--
R36	R/W	PKN9[3:0]				PKN8[3:0]				--
R37	R/W	VOS0N[3:0]				VRF0N[3:0]				--
R38	R/W	-	PKN11[2]	PKN11[1]	PKN11[0]	-	PKN10[2]	PKN10[1]	PKN10[0]	--
R39	R/W	-	PKN13[2]	PKN13[1]	PKN13[0]	-	PKN12[2]	PKN12[1]	PKN12[0]	--

Designation	Address	Description
PKP0[4:0]	R20[0], R22[3:0]	V16 Gamma selection
PKN0[4:0]	R30[0], R32[3:0]	
PKP1[4:0]	R20[1], R22[7:4]	V32 Gamma selection
PKN1[4:0]	R30[1], R32[7:4]	
PKP2[4:0]	R20[2], R23[3:0]	V48 Gamma selection
PKN2[4:0]	R30[2], R33[3:0]	
PKP3[4:0]	R20[3], R23[7:4]	V80 Gamma selection
PKN3[4:0]	R30[3], R33[7:4]	
PKP4[4:0]	R20[4], R24[3:0]	V128 Gamma selection
PKPN4[4:0]	R30[4], R34[3:0]	
PKP6[4:0]	R20[6], R25[3:0]	V176 Gamma selection
PKN6[4:0]	R30[6], R35[3:0]	
PKP7[4:0]	R20[7], R25[7:4]	V208 Gamma selection
PKN7[4:0]	R30[6], R35[7:4]	
PKP8[4:0]	R21[0], R26[3:0]	V224 Gamma selection
PKN8[4:0]	R31[0], R36[3:0]	
PKP9[4:0]	R21[1], R26[7:4]	V240 Gamma selection
PKN9[4:0]	R31[1], R36[7:4]	
VRFOP[4:0]	R21[2], R27[3:0]	V8 Gamma selection

VRFON[4:0]	R21[2], R37[3:0]	
VOS0P[4:0]	R21[3], R27[7:4]	V248 Gamma selection
VOS0N [4:0]	R31[3], R37[7:4]	
PKP10[2:0]	R28[2:0]	V12 Gamma selection
PKN10[2:0]	R38[2:0]	
PKP11[2:0]	R28[6:4]	V64 Gamma selection
PKN11[2:0]	R38[6:4]	
PKP12[2:0]	R29[2:0]	V104 Gamma selection
PKN12[2:0]	R39[2:0]	
PKP13[2:0]	R29[6:4]	V244 Gamma selection
PKN13[2:0]	R39[6:4]	
PKP14[1:0]	R21[5:4]	V152 Gamma selection
PKN14[1:0]	R31[5:4]	
PKP15[1:0]	R21[7:6]	V192 Gamma selection
PKN15[1:0]	R31[7:6]	

8.3.3 R40: VMF OFFSET SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R40	R/W	VMF_SET	VMF[6:0]							--

Designation	Address	Description
VMF_SET	R40[7]	VMF_SET=0: Enable VMF setting function VMF_SET=1: Disable VMF setting function
VMF[6:0]	R40[6:0]	VMF Setting adjustment

VMF[6]	VMF[5:0]	VGSP	GVDD	GVCL
0	000000	VCOMS[6:0]+64d	VRHP[6:0]+64d	VRHN[6:0]+64d
0	000001	VCOMS[6:0]+63d	VRHP[6:0]+63d	VRHN[6:0]+63d
0	000010	VCOMS[6:0]+62d	VRHP[6:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VCOMS[6:0]+2d	VRHP[6:0]+2d	VRHN[6:0]+2d
0	111111	VCOMS[6:0]+1d	VRHP[6:0]+1d	VRHN[6:0]+1d
1	000000	VCOMS[6:0]	VRHP[6:0]	VRHN[6:0]
1	000001	VCOMS[6:0]-1d	VRHP[6:0]-1d	VRHN[6:0]-1d
1	000010	VCOMS[6:0]-2d	VRHP[6:0]-2d	VRHN[6:0]-2d
1	|	|	|	|

		1	111110	VCOMS[6:0]-62d	VRHP[6:0]-62d	VRHN[6:0]-62d
		1	111111	VCOMS[6:0]-63d	VRHP[6:0]-63d	VRHN[6:0]-63d
		Note: d=16mV				

8.3.4 R46: GATE WIDTH SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R46	R/W	-	Parallel I/F GATE_WIDTH[2:0]			-	Serial I/F GATE_WIDTH[2:0]			--

Designation	Address	Description
Parallel I/F GATE_WIDTH [2:0]	R46[6:4]	Gate width adjustment in parallel interface.

Parallel I/F GATE_WIDTH[2:0]	G(n) width: (DCLK)	G(n+1) width: (DCLK)
000	(HSYNC Period time) /2+10	(HSYNC Period time) /2-10
001	(HSYNC Period time) /2+20	(HSYNC Period time) /2-20
010	(HSYNC Period time) /2+30	(HSYNC Period time) /2-30
011	(HSYNC Period time) /2+40	(HSYNC Period time) /2-40
100	(HSYNC Period time) /2+50	(HSYNC Period time) /2-50
101	(HSYNC Period time) /2+60	(HSYNC Period time) /2-60
110	(HSYNC Period time) /2+70	(HSYNC Period time) /2-70
111	(HSYNC Period time) /2	(HSYNC Period time) /2

Gate width adjustment in serial interface.

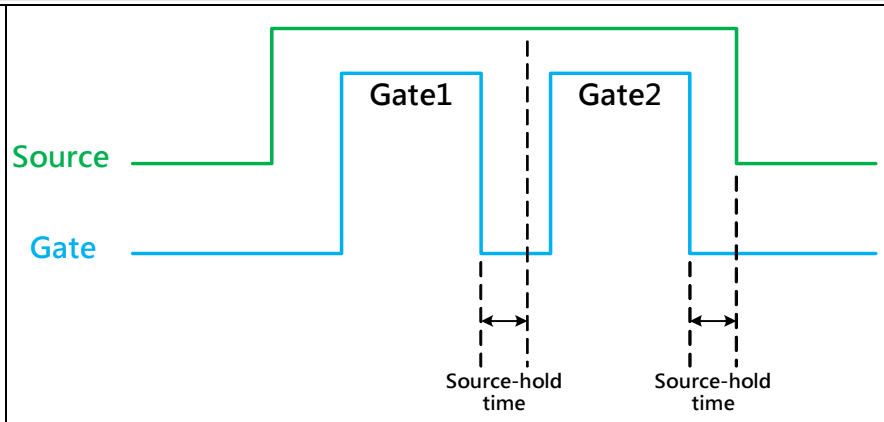
Serial I/F GATE_WIDTH [2:0]	R46[2:0]

Parallel I/F GATE_WIDTH[2:0]	G(n) width (DCLK)	G(n+1) width (DCLK)
000	(HSYNC Period time) /2+30	(HSYNC Period time) /2-30
001	(HSYNC Period time) /2+60	(HSYNC Period time) /2-60
010	(HSYNC Period time) /2+90	(HSYNC Period time) /2-90
011	(HSYNC Period time) /2+120	(HSYNC Period time) /2-120
100	(HSYNC Period time) /2+150	(HSYNC Period time) /2-150
101	(HSYNC Period time) /2+180	(HSYNC Period time) /2-180
110	(HSYNC Period time) /2+210	(HSYNC Period time) /2-210
111	(HSYNC Period time) /2	(HSYNC Period time) /2

Gate width formula:

Th (HSYNC period time)

= (Gate(n) width – source hold time) + (Gate(n+1) width – source hold time)



8.3.5 R4A: OTP FUNCTION CONTROL

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4A	W	0	0	0	0	0	0	OTP_EN	0	00h

Designation	Address	Description
OTP_EN	R4A[1]	OTP Function switch OTP_EN = 0: Disable OTP Function (default) OTP_EN = 1: Enable OTP Function

8.3.6 R4B: OTP ADDRESS SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4B	W	0	OTP_ADDR[6:0]							00h

Designation	Address	Description
OTP_ADDR	R4B[6:0]	OTP_ADDR[6:0]=0x01: VCOM Offset register OTP address.

8.3.7 R4C: OTP DATA SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4C	W	OTP_DATA[7:0]								00h

Designation	Address	Description
OTP_DATA[7:0]	R4C[7:0]	OTP DATA

8.3.8 R4D: OTP CONTROL

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R4D	W	OTP_CONTROL[7:0]								00h

Designation	Address	Description
OTP_CONTROL	R4D[7:0]	OTP_CONTROL[7:0]=0xCA: Write OTP

8.3.9 R50: GVDD SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R50	R/W	-	1	VRHP[5:0]						--

Designation	Address	Description
VRHP[5:0]	R50[5:0]	GVDD level adjustment

VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD
000000	5.9680	010000	5.7120	100000	5.4560	110000	5.2000
000001	5.9520	010001	5.6960	100001	5.4400	110001	5.1840
000010	5.9360	010010	5.6800	100010	5.4240	110010	5.1680
000011	5.9200	010011	5.6640	100011	5.4080	110011	5.1520
000100	5.9040	010100	5.6480	100100	5.3920	110100	5.1360
000101	5.8880	010101	5.6320	100101	5.3760	110101	5.1200
000110	5.8720	010110	5.6160	100110	5.3600	110110	5.1040
000111	5.8560	010111	5.6000	100111	5.3440	110111	5.0880
001000	5.8400	011000	5.5840	101000	5.3280	111000	5.0720
001001	5.8240	011001	5.5680	101001	5.3120	111001	5.0560
001010	5.8080	011010	5.5520	101010	5.2960	111010	5.0400
001011	5.7920	011011	5.5360	101011	5.2800	111011	5.0240
001100	5.7760	011100	5.5200	101100	5.2640	111100	5.0080
001101	5.7600	011101	5.5040	101101	5.2480	111101	4.9920
001110	5.7440	011110	5.4880	101110	5.2320	111110	4.9760
001111	5.7280	011111	5.4720	101111	5.2160	111111	4.9600

8.3.10 R51: GVCL SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R51	R/W	-	VRHN[6:0]							--

Designation	Address	Description
VRHN[6:0]	R51[6:0]	GVCL level adjustment

VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL
0011001	-4.4800	0110001	-4.0960	1001001	-3.7120	1100001	-3.3280
0011010	-4.4640	0110010	-4.0800	1001010	-3.6960	1100010	-3.3120
0011011	-4.448	0110011	-4.0640	1001011	-3.6800	1100011	-3.2960
0011100	-4.4320	0110100	-4.0480	1001100	-3.6640	1100100	-3.2800
0011101	-4.4160	0110101	-4.0320	1001101	-3.6480	1100101	-3.2640
0011110	-4.4000	0110110	-4.0160	1001110	-3.6320	1100110	-3.2480
0011111	-4.3840	0110111	-4.0000	1001111	-3.6160	1100111	-3.2320
0100000	-4.3680	0111000	-3.9840	1010000	-3.6000	1101000	-3.2160
0100001	-4.3520	0111001	-3.9680	1010001	-3.5840	1101001	-3.2000
0100010	-4.3360	0111010	-3.9520	1010010	-3.5680	1101010	-3.1840
0100011	-4.3200	0111011	-3.9360	1010011	-3.5520	1101011	-3.1680
0100100	-4.3040	0111100	-3.9200	1010100	-3.5360	1101100	-3.1520
0100101	-4.2880	0111101	-3.9040	1010101	-3.5200	1101101	-3.1360
0100110	-4.2720	0111110	-3.8880	1010110	-3.5040	1101110	-3.1200
0100111	-4.2560	0111111	-3.8720	1010111	-3.4880	1101111	-3.1040
0101000	-4.2400	1000000	-3.8560	1011000	-3.4720	1110000	-3.0880
0101001	-4.2240	1000001	-3.8400	1011001	-3.4560	1110001	-3.0720
0101010	-4.2080	1000010	-3.8240	1011010	-3.4400	1110010	-3.0560
0101011	-4.1920	1000011	-3.8080	1011011	-3.4240	1110011	-3.0400
0101100	-4.1760	1000100	-3.7920	1011100	-3.4080	1110100	-3.0240
0101101	-4.1600	1000101	-3.7760	1011101	-3.3920	1110101	-3.0080
0101110	-4.1440	1000110	-3.7600	1011110	-3.3760	1110110	-2.9920
0101111	-4.1280	1000111	-3.7440	1011111	-3.3600	1110111	-2.9760
0110000	-4.1120	1001000	-3.7280	1100000	-3.3440	1111000	-2.9600

8.3.11 R52: VGSP SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R52	R/W	1	VGSP[6:0]							--

Designation	Address	Description
VGSP[6:0]	R52[6:0]	VGSP level adjustment

VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP	VGSP[6:0]	VGSP
0100000	1.5520	0111000	1.1680	1010000	0.7840	1101000	0.4000
0100001	1.5360	0111001	1.1520	1010001	0.7680	1101001	0.3840
0100010	1.5200	0111010	1.1360	1010010	0.7520	1101010	0.3680
0100011	1.5040	0111011	1.1200	1010011	0.7360	1101011	0.3520
0100100	1.4880	0111100	1.1040	1010100	0.7200	1101100	0.3360
0100101	1.4720	0111101	1.0880	1010101	0.7040	1101101	0.3200
0100110	1.4560	0111110	1.0720	1010110	0.6880	1101110	0.3040
0100111	1.4400	0111111	1.0560	1010111	0.6720	1101111	0.2880
0101000	1.4240	1000000	1.0400	1011000	0.6560	1110000	0.2720
0101001	1.4080	1000001	1.0240	1011001	0.6400	1110001	0.2560
0101010	1.3920	1000010	1.0080	1011010	0.6240	1110010	0.2400
0101011	1.3760	1000011	0.9920	1011011	0.6080	1110011	0.2240
0101100	1.3600	1000100	0.9760	1011100	0.5920	1110100	0.2080
0101101	1.3440	1000101	0.9600	1011101	0.5760	1110101	0.1920
0101110	1.3280	1000110	0.9440	1011110	0.5600	1110110	0.1760
0101111	1.3120	1000111	0.9280	1011111	0.5440	1110111	0.1600
0110000	1.2960	1001000	0.9120	1100000	0.5280	1111000	0.1440
0110001	1.2800	1001001	0.8960	1100001	0.5120	1111001	0.1280
0110010	1.2640	1001010	0.8800	1100010	0.4960	1111010	0.1120
0110011	1.2480	1001011	0.8640	1100011	0.4800	1111011	0.0960
0110100	1.2320	1001100	0.8480	1100100	0.4640	1111100	0.0800
0110101	1.2160	1001101	0.8320	1100101	0.4480	1111101	0.0640
0110110	1.2000	1001110	0.8160	1100110	0.4320	1111110	0.0480
0110111	1.1840	1001111	0.8000	1100111	0.4160	1111111	0.0320

8.3.12 R53: AVDD BOOSTER SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R53	R/W	0	1	DETVDDS[1:0]		1	0	1	0	--

Designation	Address	Description
DETVDDS [1:0]	R53[5:4]	AVDD booster mode setting

DETVDDS[1]	DETVDDS[0]	AVDD booster setting
0	0	Booster : x3
0	1	Booster : x2
1	0	Auto detect function, booster will automatically set to booster x3 when VDD < 3V
1	1	Auto detect function, booster will automatically set to booster x3 when VDD < 3.1V

8.3.13 R54: NON-OVERLAP, VGH, VGL SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R54	R/W	0	0	NO[1:0]		VGLSEL[1:0]		VGHSEL[1:0]		--

Designation	Address	Description
NO[1:0]	R54[5:4]	Gate non-overlap adjustment

NO[1:0]	Non-overlap (DCLK)
00	20
01	30
10	40
11	50

VGLSEL[1:0] — R54[3:2] — VGL level adjustment

VGLSEL[1:0]	VGL(V)
00	-7
01	-8
10	-12
11	-10

VGHSEL[1:0] — R54[1:0] — VGH level adjustment

VGHSEL[1:0]	VGH(V)
00	12
01	14
10	16
11	15

8.3.14 R55: SOURCE OP-AMP POWER SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R55	R/W	1	0	1	0	1	SOURCE_AP[2:0]			--

Designation	Address	Description
SOURCE_AP [2:0]	R55[2:0]	Source driving capability selection. When setting OP capability to a higher level, the source output current will be increased.

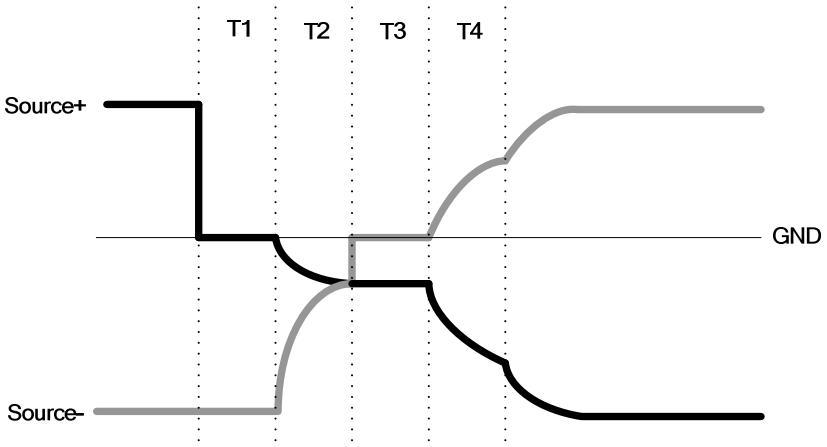
SOURCE_AP[2:0]	Source Op-amp power
000	Level1 (Least)
001	Level2 (Small)
010	Level3 (Small to Medium)
011	Level4 (Medium)
100	Level5 (Medium to Large)
101	Level6 (Large)
110	Level7 (Large to Maximum)
111	Level8 (Maximum)

Note: Setting SOURCE_AP level for turning source output current, and adjusting for a better display quality.

8.3.15 R5B: SOURCE EQUALIZE TIME SETTING

Register	TYPE	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R5B	R/W	T4[1:0]		T3[1:0]		T2[1:0]		T1[1:0]		--

Designation	Address	Description
T4[1:0] T3[1:0] T2[1:0] T1[1:0]	R5B[7:6] R5B[5:4] R5B[3:2] R5B[1:0]	Source equalizing time diagram:



Source equalizing T4 time adjustment

T4[1:0]	T4(DCLK)
00	0
01	5
10	10
11	15

Source equalizing T3 time adjustment

T3[1:0]	T3(DCLK)
00	0
01	5
10	10
11	15

Source equalizing T2 time adjustment

T2[1:0]	T2(DCLK)
00	0
01	5
10	10
11	15

Source equalizing T1 time adjustment

T1[1:0]	T1(DCLK)
00	0
01	5
10	10
11	15

Note: By the different panel condition, Adjusting source equalizing time for a better display quality.

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.6	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.6	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.6	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

1. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.

2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

3. VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)

9.2 DC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

9.2.1 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.0	3.3	3.6	V	
IO Supply Voltage	VDDI	1.65	-	VDD	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	
NVM Supply Voltage	VPP	7.4	7.5	7.6	V	

9.2.2 DC Characteristics for Digital Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-voltage power	VGH	12	15	16	V	
Negative High-voltage power	VGL	-12	-10	-7	V	
Output Voltage Deviation	Vod		±35	±45	mV	
Standby Current	Isc			50	uA	
Operation Current	Ioc		20		mA	No Load, VDD=VDDI= PVDD=3.3V @ FR=60Hz

9.3 AC Characteristics

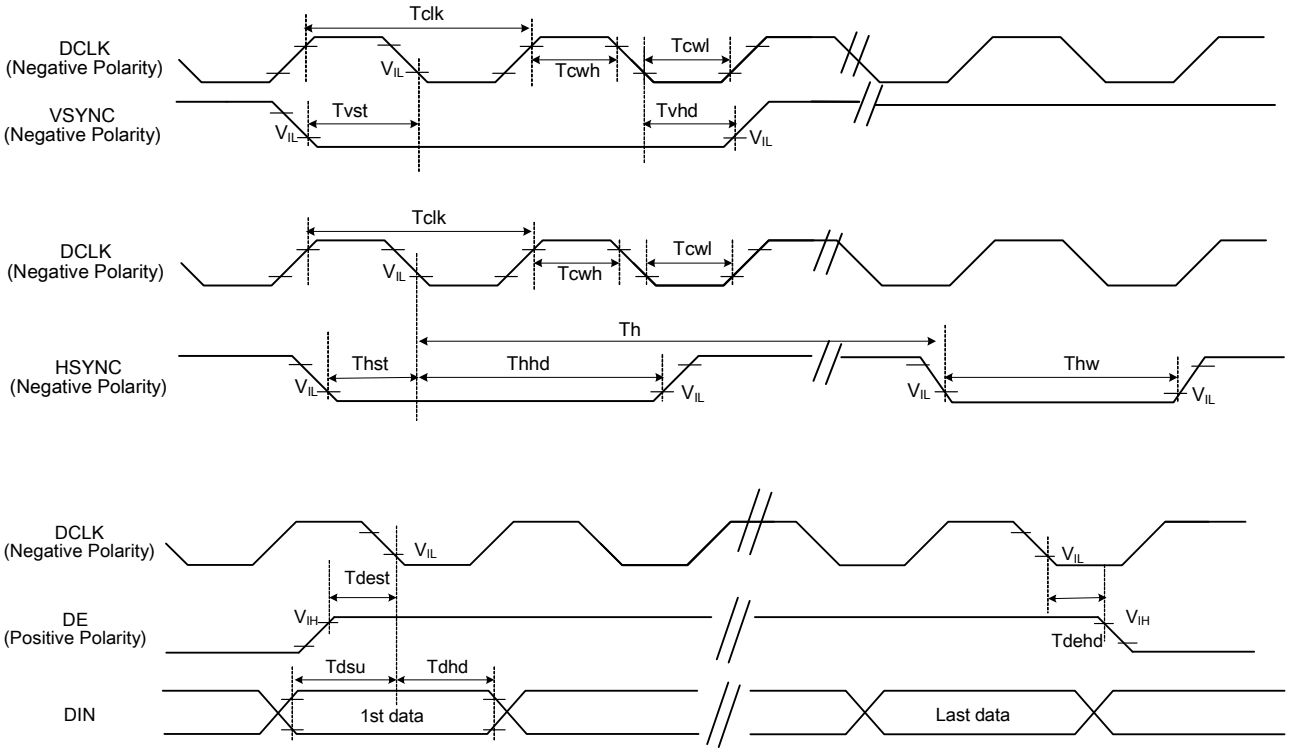
AC Electrical Characteristics (VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input/ Output timing						
CLK pulse duty	Tcw	40	50	60	%	
VSYNC setup time	Tvst	12	-	-	ns	
VSYNC hold time	Tvhd	12	-	-	ns	
HSYNC setup time	Thst	12	-	-	ns	
HSYNC hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
DE setup time	Tdest	12			ns	
DE hold time	Tdehd	12			ns	
SD output stable time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD output rise and fall time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF
3-wire serial communication						
Delay between CSB and VSYNC	Tcv	1			us	
CS input setup time	Ts0	50			ns	
Serial data input setup time	Ts1	50			ns	
CS input hold time	Th0	50			ns	
Serial data input hold time	Th1	50			ns	
SCL pulse high width	Twh1	50			ns	
SCL pulse low width	Twl1	50			ns	
CS pulse high width	Tw2	400			ns	

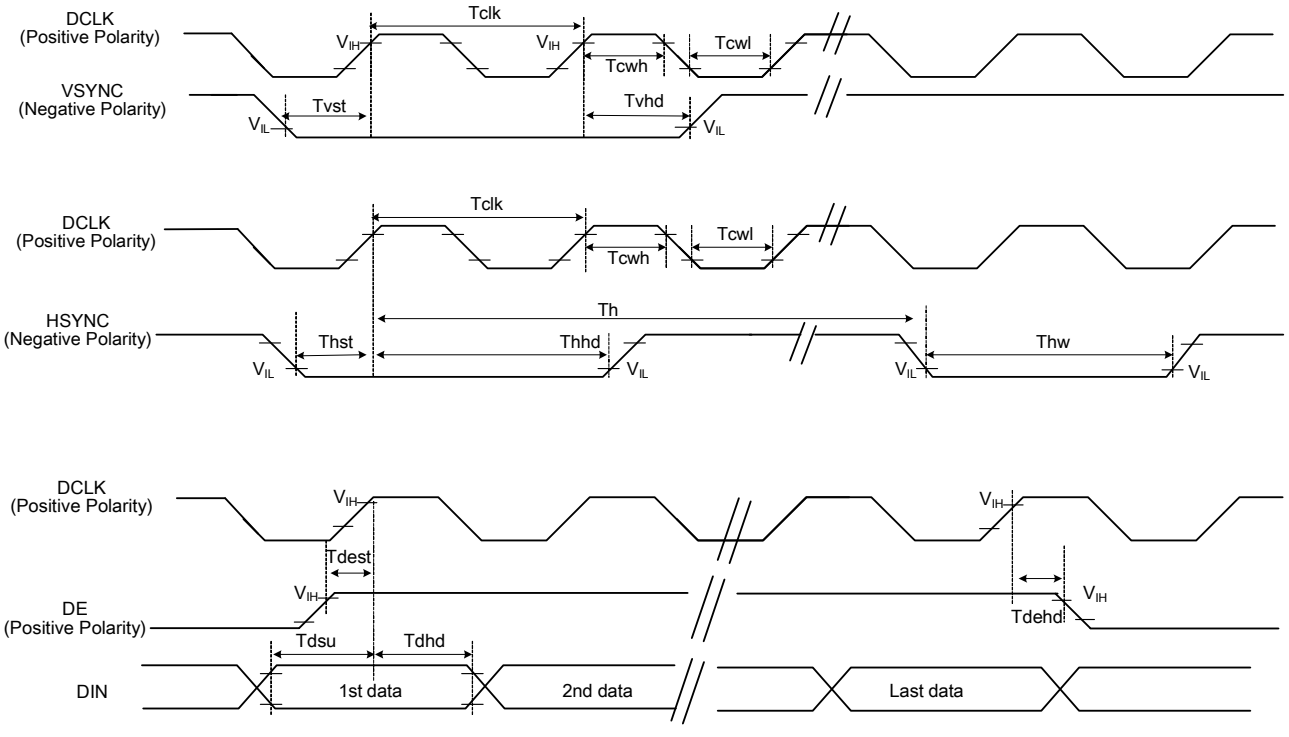
9.4 AC Timing Diagram

9.4.1 Clock and Data Input Timing Diagram

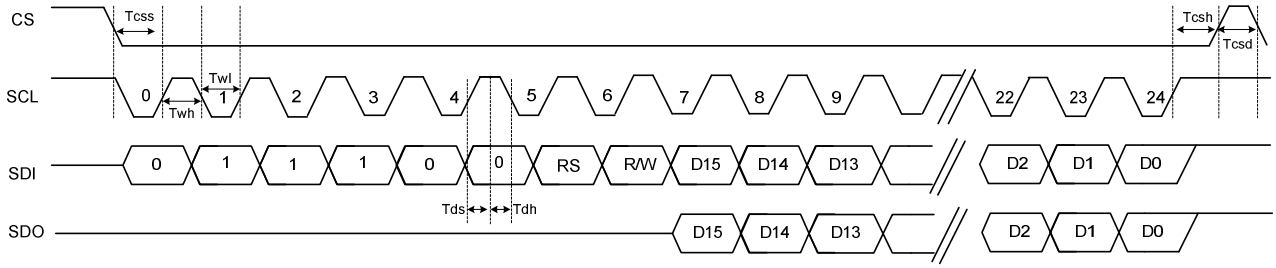
DCLK : Negative Polarity



DCLK : Positive Polarity



9.4.2 3-Wire Communication Timing Diagram



10. INPUT DATA FORMAT

10.1 RGB Input Timing Table

RGB input timing table (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C).

10.1.1 Parallel 24-bit RGB Timing Table

480RGB X 272 Resolution Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	83	111	125	ns	
HSYNC	Period Time	Th	485	531	598	DCLK	
	Display Period	Thdisp		480		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	276	292	321	H	
	Display Period	Tvdisp		272		H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	12	H	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

480RGB X 240 Resolution Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	83	111	125	ns	
HSYNC	Period Time	Th	485	531	598	DCLK	
	Display Period	Thdisp		480		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	H	
	Display Period	Tvdisp		240		H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	12	H	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

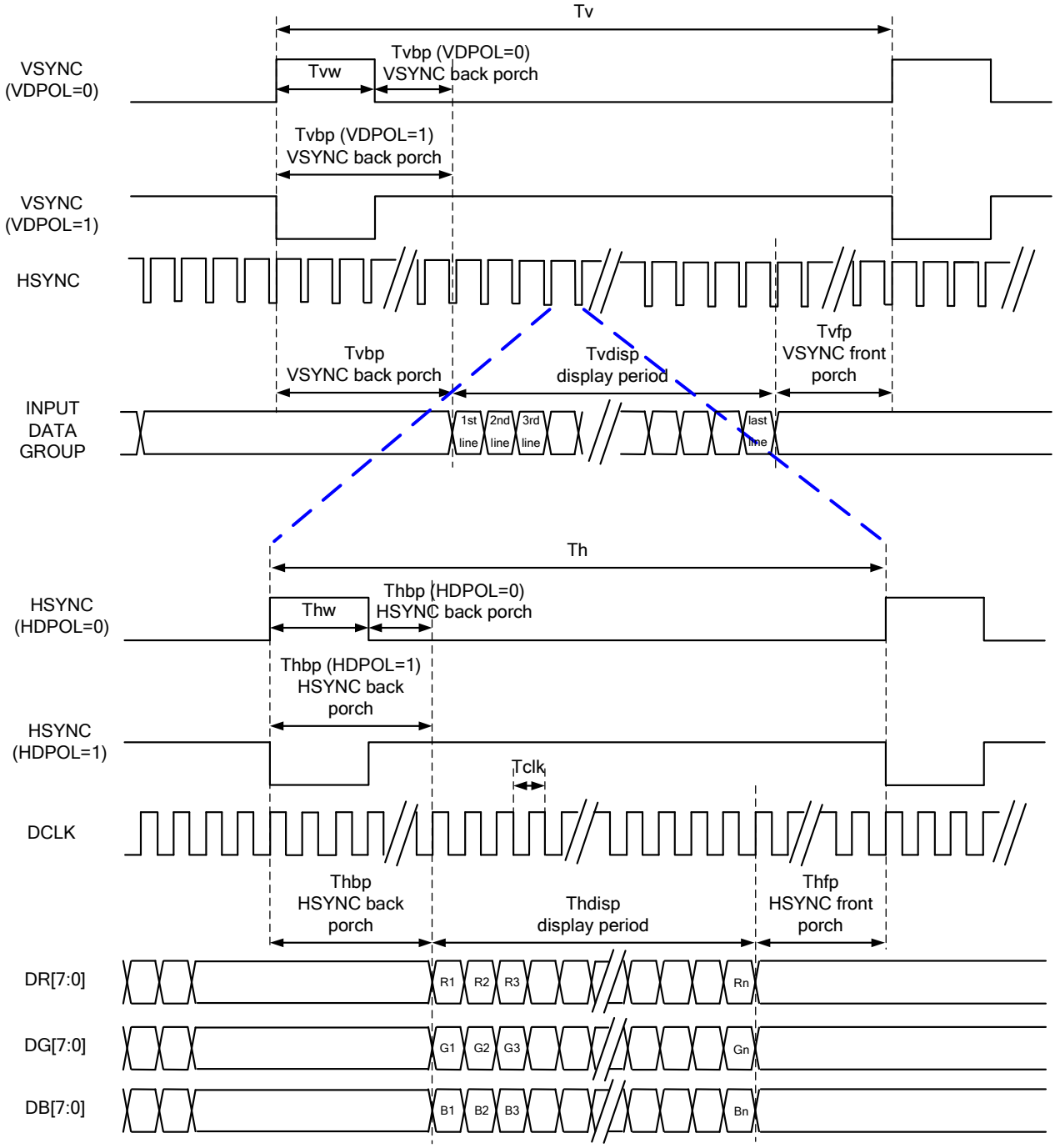
10.1.2 Serial 8-bit RGB Input Timing Table

Serial 8-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

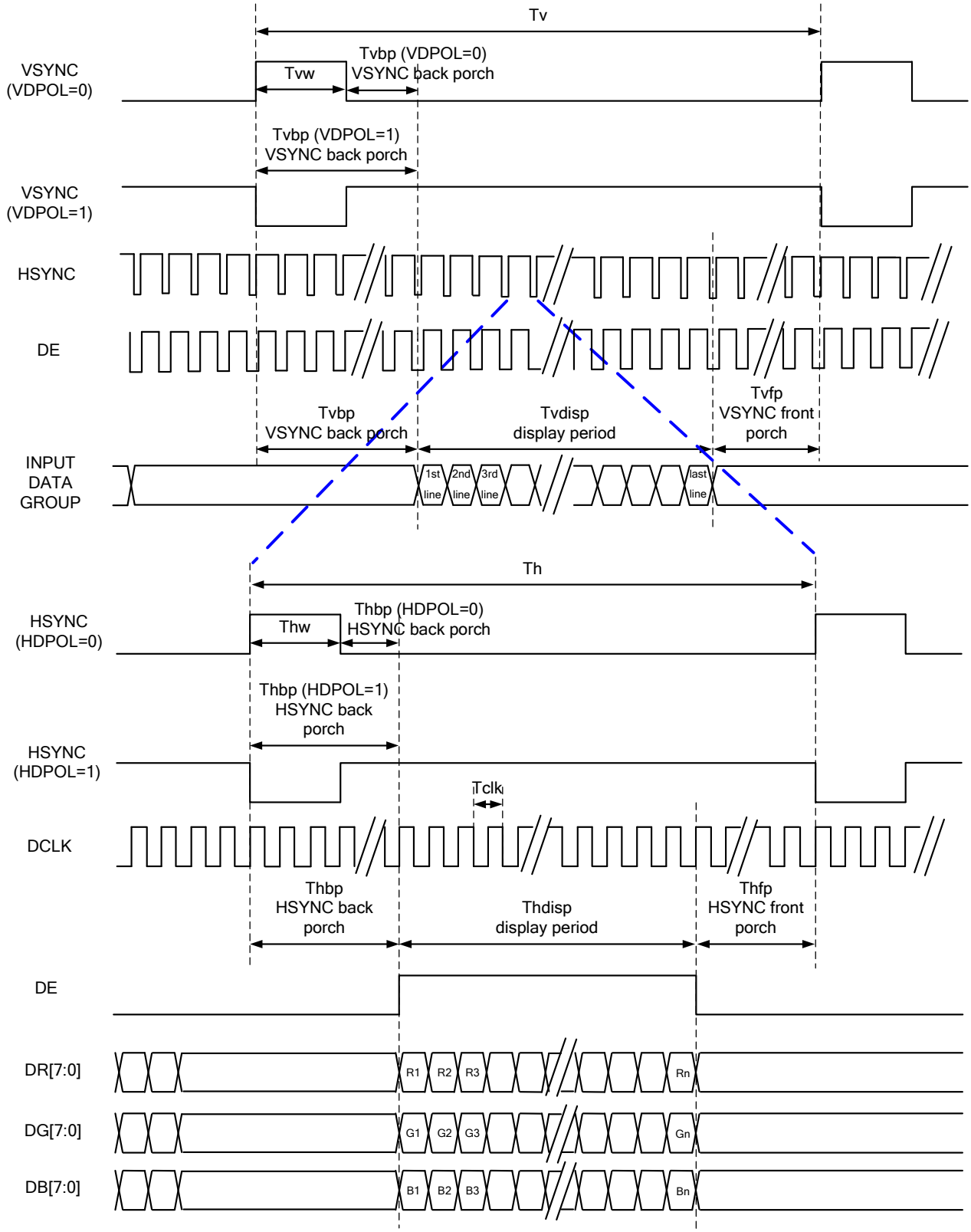
480RGB X 272 Resolution Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	24	27	30	MHz	
DCLK Period		Tclk	33	37	42	ns	
HSYNC	Period Time	Th	1445	1491	1558	DCLK	
	Display Period	Thdisp		1440		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	276	292	321	H	
	Display Period	Tvdisp		272		H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	12	H	

480RGB X 240 Resolution Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	24	27	30	MHz	
DCLK Period		Tclk	33	37	42	ns	
HSYNC	Period Time	Th	1445	1491	1558	DCLK	
	Display Period	Thdisp		1440		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	H	
	Display Period	Tvdisp		240		H	
	Back Porch	Tvbp	2	12	12	H	By V_Blanking setting
	Front Porch	Tvfp	2	8	37	H	
	Pulse Width	Tvw	2	4	12	H	

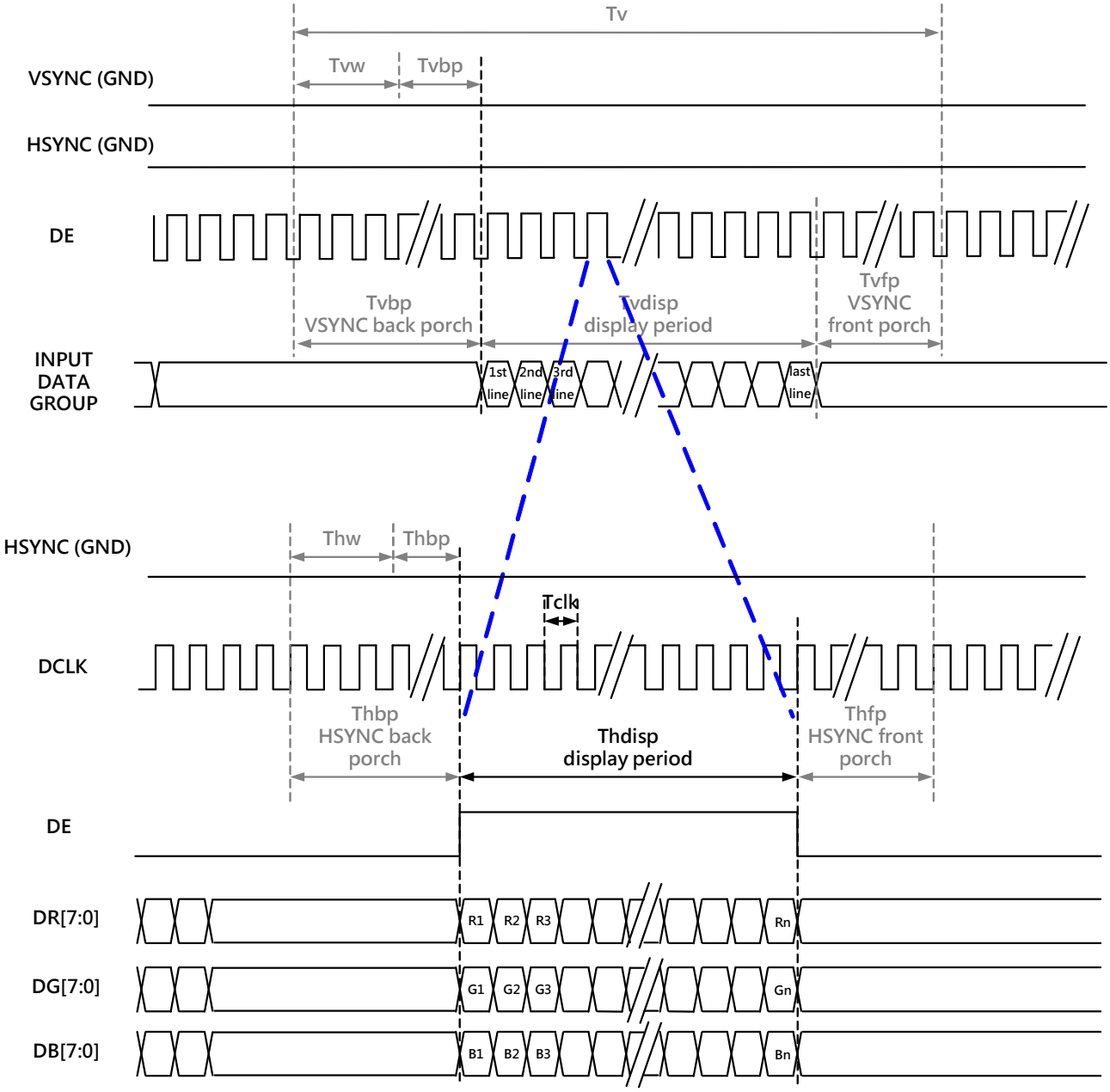
10.2 SYNC Mode Timing Diagram



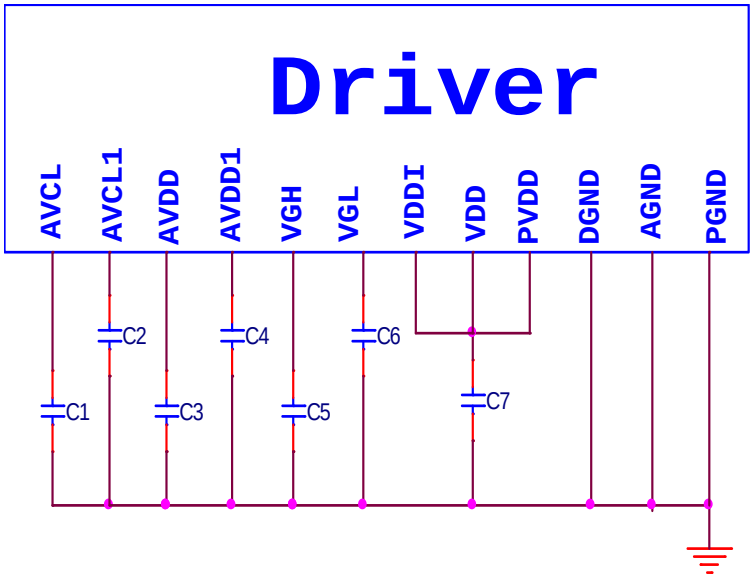
10.3 SYNC-DE Mode Timing Diagram



10.4 DE Mode Timing Diagram



11. POWER APPLICATION CIRCUIT

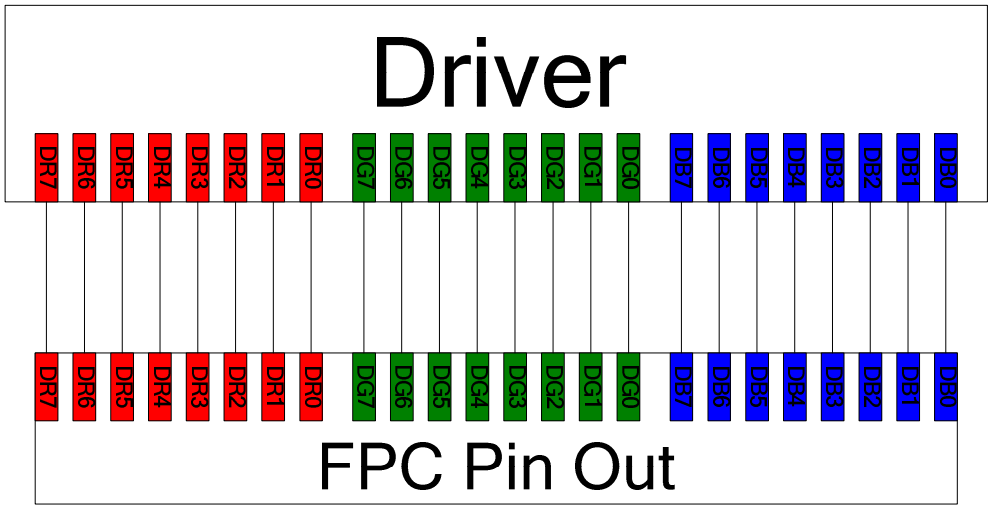


Symbol	Capacitance (uF)	Rated voltage (V)	Remarks	Note
C1	1 (default NC)	16	X7R	*1
C2	1 (default NC)	16	X7R	*1
C3	1 (default NC)	16	X7R	*1
C4	1 (default NC)	16	X7R	*1
C5	1 (default NC)	25	X7R	*1
C6	1 (default NC)	25	X7R	*1
C7	1 (default NC)	6.3	X7R	*1

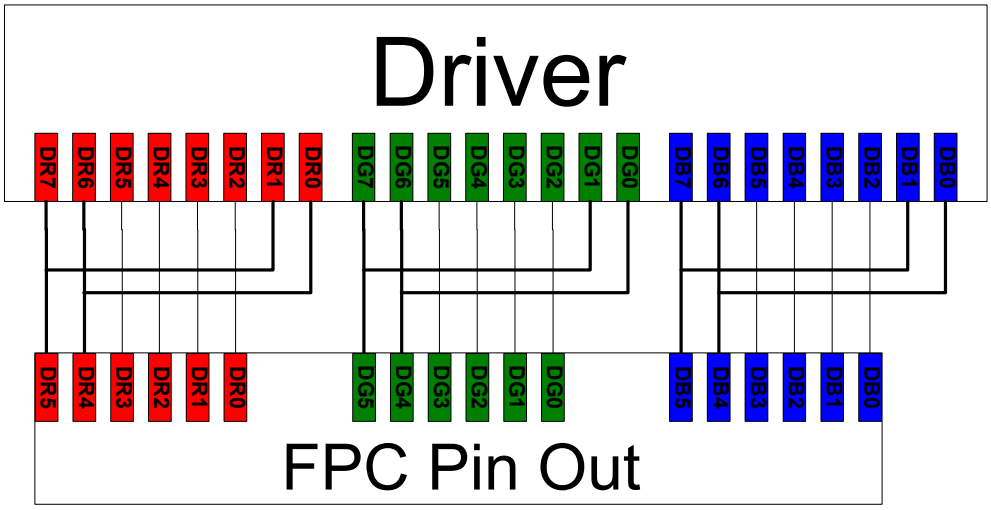
*Note: *1 The components would be needed depend on the system power, panel loading and display quality.*

12. INPUT COLOR FORMAT APPLICATION CIRCIT

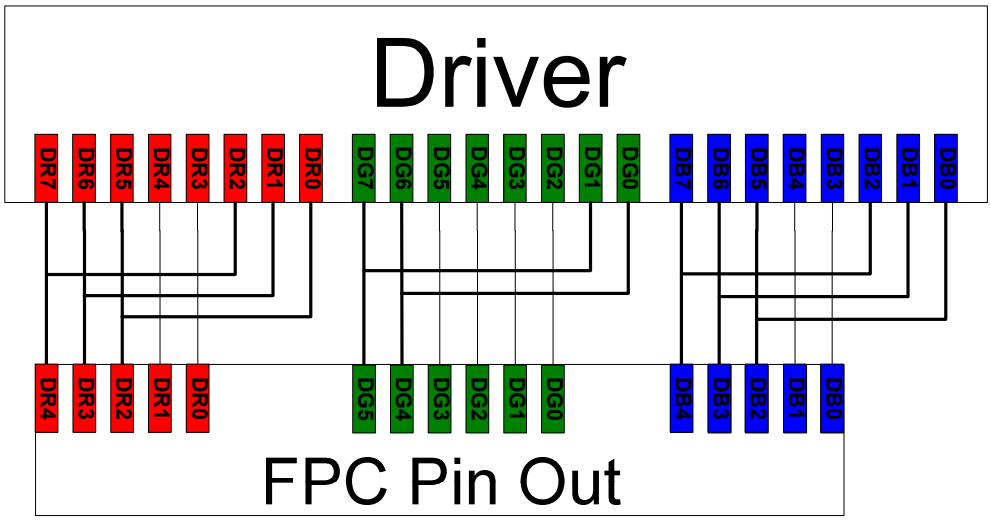
12.1 16.7M Input Color Format



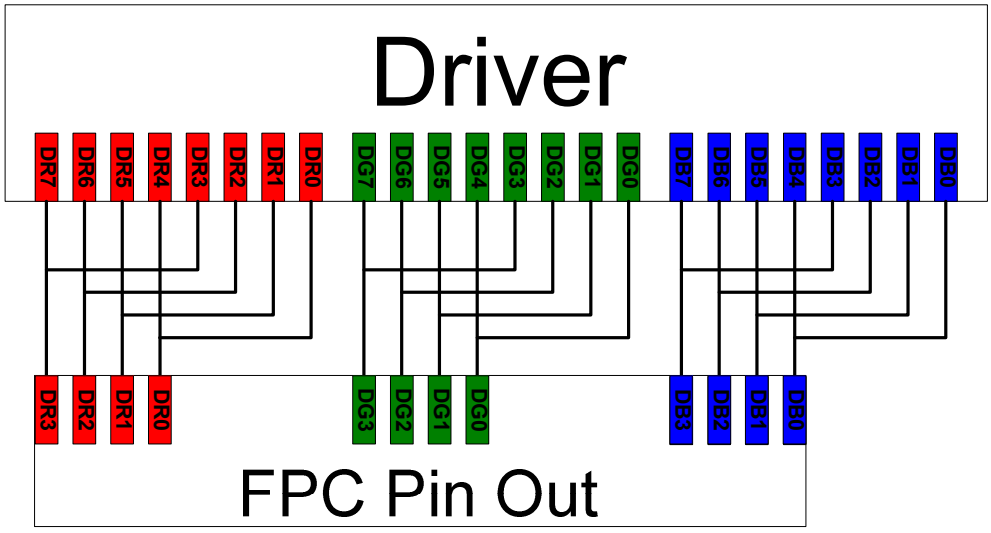
12.2 262K Input Color Format



12.3 65K Input Color Format



12.4 4K Input Color Format



13. FPC APPLICATION CIRCUIT

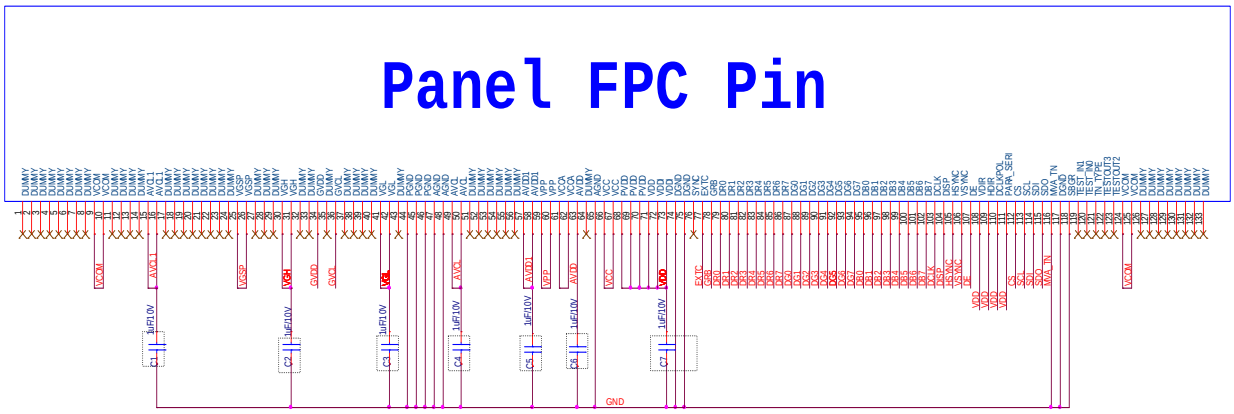
13.1 RGB Mode Selection Table

RGB Mode	DCLK	HSYNC	VSYNC	DE	DR[0:7]	DG[0:7]	DB[0:7]
Parallel RGB SYNC-DE Mode	Input	Input	Input	Input	Input	Input	Input
Parallel RGB SYNC Mode	Input	Input	Input	DGND	Input	Input	Input
Parallel RGB DE Mode	Input	DGND	DGND	Input	Input	Input	Input
Serial RGB SYNC-DE Mode	Input	Input	Input	Input	Input	DGND	DGND
Serial RGB SYNC Mode	Input	Input	Input	DGND	Input	DGND	DGND
Serial RGB DE Mode	Input	DGND	DGND	Input	Input	DGND	DGND

Input: IC input pins are driven by system RGB interface signal.

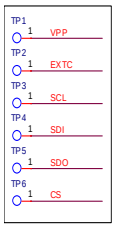
13.2 Reference Circuit

13.2.1 Parallel RGB Reference Circuit

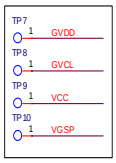


Note: *By Panel condition or system application can dummy component*

OTP Test Pad

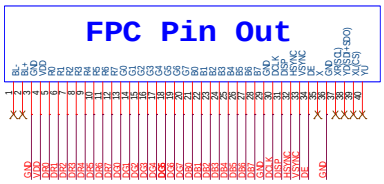


Voltage Monitor

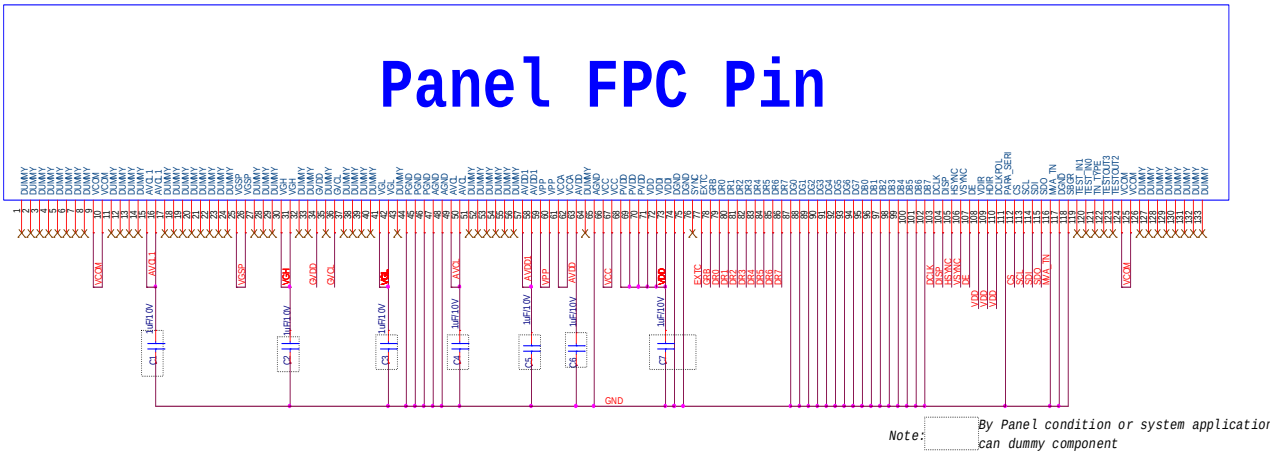


FPC Hardware Setting

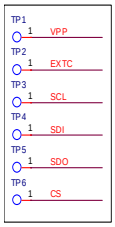
PARA_SERI="1"	Parallel 24-bit RGB
VSPOL="1"	Negative VSYNC Polarity
HSPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720
MVA_TN="0"	TN Panel

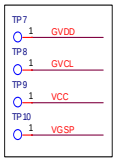


13.2.2 Serial RGB Reference Circuit

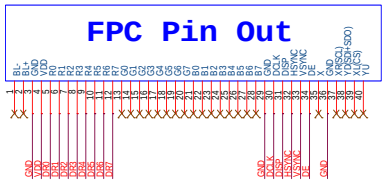


OTP Test Pad *Voltage Monitor* *FPC Hardware Setting*



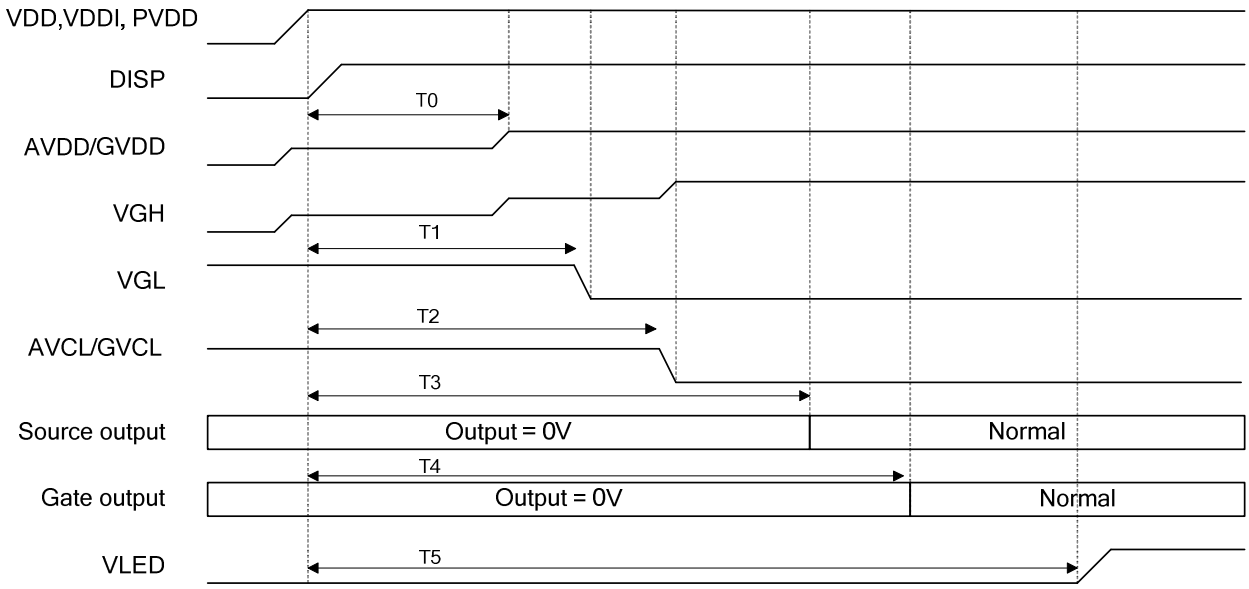


PARA_SERI="0"	Series 8-bit RGB
VDPOL="1"	Negative VSYNC Polarity
HDPOL="1"	Negative HSYNC Polarity
DCLKPOL="1"	Negative DCLK Polarity
VDIR="1"	Gate Scan direction is G1->G544
HDIR="1"	Source Scan direction is S1->S720
MVA_TN="0"	TN Panel



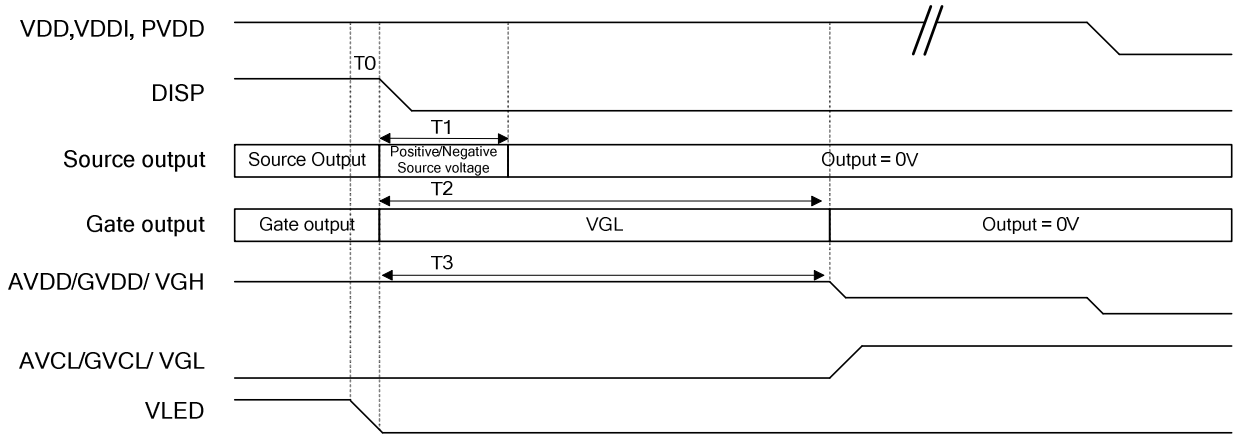
14. POWER ON/OFF SEQUENCE

14.1 Power On Sequence



Symbol	Description	Min. Time	Unit
T0	DISP=”High” to AVDD/GVDD voltage stability	40	ms
T1	DISP=”High” to VGL voltage stability	50	ms
T2	DISP=”High” to AVCL/GVCL stability	70	ms
T3	DISP=”High” to Source output	100	ms
T4	DISP=”High” to Gate output	110	ms
T5	Black Turn on	130	ms

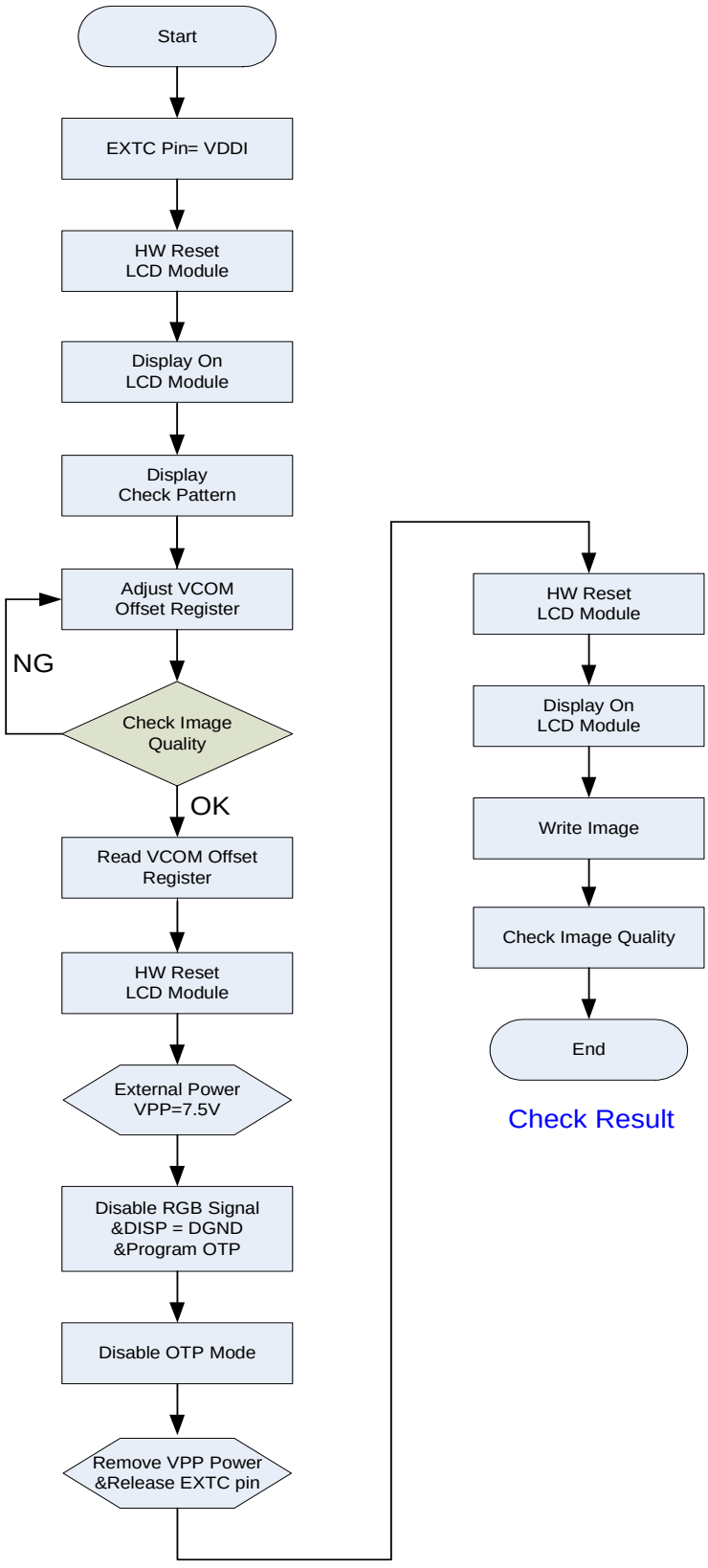
14.2 Power Off Sequence



Symbol	Description	Min. Time	Unit
T0	Backlight turn off to DISP=”Low”	5	ms
T1	DISP=”Low” to Source output disable	20	ms
T2	DISP=”Low” to Gate output disable	50	ms
T3	DISP=”Low” to Gate output disable	50	ms

15. OTP Flow

Non-Volatile Memory (OTP) can only program one time for LCD VCOM calibration .The figure below shows program flow.



Step 1: Attach LCD module on OTP programming machine.

LCD module condition	
VDD(V)	3.3
EXTC	VDDI

Step 2: Initialize the non-programmed module by software.

Function	W/R	CMD	Par	Note
HW reset	--	--	--	HW reset sequence
Waiting 100ms	--	--	--	
Display On LCD Module	--	--	--	Refer Power On Sequence
Display Check Pattern	--	--	--	Recommend Flicker Pattern
Enable Command 2	W	7F	01	
Adjust VCOM	W	40	XX	Fine tune VMF to reduce flicker

Step 3: Check the image quality of display module. If flicker can be still observed on the panel, repeat the command 40h until the flicker disappearance.

Step 4: Read Optimization VCOM Value

Function	W/R	CMD	Par	Note
Read Optimization VMF	R	40	--	VMF=Read(0x40);
Waiting 100ms				

Step 5:. HW reset LCD Module

Function	W/R	CMD	Par	Note
HW reset	--	--	--	HW reset sequence
Waiting 100ms	--	--	--	

Step 6: Hardware setting

Action	Note
RGB signal OFF	
DISP Pin = GND	
External Power 7.5V to VPP Pin	

Step 7: Enable OTP programming Mode and parameter setup

Function	W/R	CMD	Par	Note
Enable Command 2	W	7F	01	
OTP Enable	W	4A	02	
OTP parameter setup	W	4B	01	
OTP parameter setup	W	4C	VMF	
Waiting 100ms				

Step 8: Program OTP.

Function	W/R	CMD	Par	Note
OTP Write Command	W	4D	CA	Program OTP
Waiting 100ms				

Step 9: Remove 7.5V from VPP pad and EXTC=DGND.

Step 10: Disable OTP programming Mode.

Function	W/R	CMD	Par	Note
Disable OTP Programming Mode	W	4A	00	
Waiting 100ms				

Step 11: Turn off VDD and VDDI, waiting for 200ms then and turn on again.

Step 12: Execute normal display on sequence.

Function	W/R	CMD	Par	Note
HW reset	--	--	--	HW reset sequence
Waiting 100ms	--	--	--	
Display On LCD Module	--	--	--	Refer Power On Sequence
Display Check Pattern	--	--	--	Recommend Flicker Pattern

Step 13: Check the image quality.

16. RECOMMENDED PANEL ROUTING RESISTANCE

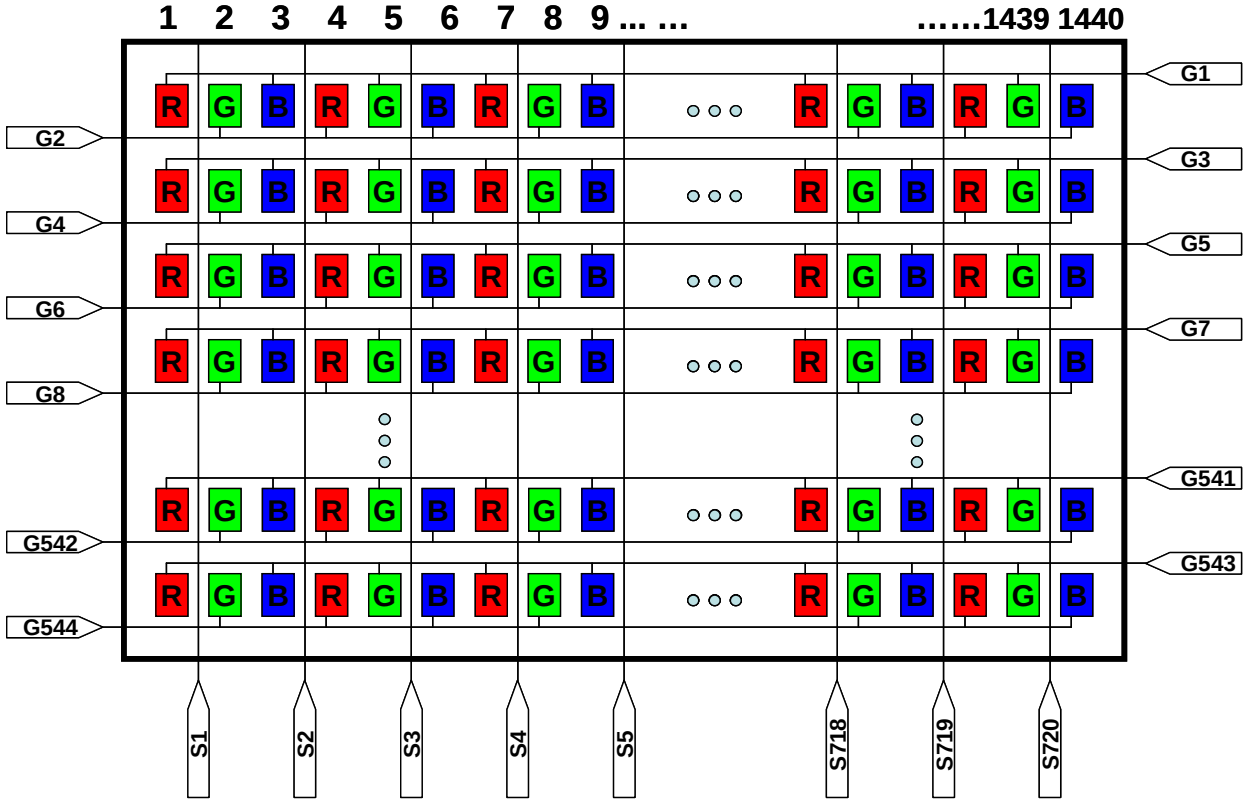
The recommended wiring resistance values are given below. The wiring resistance values affect the current ability of the power blocks and thus must be designed within the given range.

	Pin Name	Unit: ohm
1	VPP	<3
2	GVDD	<50
3	GVCL	<50
4	VCOM	<3
5	DGND	<3
6	VCC	<50
7	VDDI	<3
8	VDD	<3
9	VSYNC	<50
10	HSYNC	<50
11	DCLK	<50
12	VDPOL	<50
13	HDPOL	<50
14	DCLKPOL	<50
15	SBGR	<50
16	DE	<50
17	PARA_SERI	<50
18	EXTC	<50
19	HDIR	<50
20	VDIR	<50
21	CS	<50
22	SDI	<50
23	SDO	<50
24	SCL	<50
25	DISP	<50
26	GRB	<50
27	MVA_TN	<50
28	DR7-DR0	<50
29	DG7-DG0	<50
30	DB7-DB0	<50

	Pin Name	Unit: ohm
31	AGND	<3
32	AVCL	<50
33	AVCL1	<50
34	AVDD	<50
35	AVDD1	<50
36	VGH	<50
37	VGL	<50
38	PGND	<3
39	PVDD	<3
40	VGSP	<50
41	RES	<50

17. COLOR FILTER ARRANGEMENT

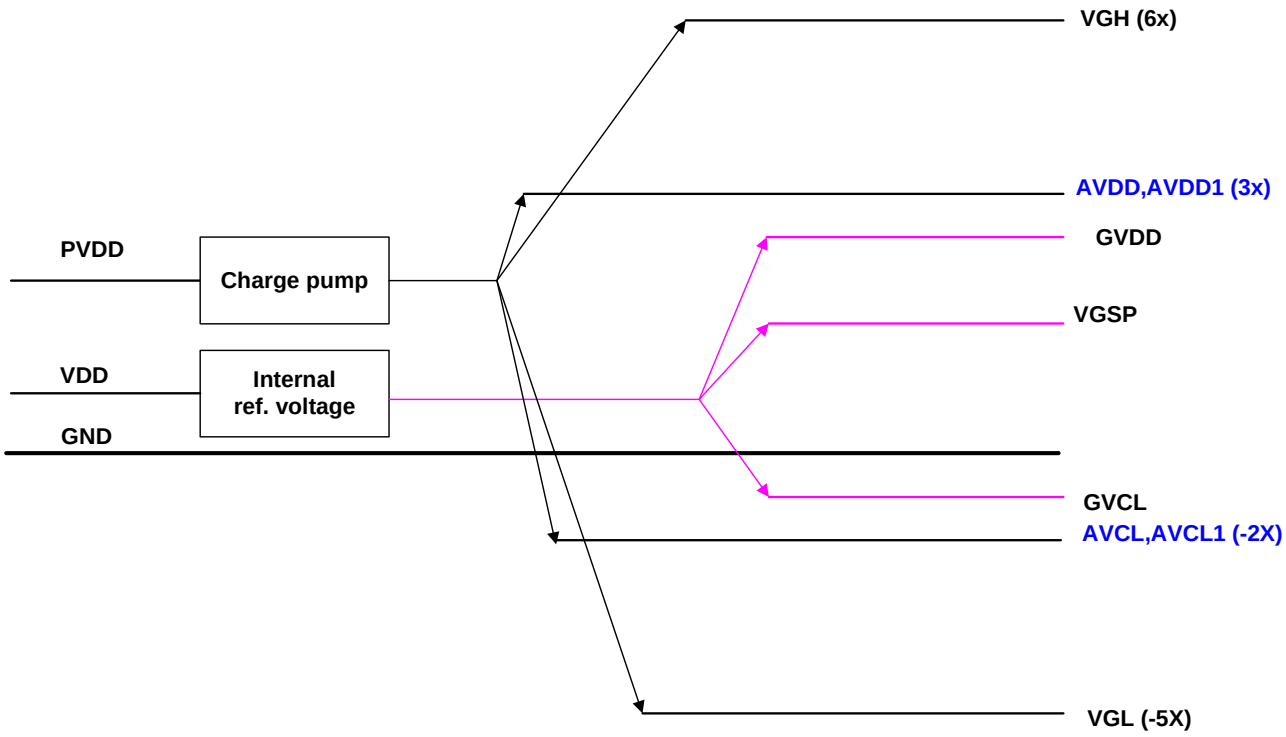
ST7257 supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.



18. POWER STRUCTURE

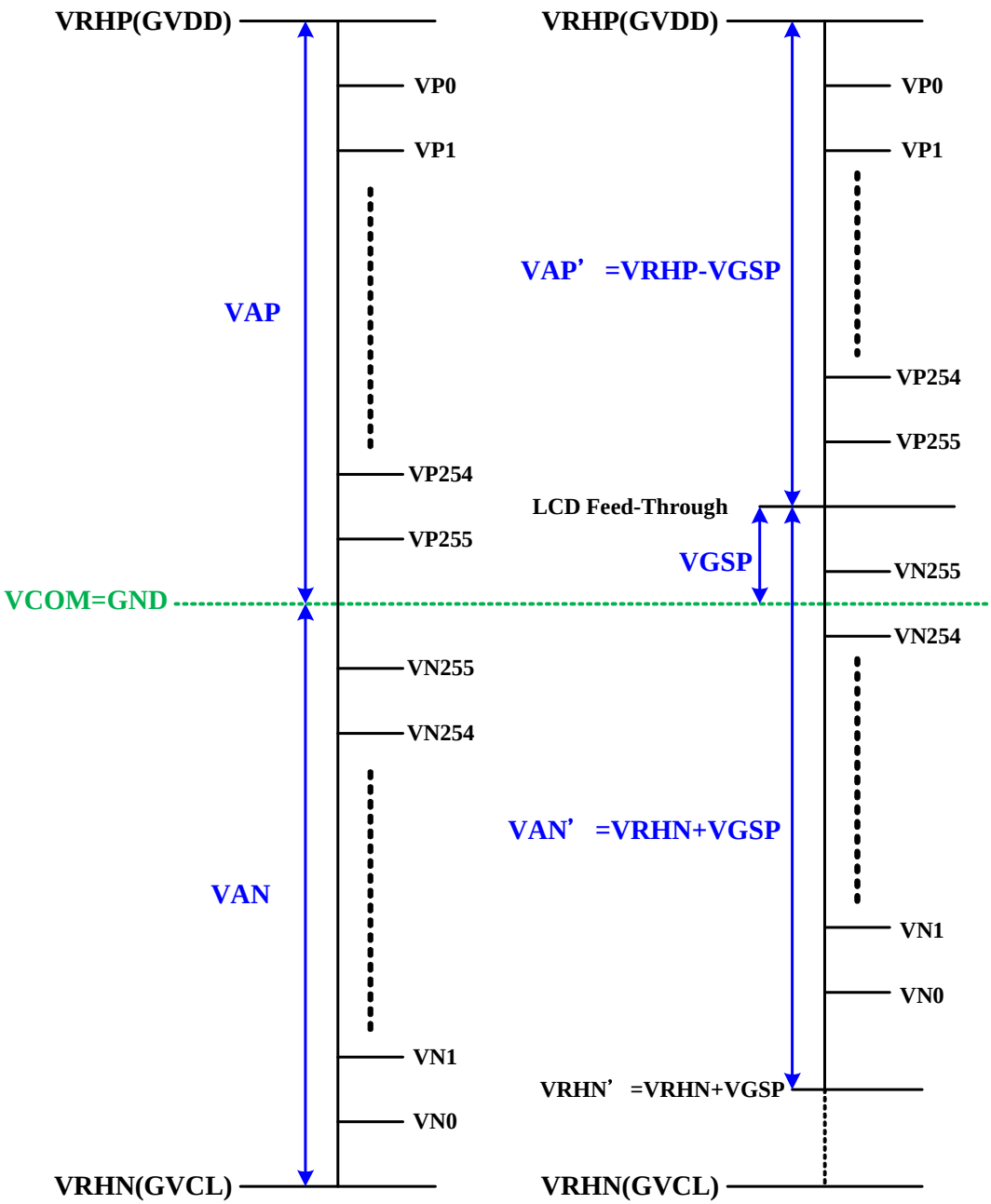
18.1 Voltage Generation

The following figure is relations of analog voltage



18.2 Source Voltage Relations

The relations between VCOM and source voltage is shown as below:



19. REVISION HISTORY

Revision	Description	Date
1.0	Official version	2017/02
1.0a	1. Add VCCA pin description. (P29) 2. Modify RGB Mode Selection Table. (P62) 3. Add application circuit capacitance. (P62~P63)	2017/03
1.1	1. Add R9 H/W pin and S/W register relation. (P37) 2. Add register R53. (P48) 3. Moving “RGB Interface” to build section “10. INPUT DATA FORMAT”.(P56) 4. Modify Serial 8-bit RGB Input Timing Table.(P57) 5. Modify Power Application Circuit. (P61) 6. Modify Voltage Generation. (P73)	2018/06