SSD1317

Advance Information

128 x 96 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SSD1317 Specification

Version	Change Items	Effective Date
1.0	1st Release	21-Dec-15

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1317 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display. It consists of 128 segments and 96 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1317 embeds with contrast control, display RAM and oscillator, which reduce the number of external components and power consumption. It has 256-step contrast. Data/Commands are sent from generic MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I2C interface or Serial Peripheral Interface. SSD1317 is suitable for many compact portable applications which require high display brightness for sunlight readability such as wearable electronics, Wifi routers, etc.

2 FEATURES

- Resolution: 128 x 96 dot matrix panel
- Power supply
  - V_{DD} = 1.65V – 3.3V (for IC logic)
  - V_{CC} = 7.0V – 16.5V (for Panel driving)
- Segment maximum source current: 600uA
- Common maximum sink current: 76.8mA
- Embedded 128 x 96 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8 bits 6800/8080-series parallel Interface
  - 3/4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving infinite content scrolling function
- Internal or external I_{REF} selection
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Power On Reset (POR)
- On-Chip Oscillator
- Chip layout for COG, COF
- Wide range of operating temperature: -40°C to 85°C

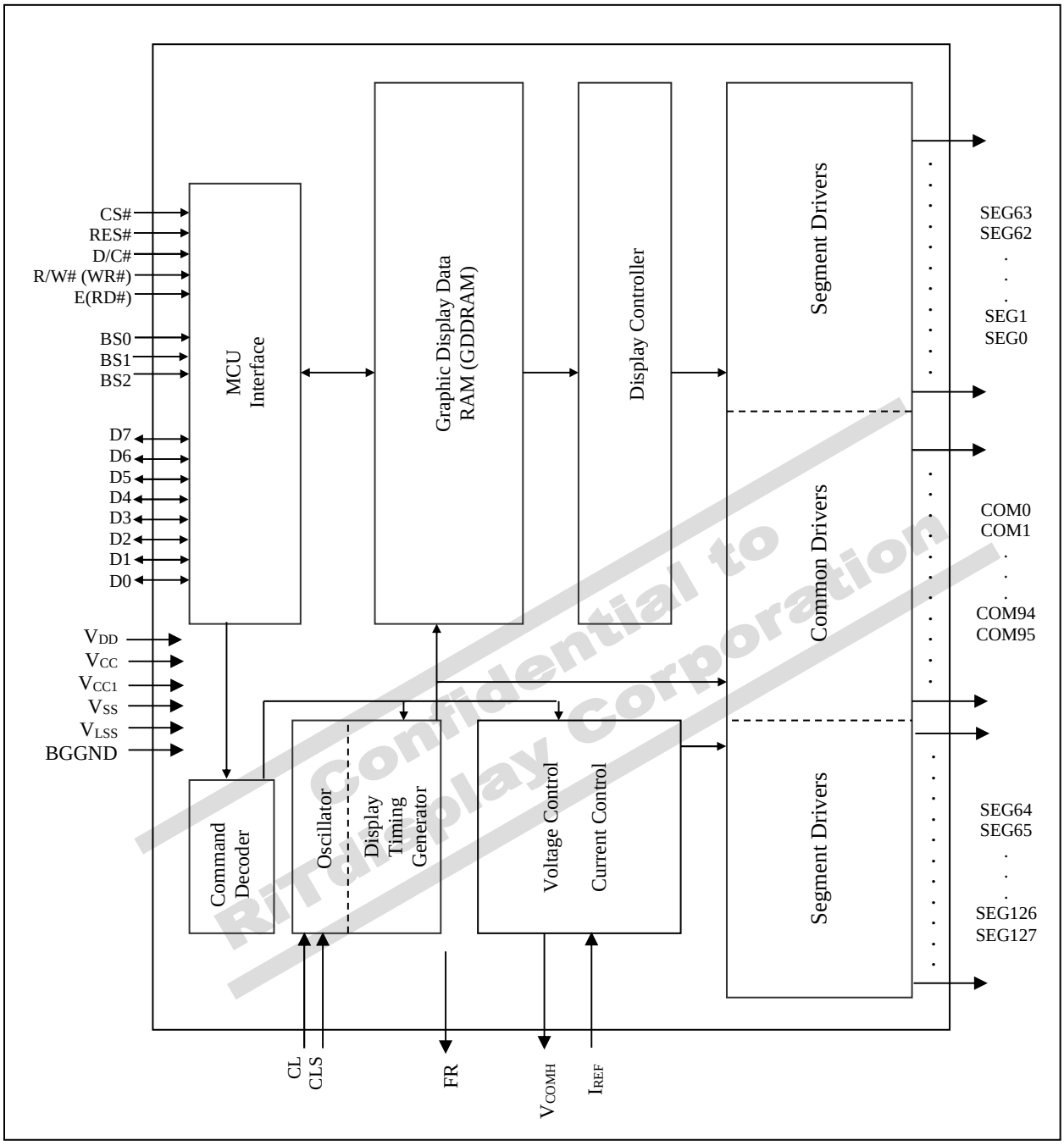
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1317Z	128	96	COG	o Min SEG pad pitch : 29um o Min COM pad pitch : 35um o Min I/O pad pitch : 45um o Die thickness: 250um o Bump height: nominal 9um

4 BLOCK DIAGRAM

Figure 4-1: SSD1317 Block Diagram



5 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 5-1: Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{CC1}	P	Clean power supply for high voltage circuit. It must be connected to V_{CC} externally.
BGGND	P	Reserved pin. It must be connected to ground.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
VSL	P	This is segment voltage (output low level) reference pin. When external VSL is not used, this pin must be connected to V_{LSS} externally. When external VSL is used, connect with resistor and diode to ground (details depends on application).
V_{LH}	P	Logic high (same voltage level as V_{DD}) for internal connection of input and I/O pins. No need to connect to external power source.
V_{LL}	P	Logic low (same voltage level as V_{SS}) for internal connection of input and I/O pins. No need to connect to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
VBREF	O	This is a reserved pin. It should be kept NC.
BS[2:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. **Table 5-2 : Bus Interface selection** BS[2:0] / Interface 000 / 4 line SPI 001 / 3 line SPI 010 / I^2C 110 / 8-bit 8080 parallel 100 / 8-bit 6800 parallel **Note** (1) 0 is connected to V_{SS} (2) 1 is connected to V_{DD}

Pin Name	Pin Type	Description
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain the current around 18.75uA. Please refer to Figure 6-15 for the details of resistor value. When internal I_{REF} is used, this pin should be kept NC.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams Figure 9-1 to Figure 9-3.
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.

Pin Name	Pin Type	Description
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
T0	I/O	This is a reserved pin. It should be kept NC.
T1	I/O	This is a reserved pin. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM95	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
TR[10:0]	-	Reserved pin. It should be kept NC.
NC	-	This is dummy pin. It should be kept NC.

6 FUNCTIONAL BLOCK DESCRIPTIONS

6.1 MCU Interface selection

SSD1317 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 5-2 for BS[2:0] setting).

Table 6-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW						SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW						SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

6.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

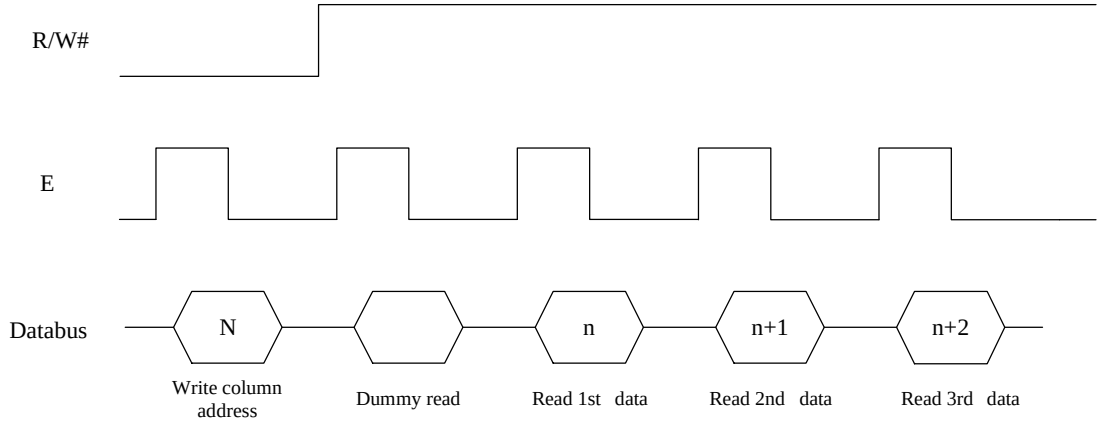
Table 6-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

Figure 6-1 : Data read back procedure - insertion of dummy read



6.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6-2 : Example of Write procedure in 8080 parallel interface mode

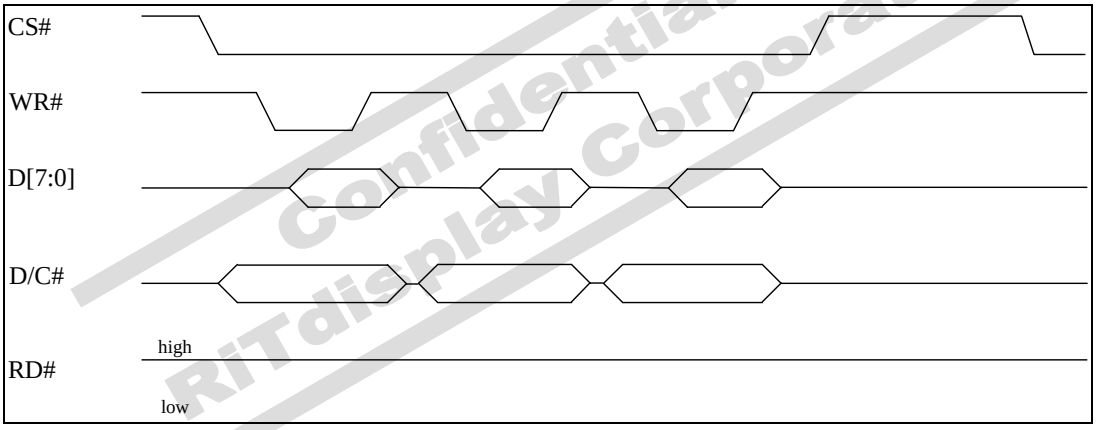


Figure 6-3 : Example of Read procedure in 8080 parallel interface mode

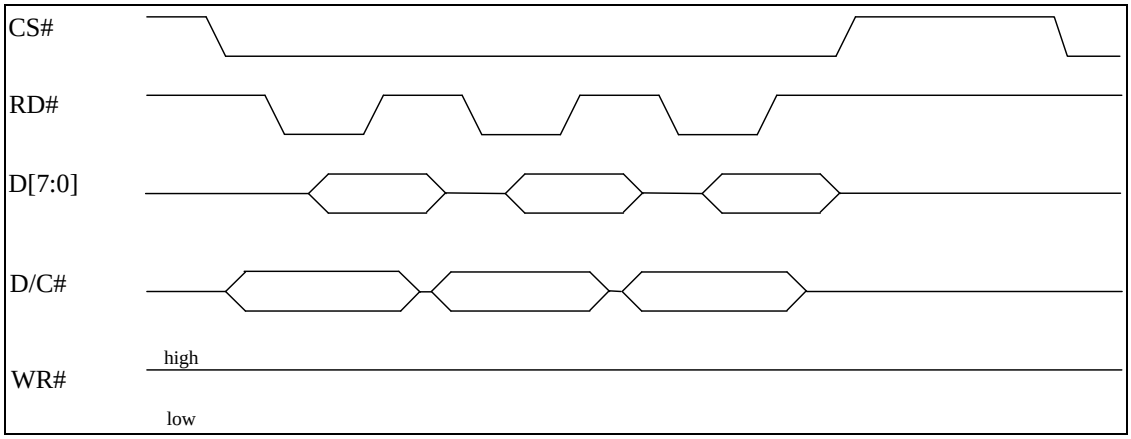


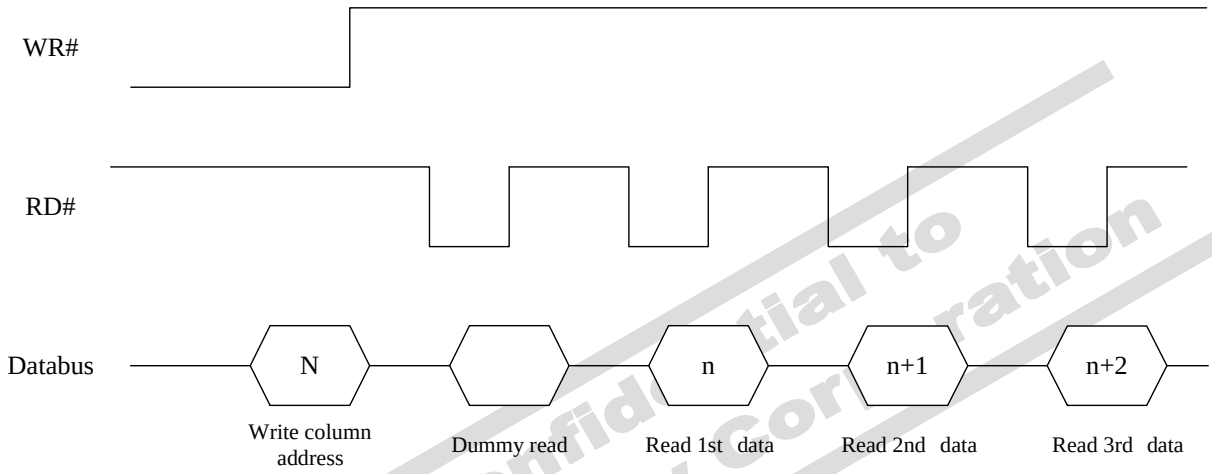
Table 6-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

Figure 6-4 : Display data read back procedure - insertion of dummy read



6.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins from D2 to D7, E(RD#) and R/W#(WR#) can be connected to an external ground.

Table 6-4 : Control pins of 4-wire Serial interface

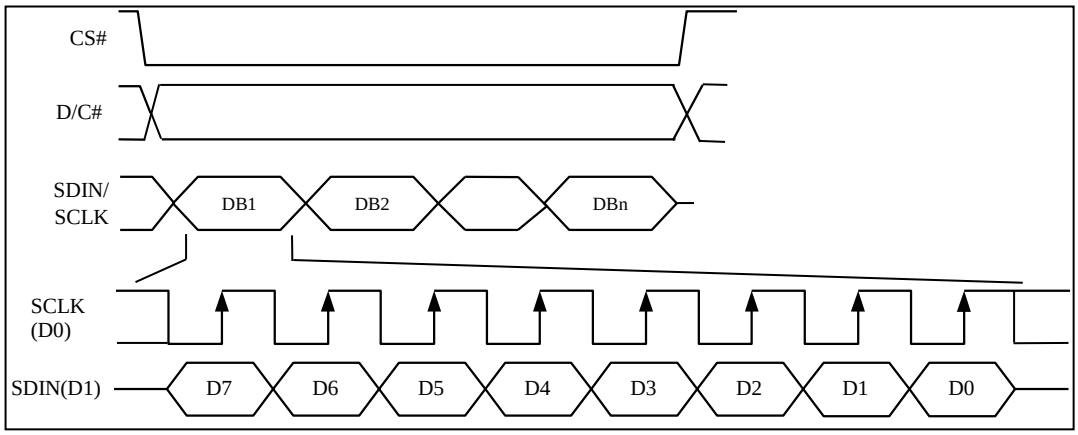
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 6-5 : Write procedure in 4-wire Serial interface mode



6.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins from D2 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

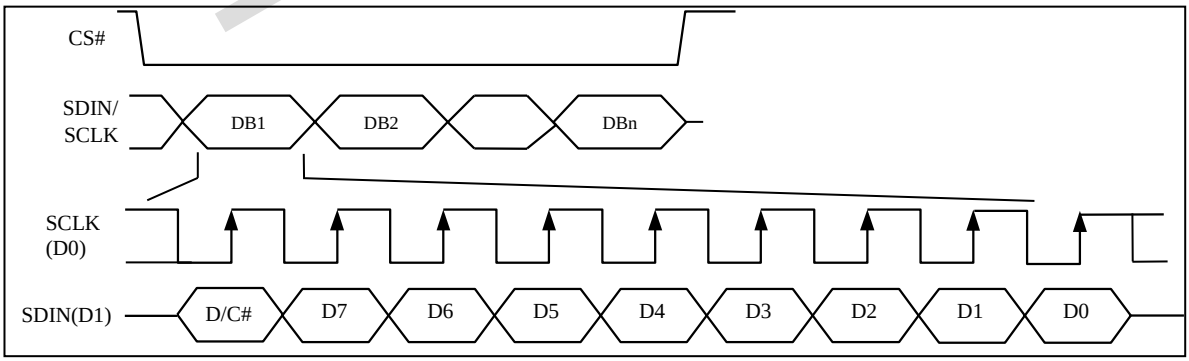
Under serial mode, only write operations are allowed.

Table 6-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 6-6 : Write procedure in 3-wire Serial interface mode



6.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1317 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1317. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

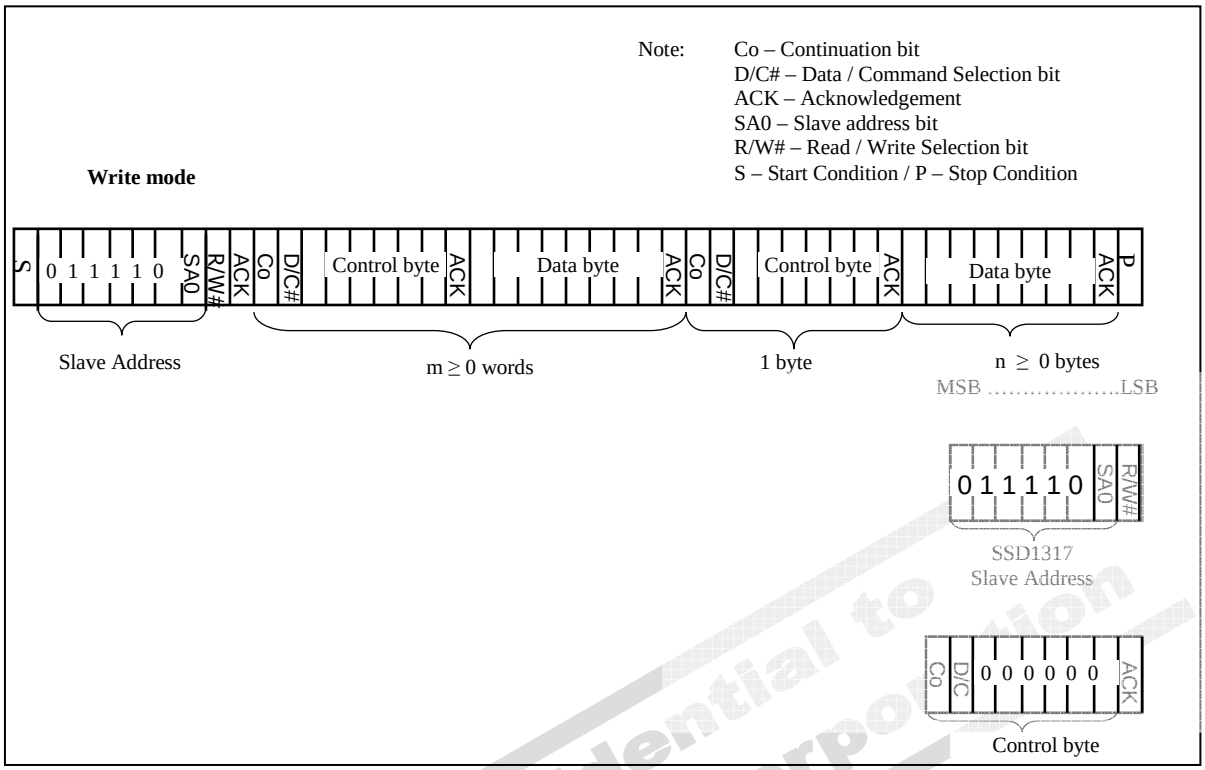
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 6-7 for the write mode of I²C-bus in chronological order.

Figure 6-7 : I²C-bus data format



6.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1317, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the
5) Figure 6-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
6) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
7) Acknowledge bit will be generated after receiving each control byte or data byte.
8) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 6-8 : Definition of the Start and Stop Condition

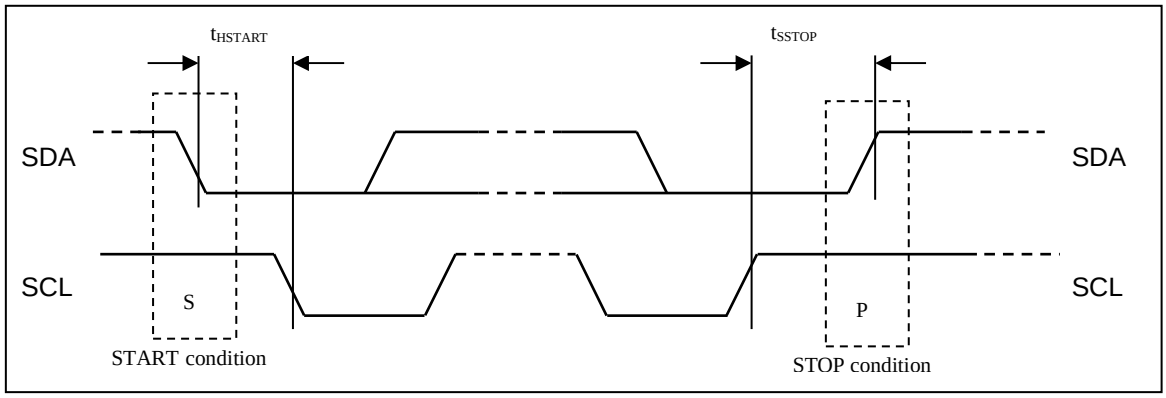
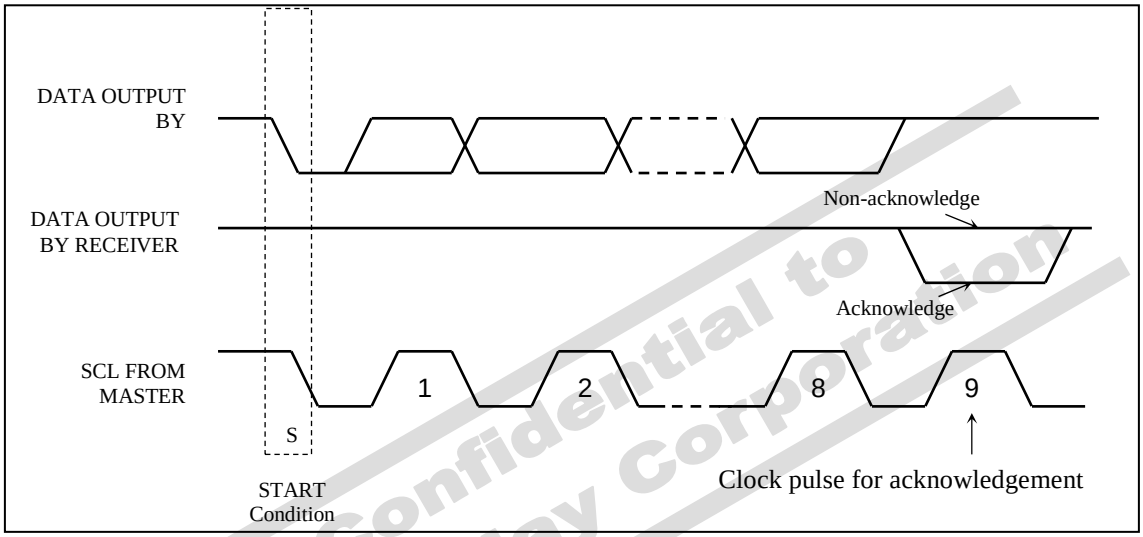


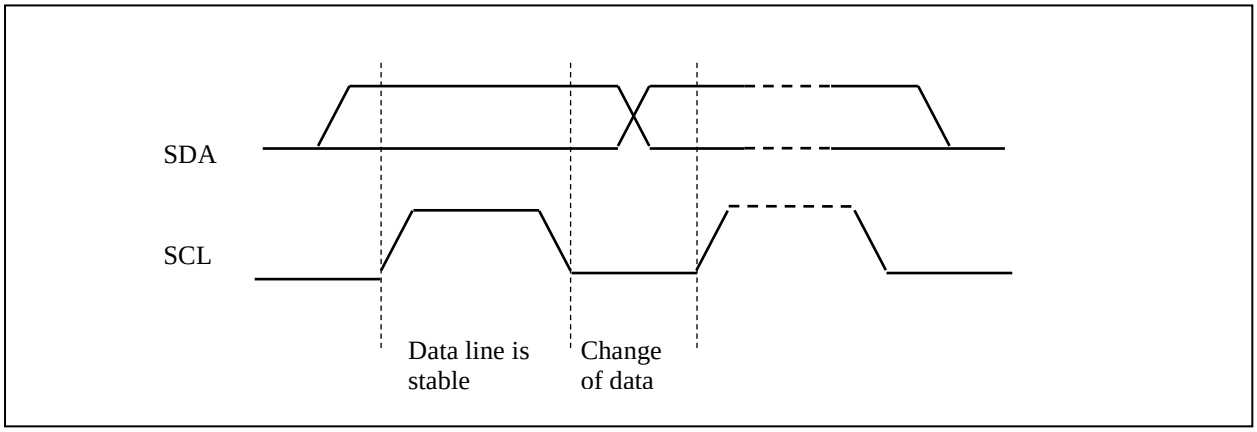
Figure 6-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 6-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-10 : Definition of the data transfer condition



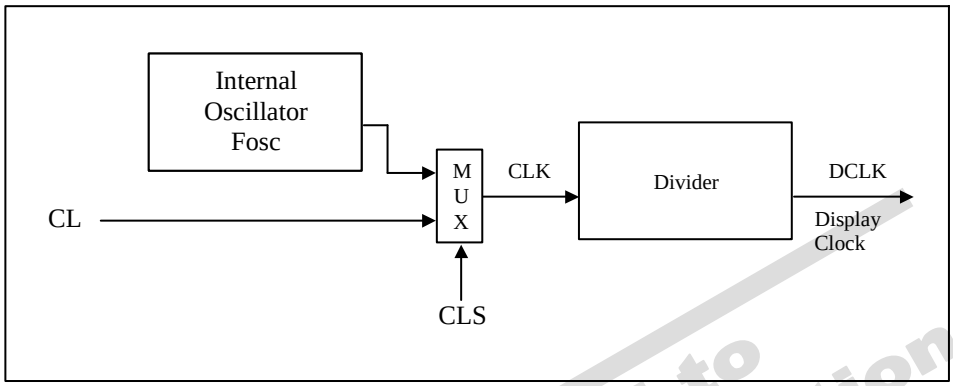
6.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

6.3 Oscillator Circuit and Display Time Generator

Figure 6-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 256 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\ of\ Mux}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 256.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 2 + 2 + 69 = 73 at power on reset (that is K_o is a constant that equals to 69)
  Please refer to Section 6.5 "Segment Drivers / Common Drivers" for the details of the "Phase".
- Number of multiplex ratio is set by command A8h. The power on reset value is 95 (i.e. 96MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

6.4 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 96 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

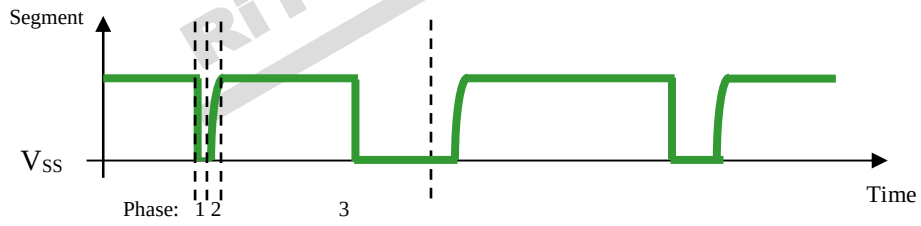
6.5 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (81h). Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 6-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 69, after finishing 69 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

6.6 Graphic Display Data RAM (GDDRAM)

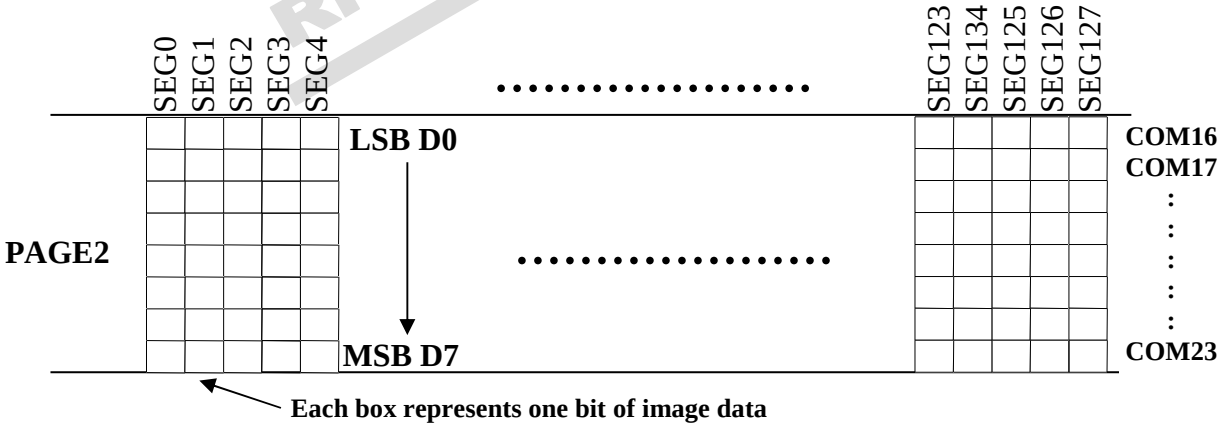
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 96 bits and the RAM is divided into eight pages, from PAGE0 to PAGE11, which are used for monochrome 128x96 dot matrix display, as shown in Figure 6-13.

Figure 6-13 : GDDRAM pages structure

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM95-COM88)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM87-COM80)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM79-COM72)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM71-COM64)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM63-COM56)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM55-COM48)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM47-COM40)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM39-COM32)
PAGE8 (COM64-COM71)	Page 8	PAGE8 (COM31-COM24)
PAGE9 (COM72-COM79)	Page 9	PAGE9 (COM23-COM16)
PAGE10 (COM80–COM87)	Page 10	PAGE10 (COM15-COM8)
PAGE11 (COM88-COM95)	Page 11	PAGE11 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 6-14.

Figure 6-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 6-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

6.7 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

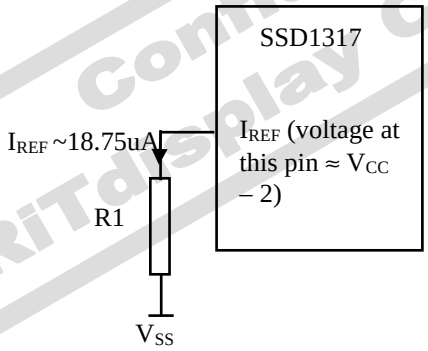
  I_{SEG} = Contrast / 8 x I_{REF}

  in which the contrast (1~255) is set by Set Contrast command 81h

  When internal I_{REF} is used, the I_{REF} pin should be kept NC.
  Bit A[4] of command ADh is used to select external or internal I_{REF} :
  A[4] = '0' Select external I_{REF} [Reset]
  A[4] = '1' Enable internal I_{REF} during display ON

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 6-15. It is recommended to set I_{REF} to 18.75 ± 2uA so as to achieve I_{SEG} = 600uA at maximum contrast 255.

Figure 6-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2V, the value of resistor R1 can be found as below:

For I_{REF} = 18.75uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 2) / 18.75uA
= 530kΩ

6.8 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1317.

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
1. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

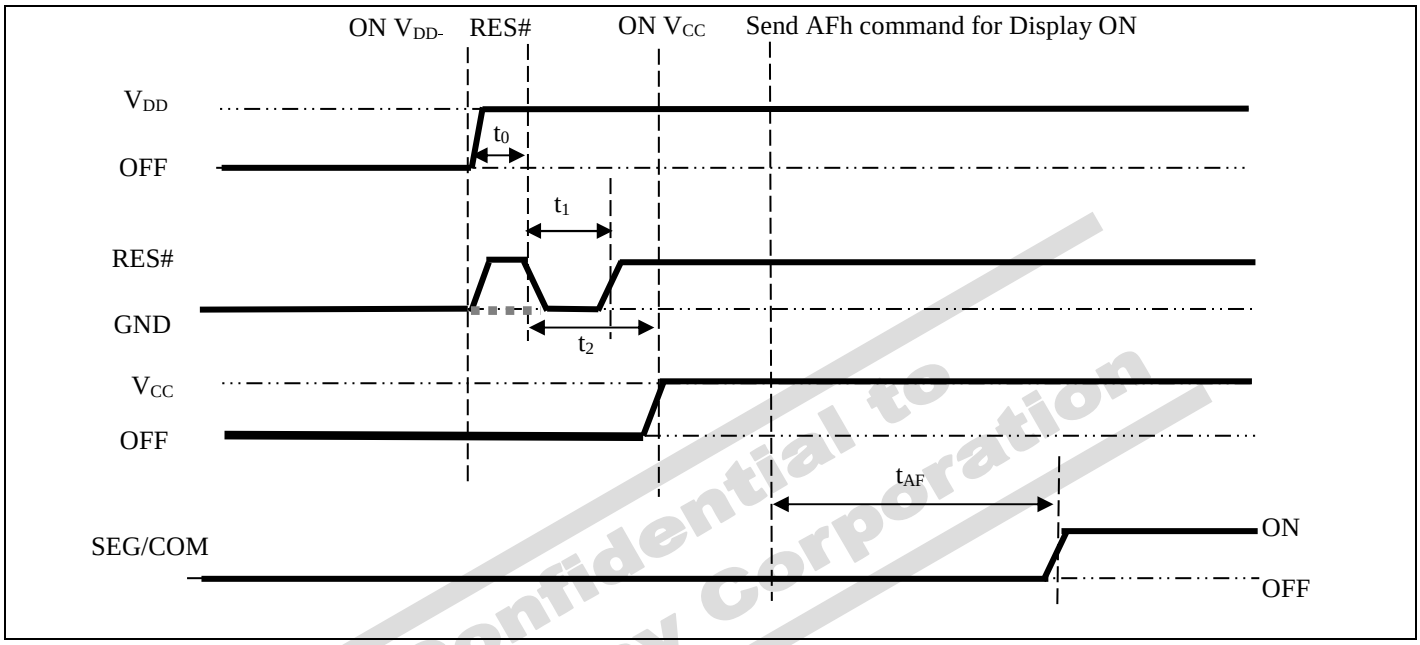
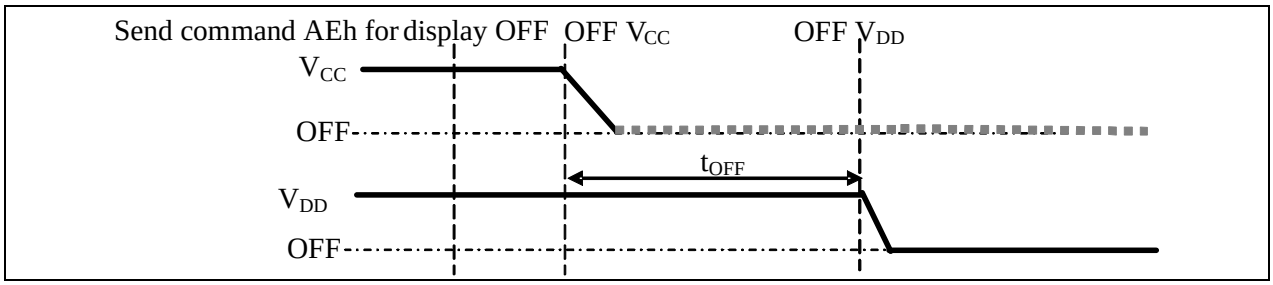


Figure 6-16 : The Power ON sequence

Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Power OFF V_{DD} after t_{OFF}. [4] (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 6-17 : The Power OFF sequence



Note:

(1) V_{CC} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

7 MAXIMUM RATINGS

Table 7-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 17	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

8 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65V to 3.3V

T_A = 25°C

Table 8-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	-	16.5	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{DD,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~16.5V Display OFF, No panel attached	-	-	10	uA
$I_{CC,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~16.5V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12V, I_{REF} = 18.75uA, No loading, Display ON, All ON	Contrast = FFh	-	800	1100	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 12V, I_{REF} = 18.75uA , No loading, Display ON, All ON,		-	220	300	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC}=12V, I_{REF}=18.75uA, Display ON.	Contrast=FFh	540	600	660	uA
		Contrast=7Fh	-	300	-	
		Contrast=3Fh	-	150	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:127] = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

9 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to 3.3V
T_A = 25°C

Table 9-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	720	800	880	kHz
F_{FRM}	Frame Frequency	128x96 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx96)(2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 1)
K: number of display clocks per row period (default value = 73)

Table 9-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	150	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	150 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 9-1 : 6800-series MCU parallel interface characteristics

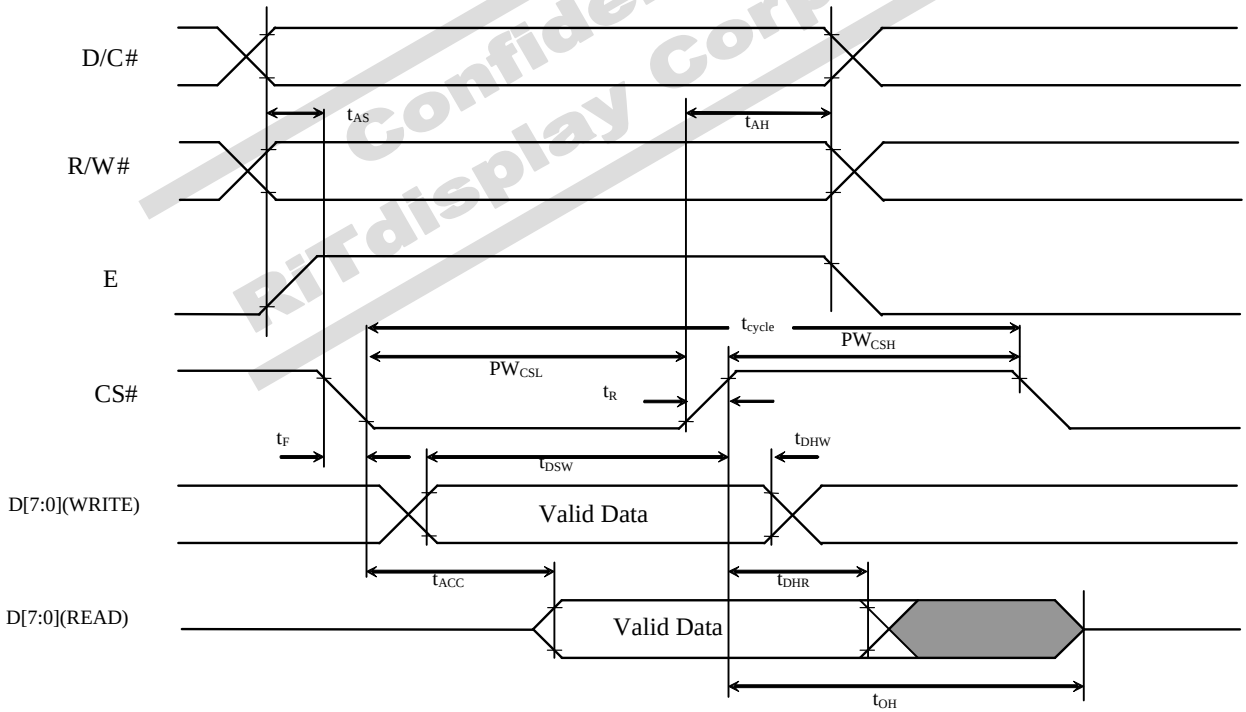
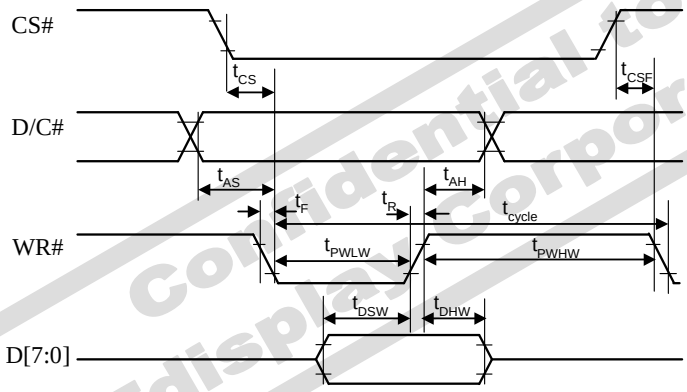


Table 9-3 : 8080-Series MCU Parallel Interface Timing Characteristics

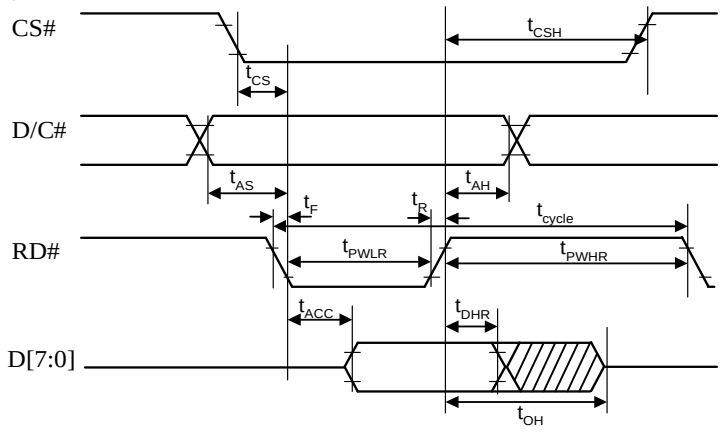
(V_{DD} - V_{SS} = 1.65V ~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	150	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 9-2 : 8080-series parallel interface characteristics



Write cycle



Read Cycle

Table 9-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	50	-	-	ns
t_{DSW}	Write Data Setup Time	20	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	50	-	-	ns
t_{CLKH}	Clock High Time	50	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 9-3 : Serial interface characteristics (4-wire SPI)

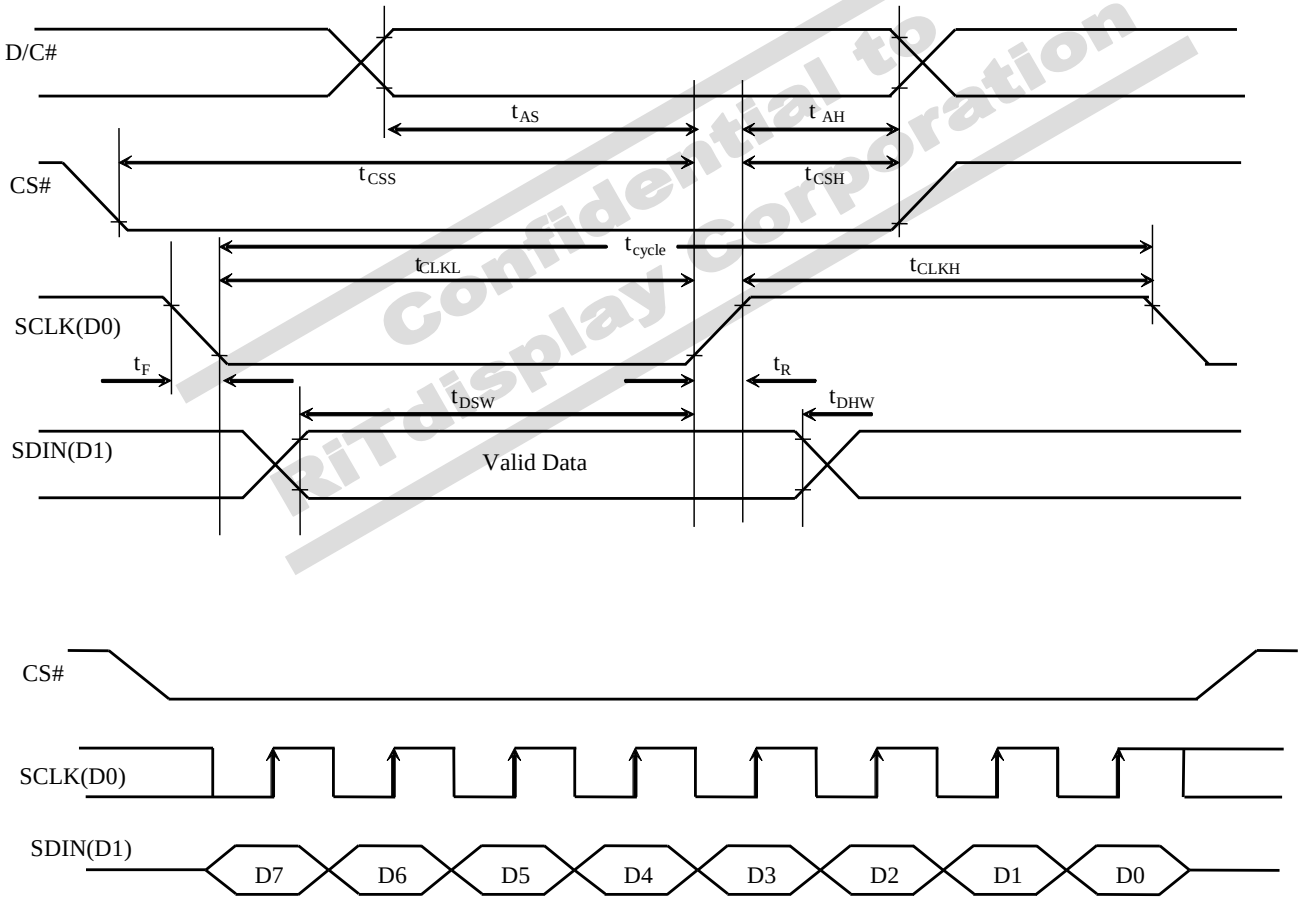


Table 9-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	50	-	-	ns
t_{DSW}	Write Data Setup Time	20	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	50	-	-	ns
t_{CLKH}	Clock High Time	50	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 9-4 : Serial interface characteristics (3-wire SPI)

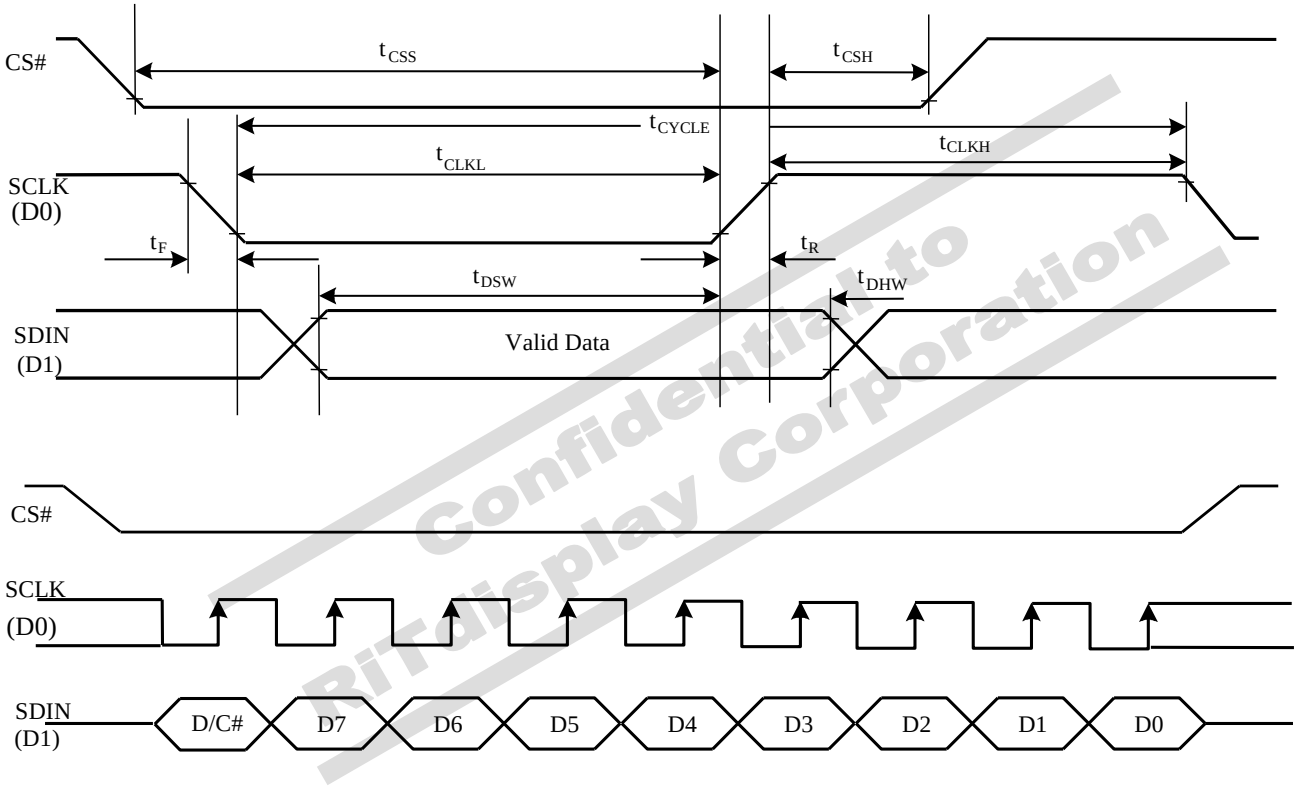
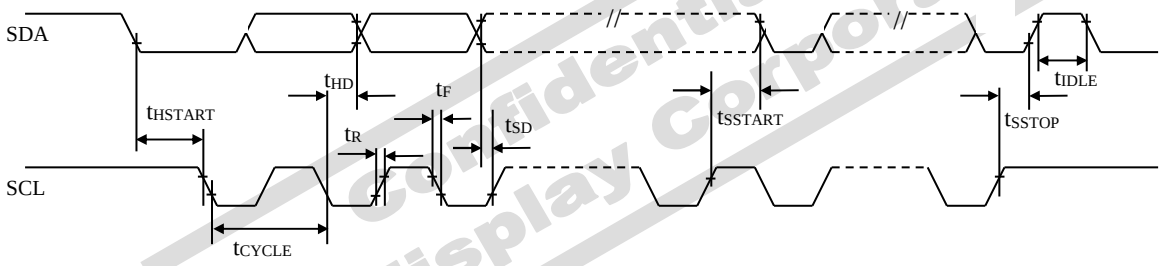


Table 9-6 : I²C Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

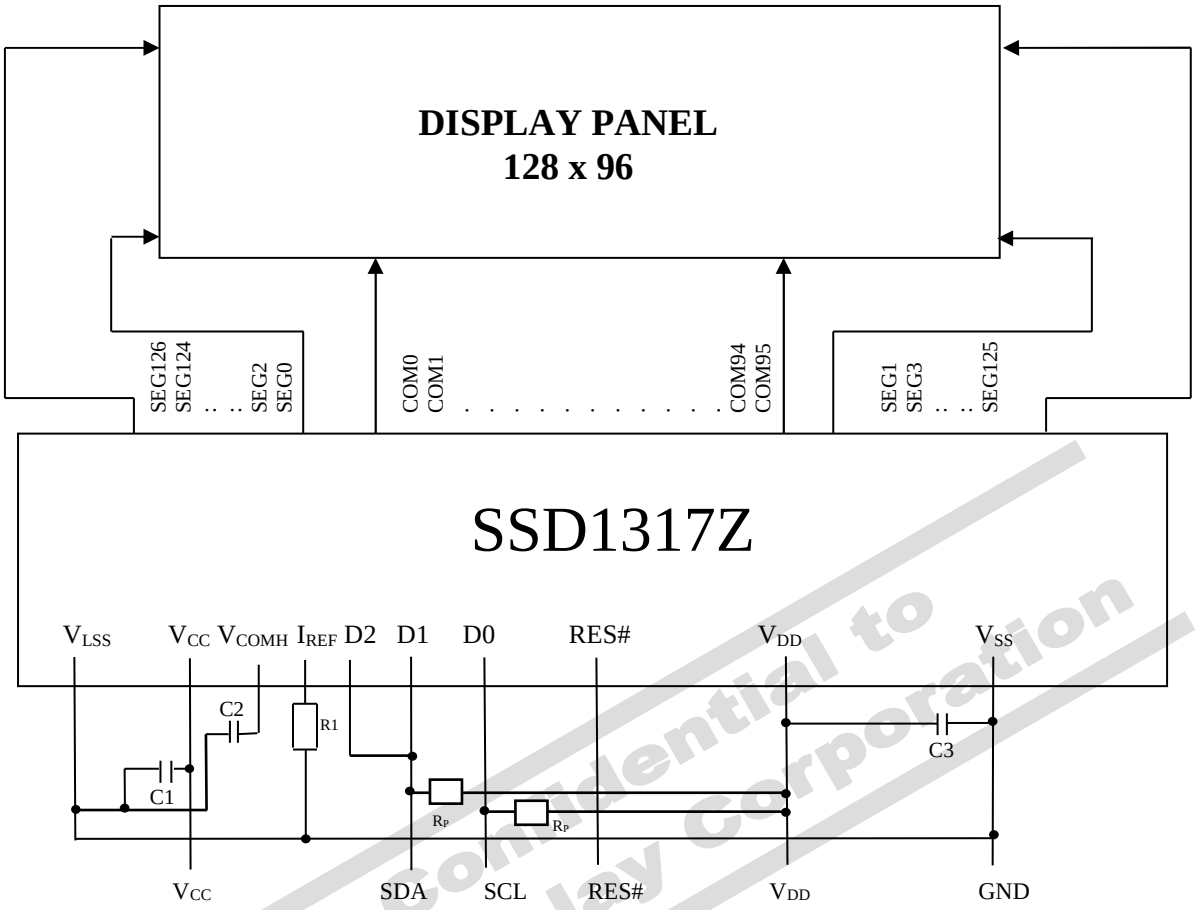
Figure 9-5 : I²C interface Timing characteristics



10 APPLICATION EXAMPLE

Figure 10-1 : Application Example of SSD1317Z

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD}=2.8V, V_{CC} =12V, I_{REF}=18.75uA)



Pin connected to MCU interface: D[2:0], RES#
Pin internally connected to V_{LSS}: BGGND, VSL
Pin internally connected to V_{SS} (or V_{LL}): D[7:3], BS0, BS2, E, R/W#, CS#, CL
Pin internally connected to V_{DD} (or V_{LL}): BS1, CLS
Pin internally connected to V_{CC}: V_{CC1}
VBREF, FR, T0, T1, TR[10:0] should be left open
D/C# acts as SA0 for slave address selection

C1, C2: 2.2uF (1)
C3: 1.0uF (1) place close to IC V_{DD} and V_{SS} pins on PCB
R_P : Pull up resistor

Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 12V, I_{REF} = 18.75uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (12-2)V / 18.75uA
≈ 530KΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face down.
(3) V_{LSS} of IC pad no. 25 to 29 are recommended to be connected to the V_{LSS} of pad no. 65 to 68 to form a larger area of GND.
(4) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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Appendix II: SSD1317 Command Table and Command Descriptions

1 COMMAND TABLE

Table 1-1: SSD1317 Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	10~17	0	0	0	1	0	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[2:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 0 0	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[3:0] B[3:0]	0 * *	0 * *	1 * *	0 * *	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[3:0] : Page start Address, range : 0-11d, (RESET = 0d) B[3:0] : Page end Address, range : 0-11d, (RESET = 11d) **Note** (1) This command is only for horizontal or vertical addressing mode.

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET. **Note** (1) For display start line register up to 95, please refer to command A2h.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh) A[7:0] valid range: 01h to FFh
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A2 A[6:0]	1 0	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Start Line	Set display RAM display start line register from 0-95 by A[6:0] (RESET=00h) **Note** (1) In command A2h, A[6:0] from 00h to 3Fh has the same effect as command 40h-7Fh.
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[6:0] : from 16MUX to 96MUX. RESET= 101 1111b (i.e. 95d, 96MUX) A[6:0] from 0 to 14 are invalid entry.
0 0	AD A[4]	1 0	0 0	1 0	0 A_4	1 0	1 0	0 0	1 0	External or internal I_{REF} Selection	Select external or internal I_{REF} : A[4] = '0' Select external I_{REF} (RESET) A[4] = '1' Enable internal I_{REF} during display ON **Note** (1) Refer to section 7.7 in SSD1317 datasheet for details.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	B0~BB	1	0	1	1	X_3	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE11) for Page Addressing Mode using X[3:0]. **Note** (1) This command is only for page addressing mode
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[6:0]	1 *	1 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~95d The value is reset to 00h after RESET.
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) (i.e. 1, 2, 4, 8…256) (RESET is 0000b, i.e. divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (RESET is 0000b) Range: 0000b~1111b.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h)
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set SEG Pins Hardware Configuration	A[4]=0b, Sequential SEG pin configuration A[4]=1b (RESET), Alternative (odd/even) SEG pin configuration A[5]=0b (RESET), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap
0 0	DB A[5:3]	1 0	1 0	0 A_5	1 A_4	1 A_3	0 0	1 0	1 0	Set V_{COMH} select Level	Set COM select voltage level. **A[5:3]** / **Hex code** / **V_{COMH} deselect level** 000b / 00h / ~ 0.43 x V_{CC} 010b / 10h / ~ 0.57 x V_{CC} 100b / 20h / ~ 0.67 x V_{CC} 110b / 30h / ~ 0.78 x V_{CC} (RESET) 111b / 38h / ~ 0.84 x V_{CC}

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll Horizontal scroll by 1 column A[7:0] : Dummy byte (Set as 00h) B[3:0] : Define start page address C[2:0] : Set time interval between each scroll step in terms of frame frequency D[3:0] : Define end page address E[7:0] : Dummy byte (Set as 00h) F[7:0] : Define the start column address (RESET = 00h) G[7:0] : Define the end column address (RESET = 7Fh) **Notes:** (1) The value of D[3:0] must be larger than or equal to B[3:0] (2) The value of G[6:0] must be larger than or equal to F[6:0]
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[3:0]	*	*	*	*	B_3	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[3:0]	*	*	*	*	D_3	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[6:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[6:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0		

0000b – PAGE0	0100b – PAGE4	1000b – PAGE8
0001b – PAGE1	0101b – PAGE5	1001b – PAGE9
0010b – PAGE2	0110b – PAGE6	1010b – PAGE10
0011b – PAGE3	0111b – PAGE7	1011b – PAGE11

000b – 6 frames	100b – 3 frames
001b – 32 frames	101b – 4 frames
010b – 64 frames	110b – 5 frames
011b – 128 frames	111b – 2 frames

0000b – PAGE0	0100b – PAGE4	1000b – PAGE8
0001b – PAGE1	0101b – PAGE5	1001b – PAGE9
0010b – PAGE2	0110b – PAGE6	1010b – PAGE10
0011b – PAGE3	0111b – PAGE7	1011b – PAGE11

Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll A[0] : Set number of column scroll offset 0b No horizontal scroll 1b Horizontal scroll by 1 column B[3:0] : Define start page address 0000b – PAGE0 | 0100b – PAGE4 | 1000b – PAGE8 0001b – PAGE1 | 0101b – PAGE5 | 1001b – PAGE9 0010b – PAGE2 | 0110b – PAGE6 | 1010b – PAGE10 0011b – PAGE3 | 0111b – PAGE7 | 1011b – PAGE11 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 5 frames 011b – 128 frames | 111b – 2 frames D[3:0] : Define end page address 0000b – PAGE0 | 0100b – PAGE4 | 1000b – PAGE8 0001b – PAGE1 | 0101b – PAGE5 | 1001b – PAGE9 0010b – PAGE2 | 0110b – PAGE6 | 1010b – PAGE10 0011b – PAGE3 | 0111b – PAGE7 | 1011b – PAGE11 E[7:4]: (Set as 0000b) E[3:0] : Vertical scrolling offset e.g. E[3:0]= 0001b refer to offset = 1 row E[3:0]= 1111b refer to offset = 15 rows F[6:0] : Define the start column address (RESET = 00h) G[6:0] : Define the end column address (RESET = 7Fh) **Note** (1) The value of D[3:0] must be larger than or equal to B[3:0] (2) The value of G[6:0] must be larger than or equal to F[6:0]
0	A[0]	*	*	*	*	*	*	*	A_0		
0	B[3:0]	*	*	*	*	B_3	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[3:0]	*	*	*	*	D_3	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	E_3	E_2	E_1	E_0		
0	F[6:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[6:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0		

Scrolling Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands : 26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h; 2Fh. Valid command sequence 2: 27h; 2Fh. Valid command sequence 3: 29h; 2Fh. Valid command sequence 4: 2Ah; 2Fh. For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[6:0] B[6:0]	1 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[6:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 96] **Note** (1) A[6:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[6:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_6X_5X_4X_3X_2X_1X_0$ of 40h~7Fh or A[6:0] of A2h) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 96d MUX display A[6:0] = 0, B[6:0]=96 : whole area scrolls A[6:0]= 0, B[6:0] < 96 : top area scrolls A[6:0] + B[6:0] < 96 : central area scrolls A[6:0] + B[6:0] = 96 : bottom area scrolls (6) When vertical scrolling is enabled by command 29h / 2Ah, the vertical scroll area is defined by this command.

<table>
<tr><th colspan="12">Advance Graphic Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>2C/2D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>X_0</td><td rowspan="9">Content Scroll Setup</td><td rowspan="9">2Ch, X[0]=0, Right Horizontal Scroll by one column
2Dh, X[0]=1, Left Horizontal Scroll by one column

Horizontal scroll by 1 column

A[7:0] : Dummy byte (Set as 00h)

B[3:0] : Define start page address

0000b – PAGE0 | 0100b – PAGE4 | 1000b – PAGE8
0001b – PAGE1 | 0101b – PAGE5 | 1001b – PAGE9
0010b – PAGE2 | 0110b – PAGE6 | 1010b – PAGE10
0011b – PAGE3 | 0111b – PAGE7 | 1011b – PAGE11

C[7:0] : Dummy byte (Set as 01h)

D[3:0] : Define end page address

0000b – PAGE0 | 0100b – PAGE4 | 1000b – PAGE8
0001b – PAGE1 | 0101b – PAGE5 | 1001b – PAGE9
0010b – PAGE2 | 0110b – PAGE6 | 1010b – PAGE10
0011b – PAGE3 | 0111b – PAGE7 | 1011b – PAGE11

E[7:0] : Dummy byte (Set as 00h)

F[6:0] : Define the start column address (RESET = 00h)

G[6:0] : Define the end column address (RESET = 7Fh)

Note
(1) The value of D[3:0] must be larger than or equal to B[3:0]

(2) The value of G[6:0] must be larger than F[6:0]

(3) A delay time of $2/FrameFreq$ must be set if sending the command of 2Ch / 2Dh consecutively.</td></tr>
<tr><td>0</td><td>A[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>B[3:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>C[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>D[3:0]</td><td>*</td><td>*</td><td>*</td><td>*</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>E[7:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>F[6:0]</td><td>*</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>0</td><td>G[6:0]</td><td>*</td><td>G_6</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
</table>

Note
(1) "*" stands for "Don't care".

Table 1-2 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : "1" for display OFF / "0" for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note
(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

1.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read.
To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 1-3 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

2 COMMAND DESCRIPTIONS

2.1 Fundamental Command

2.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 1-1 and Section 2.1.3 for details.

2.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~17h)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 1-1 and Section 2.1.3 for details.

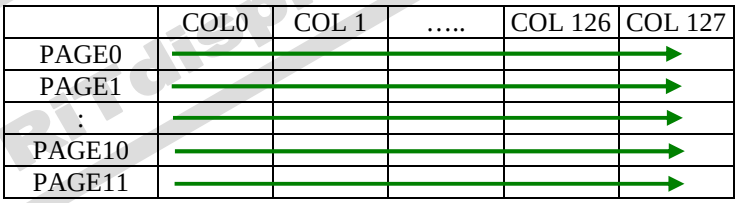
2.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1317: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, "COL" means the graphic display data RAM column.

Page addressing mode (A[1:0]=10b)

In page addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1 and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 2-1.

Figure 2-1 : Address Pointer Movement of Page addressing mode

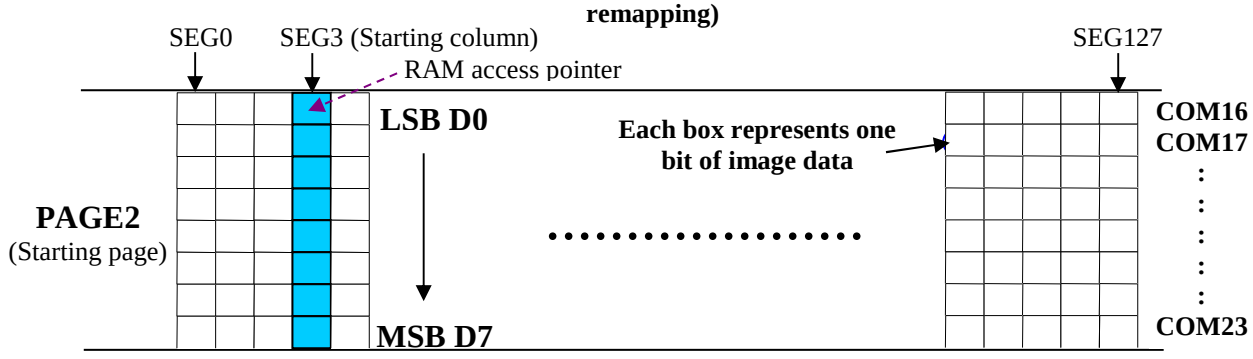


In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to BBh.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~17h.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 2-2. The input data byte will be written into RAM position of column 3.

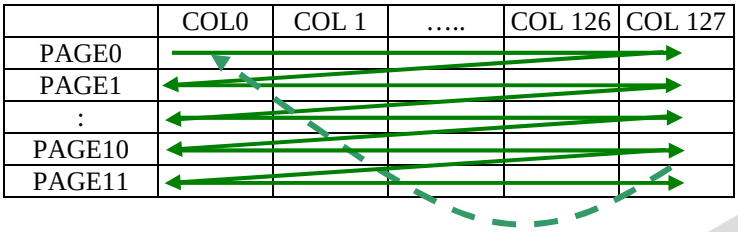
Figure 2-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 2-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 2-3.)

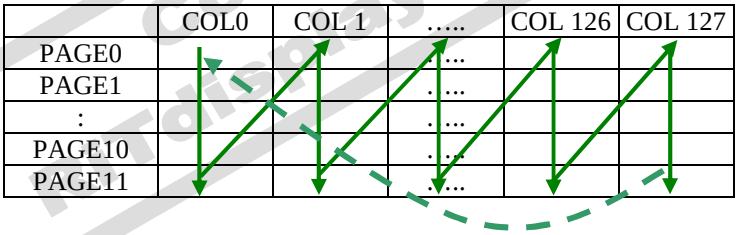
Figure 2-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read / written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 2-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 2-4.)

Figure 2-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 2-5.

2.1.4 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

2.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 97, page start address is set to 1 and page end address is set to 2; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 97 and from page 1 to page 2 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 2-5*). Whenever the column address pointer finishes accessing the end column 97, it is reset back to column 2 and page address is automatically increased by 1 (*solid line in Figure 2-5*). While the end page 2 and end column 97 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 2-5*). .

Figure 2-5: Example of Column and Row Address Pointer Movement

	Col 0	Col 1	Col 2	…..	…….	Col 97	Col98	.....	Col 126	Col 127
PAGE0										
PAGE1										
PAGE2										
:										
PAGE10										
PAGE11										

2.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on. Refer to Table 2-1 for more illustrations. For display start line register setting up to 95, please refer to command A2h.

2.1.7 Set Contrast Control (81h)

This command sets the Contrast Setting of the display, with a valid range from 01h to FFh. The segment output current increases as the contrast step value increases

2.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 1-1.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

2.1.9 Set Display Start Line (A2h)

This double byte command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 95. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on. Refer to Table 2-1 for more illustrations. The value setting from 0 to 63 has the same effect as single byte command 40h-7Fh.

2.1.10 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents. In other words, A4h command resumes the display from entire display "ON" stage.
A5h command forces the entire display to be "ON", regardless of the contents of the display data RAM.

2.1.11 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

2.1.12 Set Multiplex Ratio (A8h)

This command switches the default 64 multiplex mode to any multiplex ratio, ranging from 16 to 95. The output pads COM0~COM95 will be switched to the corresponding COM signal.

2.1.13 External or internal IREF Selection (ADh)

This double byte command supports External or Internal I_{REF} Selection.

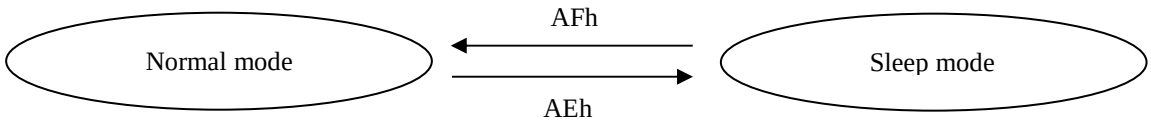
Default A[4] = '0', Select external I_{REF}.
When A[4] = '1', Select internal I_{REF} during display ON.

2.1.14 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 2-6 : Transition between different modes



2.1.15 Set Page Start Address for Page Addressing Mode (B0h~BBh)

This command positions the page start address from 0 to 11 in GDDRAM under Page Addressing Mode. Please refer to Table 1-1 and Section 2.1.3 for details.

2.1.16 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 2-3 for details.

2.1.17 Set Display Offset (D3h)

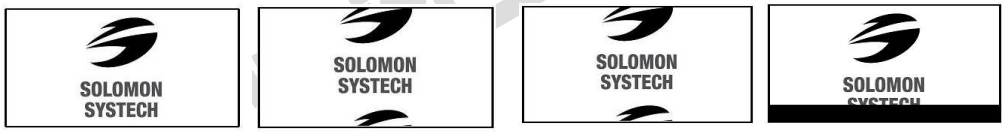
This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM95 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 7-bit data in the second byte should be given as 0010000b. To move in the opposite direction by 16 lines the 7-bit data should be given by 96 – 16, so the second byte would be 1010000b. The following two tables (Table 2-1 and Table 2-2) show the examples of setting the command C0h/C8h and D3h.

Table 2-1: Example of Set Display Offset and Display Start Line without Remap

	Output												
	96		96		96		80		80		80		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offset (D3h)
pin name	0		0		8		0		0		8		Display start line (A2h)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	Row56	RAM56	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	Row57	RAM57	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	Row58	RAM58	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	Row59	RAM59	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	Row60	RAM60	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	Row61	RAM61	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	Row62	RAM62	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	Row63	RAM63	Row55	RAM63	
COM56	Row56	RAM56	Row64	RAM64	Row56	RAM64	Row56	RAM56	Row64	RAM64	Row56	RAM64	
COM57	Row57	RAM57	Row65	RAM65	Row57	RAM65	Row57	RAM57	Row65	RAM65	Row57	RAM65	
COM58	Row58	RAM58	Row66	RAM66	Row58	RAM66	Row58	RAM58	Row66	RAM66	Row58	RAM66	
COM59	Row59	RAM59	Row67	RAM67	Row59	RAM67	Row59	RAM59	Row67	RAM67	Row59	RAM67	
COM60	Row60	RAM60	Row68	RAM68	Row60	RAM68	Row60	RAM60	Row68	RAM68	Row60	RAM68	
COM61	Row61	RAM61	Row69	RAM69	Row61	RAM69	Row61	RAM61	Row69	RAM69	Row61	RAM69	
COM62	Row62	RAM62	Row70	RAM70	Row62	RAM70	Row62	RAM62	Row70	RAM70	Row62	RAM70	
COM63	Row63	RAM63	Row71	RAM71	Row63	RAM71	Row63	RAM63	Row71	RAM71	Row63	RAM71	

	Output												
	96		96		96		80		80		80		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offset (D3h)
pin name	0		0		8		0		0		8		Display start line (A2h)
COM64	Row64	RAM64	Row72	RAM72	Row64	RAM72	Row64	RAM64	Row72	RAM72	Row64	RAM72	
COM65	Row65	RAM65	Row73	RAM73	Row65	RAM73	Row65	RAM65	Row73	RAM73	Row65	RAM73	
COM66	Row66	RAM66	Row74	RAM74	Row66	RAM74	Row66	RAM66	Row74	RAM74	Row66	RAM74	
COM67	Row67	RAM67	Row75	RAM75	Row67	RAM75	Row67	RAM67	Row75	RAM75	Row67	RAM75	
COM68	Row68	RAM68	Row76	RAM76	Row68	RAM76	Row68	RAM68	Row76	RAM76	Row68	RAM76	
COM69	Row69	RAM69	Row77	RAM77	Row69	RAM77	Row69	RAM69	Row77	RAM77	Row69	RAM77	
COM70	Row70	RAM70	Row78	RAM78	Row70	RAM78	Row70	RAM70	Row78	RAM78	Row70	RAM78	
COM71	Row71	RAM71	Row79	RAM79	Row71	RAM79	Row71	RAM71	Row79	RAM79	Row71	RAM79	
COM72	Row72	RAM72	Row80	RAM80	Row72	RAM80	Row72	RAM72	-	-	Row72	RAM80	
COM73	Row73	RAM73	Row81	RAM81	Row73	RAM81	Row73	RAM73	-	-	Row73	RAM81	
COM74	Row74	RAM74	Row82	RAM82	Row74	RAM82	Row74	RAM74	-	-	Row74	RAM82	
COM75	Row75	RAM75	Row83	RAM83	Row75	RAM83	Row75	RAM75	-	-	Row75	RAM83	
COM76	Row76	RAM76	Row84	RAM84	Row76	RAM84	Row76	RAM76	-	-	Row76	RAM84	
COM77	Row77	RAM77	Row85	RAM85	Row77	RAM85	Row77	RAM77	-	-	Row77	RAM85	
COM78	Row78	RAM78	Row86	RAM86	Row78	RAM86	Row78	RAM78	-	-	Row78	RAM86	
COM79	Row79	RAM79	Row87	RAM87	Row79	RAM87	Row79	RAM79	-	-	Row79	RAM87	
COM80	Row80	RAM80	Row88	RAM88	Row80	RAM88	-	-	-	-	-	-	
COM81	Row81	RAM81	Row89	RAM89	Row81	RAM89	-	-	-	-	-	-	
COM82	Row82	RAM82	Row90	RAM90	Row82	RAM90	-	-	-	-	-	-	
COM83	Row83	RAM83	Row91	RAM91	Row83	RAM91	-	-	-	-	-	-	
COM84	Row84	RAM84	Row92	RAM92	Row84	RAM92	-	-	-	-	-	-	
COM85	Row85	RAM85	Row93	RAM93	Row85	RAM93	-	-	-	-	-	-	
COM86	Row86	RAM86	Row94	RAM94	Row86	RAM94	-	-	-	-	-	-	
COM87	Row87	RAM87	Row95	RAM95	Row87	RAM95	-	-	-	-	-	-	
COM88	Row88	RAM88	Row0	RAM0	Row88	RAM0	-	-	Row0	RAM0	-	-	
COM89	Row89	RAM89	Row1	RAM1	Row89	RAM1	-	-	Row1	RAM1	-	-	
COM90	Row90	RAM90	Row2	RAM2	Row90	RAM2	-	-	Row2	RAM2	-	-	
COM91	Row91	RAM91	Row3	RAM3	Row91	RAM3	-	-	Row3	RAM3	-	-	
COM92	Row92	RAM92	Row4	RAM4	Row92	RAM4	-	-	Row4	RAM4	-	-	
COM93	Row93	RAM93	Row5	RAM5	Row93	RAM5	-	-	Row5	RAM5	-	-	
COM95	Row94	RAM94	Row6	RAM6	Row94	RAM6	-	-	Row6	RAM6	-	-	
COM95	Row95	RAM95	Row7	RAM7	Row95	RAM7	-	-	Row7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		



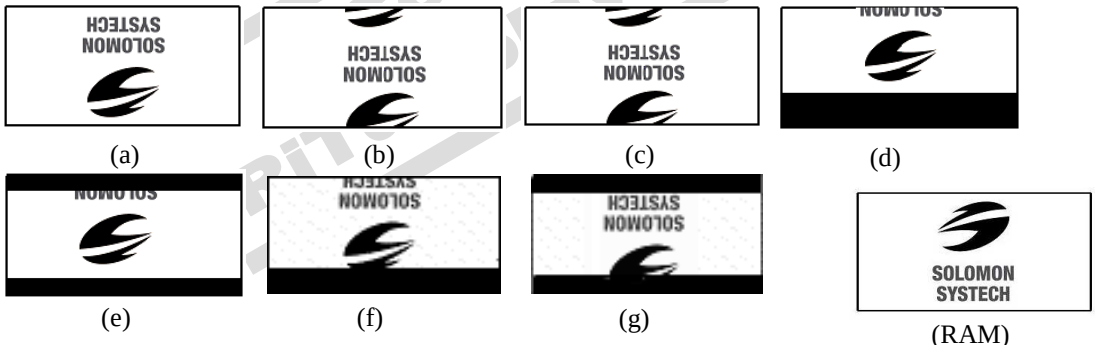
(a) (b) (c) (d)

(e) (f) (RAM)

Table 2-2: Example of Set Display Offset and Display Start Line with Remap

	Output																
	96		96		96		80		80		80		80				Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap				COM Normal / Remapped (C0h / C8h)
Hardware pin	0		8		0		0		8		0		8				Display offset (D3h)
name	0		0		8		0		0		8		16				Display start line (A2h)
COM0	Row 95	RAM95	Row 7	RAM7	Row 95	RAM7	Row 79	RAM79	-	-	Row 79	RAM87	-	-			
COM1	Row 94	RAM94	Row 6	RAM6	Row 94	RAM6	Row 78	RAM78	-	-	Row 78	RAM86	-	-			
COM2	Row 93	RAM93	Row 5	RAM5	Row 93	RAM5	Row 77	RAM77	-	-	Row 77	RAM85	-	-			
COM3	Row 92	RAM92	Row 4	RAM4	Row 92	RAM4	Row 76	RAM76	-	-	Row 76	RAM84	-	-			
COM4	Row 91	RAM91	Row 3	RAM3	Row 91	RAM3	Row 75	RAM75	-	-	Row 75	RAM83	-	-			
COM5	Row 90	RAM90	Row 2	RAM2	Row 90	RAM2	Row 74	RAM74	-	-	Row 74	RAM82	-	-			
COM6	Row 89	RAM89	Row 1	RAM1	Row 89	RAM1	Row 73	RAM73	-	-	Row 73	RAM81	-	-			
COM7	Row 88	RAM88	Row 0	RAM0	Row 88	RAM0	Row 72	RAM72	-	-	Row 72	RAM80	-	-			
COM8	Row 87	RAM87	Row 95	RAM95	Row 87	RAM95	Row 71	RAM71	Row 79	RAM79	Row 71	RAM79	Row 79	RAM95			
COM9	Row 86	RAM86	Row 94	RAM94	Row 86	RAM94	Row 70	RAM70	Row 78	RAM78	Row 70	RAM78	Row 78	RAM94			
COM10	Row 85	RAM85	Row 93	RAM93	Row 85	RAM93	Row 69	RAM69	Row 77	RAM77	Row 69	RAM77	Row 77	RAM93			
COM11	Row 84	RAM84	Row 92	RAM92	Row 84	RAM92	Row 68	RAM68	Row 76	RAM76	Row 68	RAM76	Row 76	RAM92			
COM12	Row 83	RAM83	Row 91	RAM91	Row 83	RAM91	Row 67	RAM67	Row 75	RAM75	Row 67	RAM75	Row 75	RAM91			
COM13	Row 82	RAM82	Row 90	RAM90	Row 82	RAM90	Row 66	RAM66	Row 74	RAM74	Row 66	RAM74	Row 74	RAM90			
COM14	Row 81	RAM81	Row 89	RAM89	Row 81	RAM89	Row 65	RAM65	Row 73	RAM73	Row 65	RAM73	Row 73	RAM89			
COM15	Row 80	RAM80	Row 88	RAM88	Row 80	RAM88	Row 64	RAM64	Row 72	RAM72	Row 64	RAM72	Row 72	RAM88			
COM16	Row 79	RAM79	Row 87	RAM87	Row 79	RAM87	Row 63	RAM63	Row 71	RAM71	Row 63	RAM71	Row 71	RAM87			
COM17	Row 78	RAM78	Row 86	RAM86	Row 78	RAM86	Row 62	RAM62	Row 70	RAM70	Row 62	RAM70	Row 70	RAM86			
COM18	Row 77	RAM77	Row 85	RAM85	Row 77	RAM85	Row 61	RAM61	Row 69	RAM69	Row 61	RAM69	Row 69	RAM85			
COM19	Row 76	RAM76	Row 84	RAM84	Row 76	RAM84	Row 60	RAM60	Row 68	RAM68	Row 60	RAM68	Row 68	RAM84			
COM20	Row 75	RAM75	Row 83	RAM83	Row 75	RAM83	Row 59	RAM59	Row 67	RAM67	Row 59	RAM67	Row 67	RAM83			
COM21	Row 74	RAM74	Row 82	RAM82	Row 74	RAM82	Row 58	RAM58	Row 66	RAM66	Row 58	RAM66	Row 66	RAM82			
COM22	Row 73	RAM73	Row 81	RAM81	Row 73	RAM81	Row 57	RAM57	Row 65	RAM65	Row 57	RAM65	Row 65	RAM81			
COM23	Row 72	RAM72	Row 80	RAM80	Row 72	RAM80	Row 56	RAM56	Row 64	RAM64	Row 56	RAM64	Row 64	RAM80			
COM24	Row 71	RAM71	Row 79	RAM79	Row 71	RAM79	Row 55	RAM55	Row 63	RAM63	Row 55	RAM63	Row 63	RAM79			
COM25	Row 70	RAM70	Row 78	RAM78	Row 70	RAM78	Row 54	RAM54	Row 62	RAM62	Row 54	RAM62	Row 62	RAM78			
COM26	Row 69	RAM69	Row 77	RAM77	Row 69	RAM77	Row 53	RAM53	Row 61	RAM61	Row 53	RAM61	Row 61	RAM77			
COM27	Row 68	RAM68	Row 76	RAM76	Row 68	RAM76	Row 52	RAM52	Row 60	RAM60	Row 52	RAM60	Row 60	RAM76			
COM28	Row 67	RAM67	Row 75	RAM75	Row 67	RAM75	Row 51	RAM51	Row 59	RAM59	Row 51	RAM59	Row 59	RAM75			
COM29	Row 66	RAM66	Row 74	RAM74	Row 66	RAM74	Row 50	RAM50	Row 58	RAM58	Row 50	RAM58	Row 58	RAM74			
COM30	Row 65	RAM65	Row 73	RAM73	Row 65	RAM73	Row 49	RAM49	Row 57	RAM57	Row 49	RAM57	Row 57	RAM73			
COM31	Row 64	RAM64	Row 72	RAM72	Row 64	RAM72	Row 48	RAM48	Row 56	RAM56	Row 48	RAM56	Row 56	RAM72			
COM32	Row 63	RAM63	Row 71	RAM71	Row 63	RAM71	Row 47	RAM47	Row 55	RAM55	Row 47	RAM55	Row 55	RAM71			
COM33	Row 62	RAM62	Row 70	RAM70	Row 62	RAM70	Row 46	RAM46	Row 54	RAM54	Row 46	RAM54	Row 54	RAM70			
COM34	Row 61	RAM61	Row 69	RAM69	Row 61	RAM69	Row 45	RAM45	Row 53	RAM53	Row 45	RAM53	Row 53	RAM69			
COM35	Row 60	RAM60	Row 68	RAM68	Row 60	RAM68	Row 44	RAM44	Row 52	RAM52	Row 44	RAM52	Row 52	RAM68			
COM36	Row 59	RAM59	Row 67	RAM67	Row 59	RAM67	Row 43	RAM43	Row 51	RAM51	Row 43	RAM51	Row 51	RAM67			
COM37	Row 58	RAM58	Row 66	RAM66	Row 58	RAM66	Row 42	RAM42	Row 50	RAM50	Row 42	RAM50	Row 50	RAM66			
COM38	Row 57	RAM57	Row 65	RAM65	Row 57	RAM65	Row 41	RAM41	Row 49	RAM49	Row 41	RAM49	Row 49	RAM65			
COM39	Row 56	RAM56	Row 64	RAM64	Row 56	RAM64	Row 40	RAM40	Row 48	RAM48	Row 40	RAM48	Row 48	RAM64			
COM40	Row 55	RAM55	Row 63	RAM63	Row 55	RAM63	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 47	RAM63			
COM41	Row 54	RAM54	Row 62	RAM62	Row 54	RAM62	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 46	RAM62			
COM42	Row 53	RAM53	Row 61	RAM61	Row 53	RAM61	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 45	RAM61			
COM43	Row 52	RAM52	Row 60	RAM60	Row 52	RAM60	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 44	RAM60			
COM44	Row 51	RAM51	Row 59	RAM59	Row 51	RAM59	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 43	RAM59			
COM45	Row 50	RAM50	Row 58	RAM58	Row 50	RAM58	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 42	RAM58			
COM46	Row 49	RAM49	Row 57	RAM57	Row 49	RAM57	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 41	RAM57			
COM47	Row 48	RAM48	Row 56	RAM56	Row 48	RAM56	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 40	RAM56			
COM48	Row 47	RAM47	Row 55	RAM55	Row 47	RAM55	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 39	RAM55			
COM49	Row 46	RAM46	Row 54	RAM54	Row 46	RAM54	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 38	RAM54			
COM50	Row 45	RAM45	Row 53	RAM53	Row 45	RAM53	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 37	RAM53			
COM51	Row 44	RAM44	Row 52	RAM52	Row 44	RAM52	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 36	RAM52			
COM52	Row 43	RAM43	Row 51	RAM51	Row 43	RAM51	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 35	RAM51			
COM53	Row 42	RAM42	Row 50	RAM50	Row 42	RAM50	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 34	RAM50			
COM54	Row 41	RAM41	Row 49	RAM49	Row 41	RAM49	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 33	RAM49			
COM55	Row 40	RAM40	Row 48	RAM48	Row 40	RAM48	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 32	RAM48			
COM56	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 31	RAM47			
COM57	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 30	RAM46			
COM58	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 29	RAM45			
COM59	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 28	RAM44			
COM60	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 27	RAM43			
COM61	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 26	RAM42			
COM62	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 25	RAM41			
COM63	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 24	RAM40			
COM64	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	Row 23	RAM39			
COM65	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	Row 22	RAM38			
COM66	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	Row 21	RAM37			
COM67	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	Row 20	RAM36			
COM68	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	Row 19	RAM35			
COM69	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	Row 18	RAM34			
COM70	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	Row 17	RAM33			
COM71	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	Row 16	RAM32			
COM72	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	Row 15	RAM31			

	Output														
	96		96		96		80		80		80		80		Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		8		Display offset (D3h)
pin name	0		0		8		0		0		8		16		Display start line (A2h)
COM73	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	Row 14	RAM30	
COM74	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	Row 13	RAM29	
COM75	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	Row 12	RAM28	
COM76	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 3	RAM3	Row 11	RAM11	Row 3	RAM11	Row 11	RAM27	
COM77	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	Row 10	RAM26	
COM78	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	Row 9	RAM25	
COM79	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	Row 8	RAM24	
COM80	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	-	-	Row 7	RAM7	-	-	Row 7	RAM23	
COM81	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	-	-	Row 6	RAM6	-	-	Row 6	RAM22	
COM82	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	-	-	Row 5	RAM5	-	-	Row 5	RAM21	
COM83	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	-	-	Row 4	RAM4	-	-	Row 4	RAM20	
COM84	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	-	-	Row 3	RAM3	-	-	Row 3	RAM19	
COM85	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	-	-	Row 2	RAM2	-	-	Row 2	RAM18	
COM86	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	-	-	Row 1	RAM1	-	-	Row 1	RAM17	
COM87	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	-	-	Row 0	RAM0	-	-	Row 0	RAM16	
COM88	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	-	-	-	-	-	-	-	-	
COM89	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	-	-	-	-	-	-	-	-	
COM90	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	-	-	-	-	-	-	-	-	
COM91	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	-	-	-	-	-	-	-	-	
COM92	Row 3	RAM3	Row 11	RAM11	Row 3	RAM11	-	-	-	-	-	-	-	-	
COM93	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	-	-	-	-	-	-	-	-	
COM94	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	-	-	-	-	-	-	-	-	
COM95	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



(a) (b) (c) (d)

(e) (f) (g)

(RAM)

2.1.18 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 256, with reset value = 0000b. Please refer to section 7.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 0000b.

2.1.19 Set Pre-charge Period (D9h)

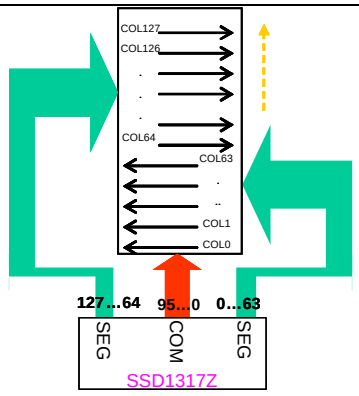
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals to 2 DCLKs.

2.1.20 Set SEG Pins Hardware Configuration (DAh)

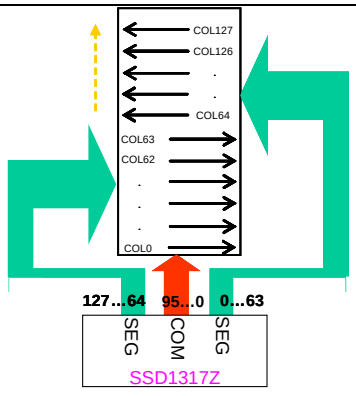
This command sets the SEG signals pin configuration to match the OLED panel hardware layout. SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings:

Table 2-3 : SEG Pins Hardware Configuration

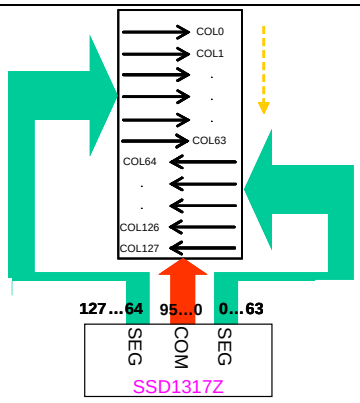
Case no.	Oddeven (1) / Sequential (0) Command : DAh -> A[4]	SEG Remap Command : A0h / A1h	Left / Right Swap Command : DAh -> A[5]	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	



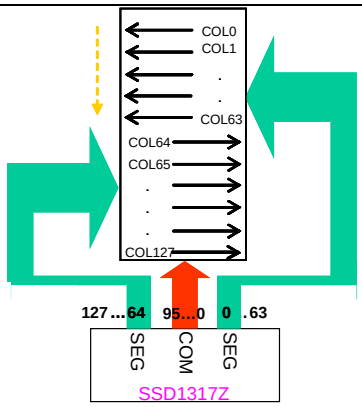
(1) Sequential SEG



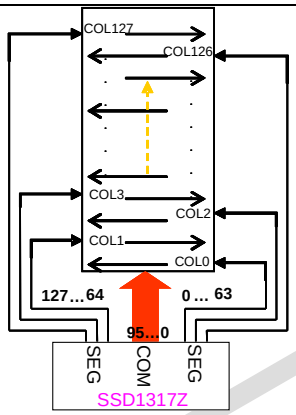
(2) Sequential SEG & left / right



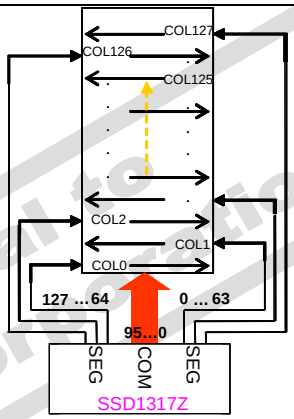
(3) Sequential SEG & SEG remap



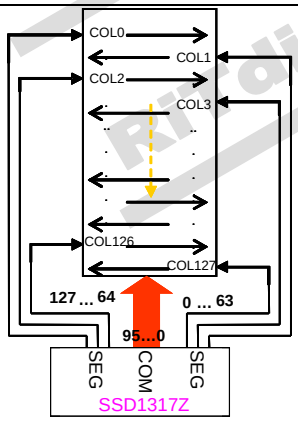
(4) Sequential SEG & SEG remap & left / right



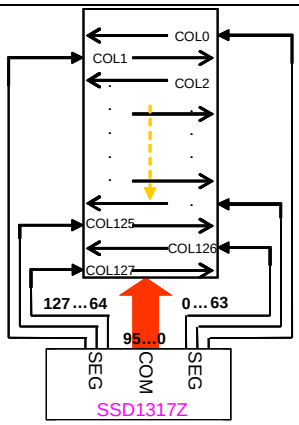
(5) Odd / even SEG



(6) Odd / even SEG & left / right



(7) Odd / even SEG & SEG remap



(8) Odd / even SEG & SEG remap & left / right

Note:

(1) The above eight figures are all with bump pads being faced up.

2.1.21 Set V_{COMH} Deselect Level (DBh)

This command adjusts the VCOMH regulator output. Please refer Table 1-1 for details.

2.1.22 NOP (E3h)

No Operation Command.

2.1.23 Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is called “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resumes from the “Lock” state, and the driver IC will then respond to the command and memory access.

2.2 Graphic Acceleration Command

2.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of seven consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page, scrolling speed, start column and end column.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1317 horizontal scroll is designed for 128 columns scrolling. The following figures (Figure 2-7, Figure 2-8, and Figure 2-9) show the examples of using the horizontal scroll:

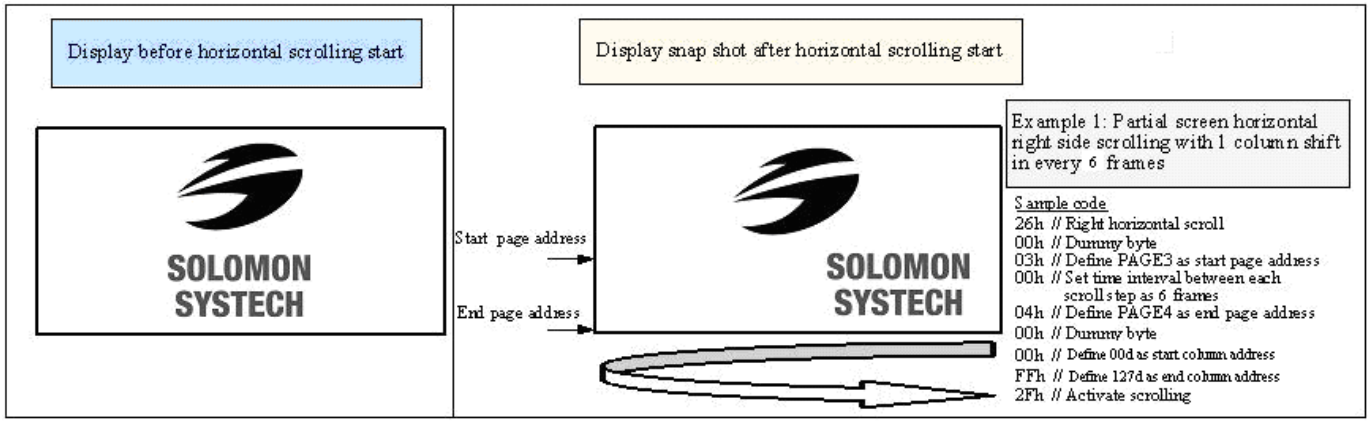
Figure 2-7 : Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	…	…	…	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126

Figure 2-8 : Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	…	…	SEG123	SEG124	SEG125	SEG126	SEG127	SEG0

Figure 2-9 : Horizontal scrolling setup example



2.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

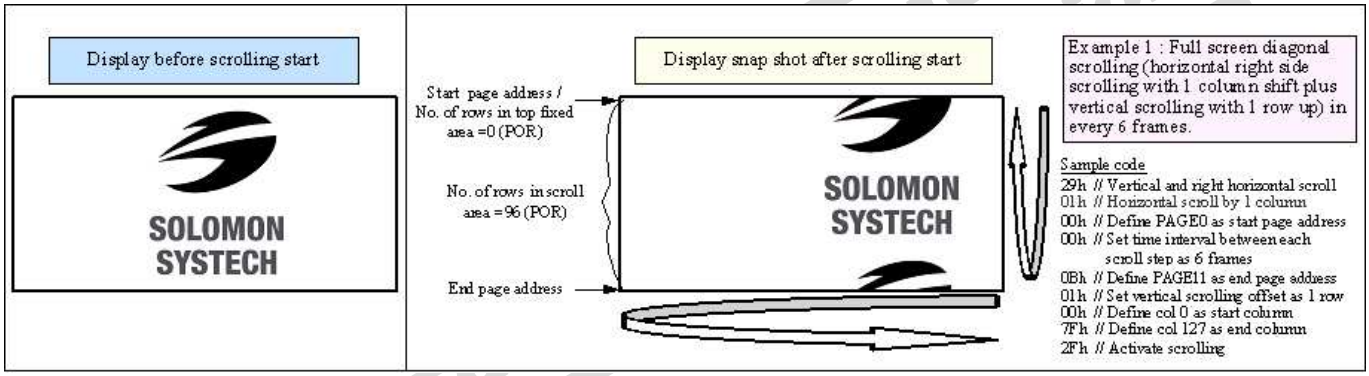
This command consists of seven consecutive bytes to set up the continuous vertical scroll parameters and determine the scrolling start page, end page, start column, end column, scrolling speed, horizontal and vertical scrolling offset.

If the vertical scrolling offset byte E[3:0] of command 29h / 2Ah is set to zero, then only horizontal scrolling is performed (like command 26/27h). On the other hand, if the number of column scroll offset byte A[0] is set to zero, then only vertical scrolling is performed.

Continuous diagonal (horizontal + vertical) scrolling would be enabled if both A[0] and E[3:0] are set to be non-zero, whereas full column diagonal scrolling mode is suggested by setting F[6:0]=00h and G[6:0]=7Fh.

Before issuing this command the scroll must be deactivated (2Eh), or otherwise, RAM content may be corrupted. The following figure (Figure 2-10) show the examples of using the continuous vertical and horizontal scroll.

Figure 2-10 : Continuous Vertical and Horizontal scrolling setup example



2.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

2.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands: 26h / 27h / 29h / 2Ah. The setting in the latest scrolling setup command overwrites the setting in the previous scrolling setup command.

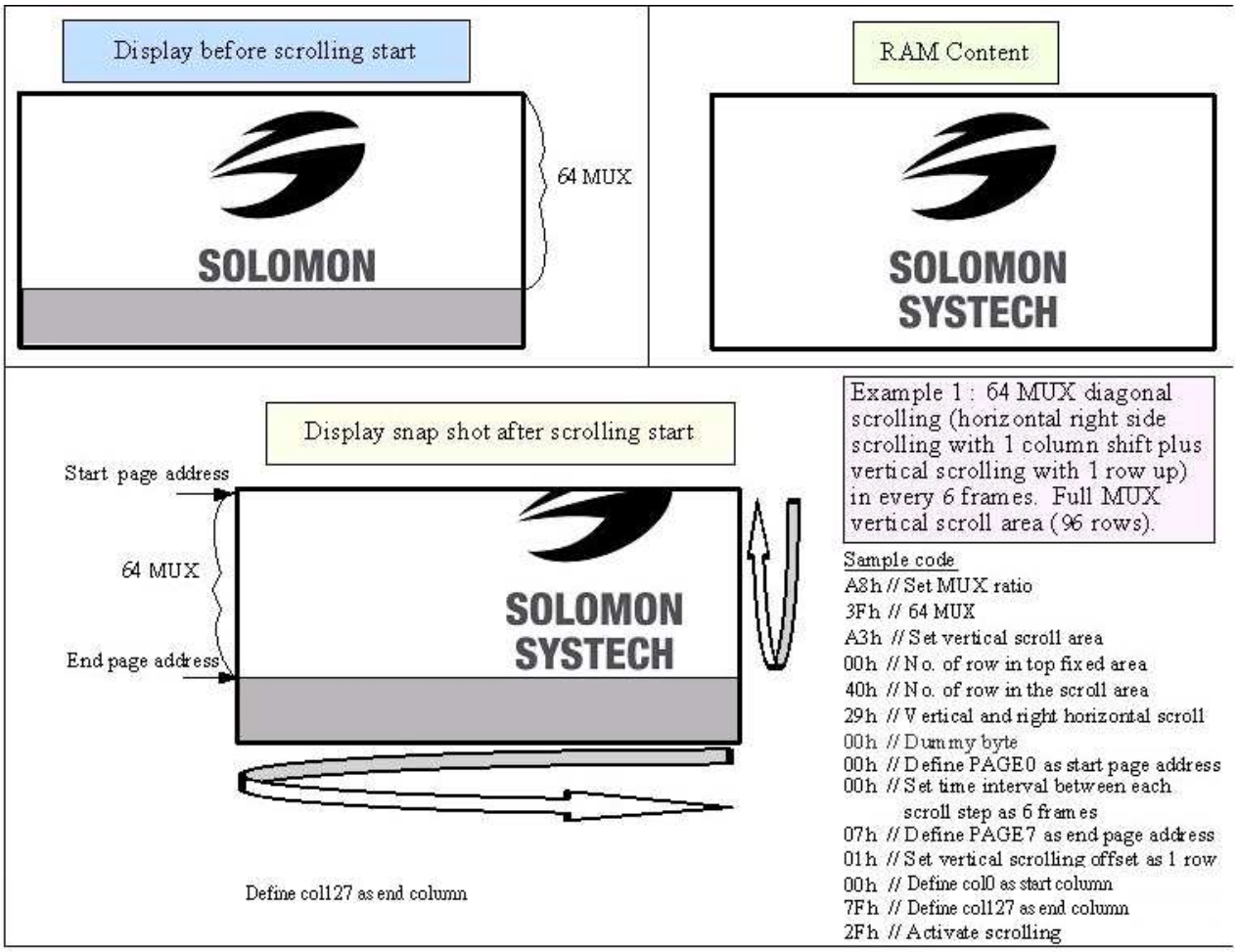
The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

2.2.5 Set Vertical Scroll Area (A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29h / 2Ah), the number of rows in the vertical scroll area can be set smaller than or equating to the MUX ratio. Figure 2-11 shows a vertical scrolling example with different settings in vertical scroll area.

Figure 2-11 : Vertical scroll area setup examples



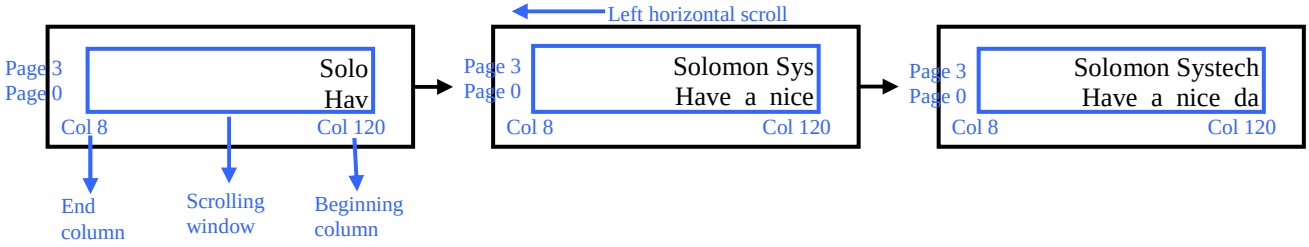
2.3 Advance Graphic Acceleration Command

2.3.1 Content Scroll Setup (2Ch/2Dh)

This command consists of seven consecutive bytes to set up the horizontal scroll parameters and determine the scrolling start page, end page, start column and end column. One column will be scrolled horizontally by sending the setting of command 2Ch / 2Dh once.

When command 2Ch / 2Dh are sent consecutively, a delay time of $2/FrameFreq$ must be set. Figure 2-12 shown an example of using 2Dh "Content Scroll Setup" command for horizontal scrolling to left with infinite content update. In there, "Col" means the graphic display data RAM column.

Figure 2-12: Content Scrolling example (2Dh, Left Horizontal Scroll by one column)



By using command 2Ch/2Dh, RAM contents are scrolled and updated by one column. Table 2-4 is an example of content scrolling setting of SSD1317 (eg. scrolling window of 4 pages). The values of registers depend on different conditions and applications.

Table 2-4 : Content Scrolling software flow example (Page addressing mode – command 20h, 02h)

Step	Action	D/C#	Code	Remarks
1	**For i= 1 to n**	-	-	Create "For loop" for infinite content scrolling
2	Set Content scrolling command (scrolling window : Page 0 to 3, Col 8 to Col 120)	0	2Dh	Left Horizontal Scroll by one column
		0	00h	A[7:0] : Dummy byte (Set as 00h)
		0	00h	B[3:0] : Define start page address
		0	01h	C[7:0] : Dummy byte (Set as 01h)
		0	03h	D[3:0] : Define end page address
		0	00h	E[7:0] : Dummy byte (Set as 00h)
		0	08h	F[6:0] : Define start column address
		0	78h	G[6:0] : Define end column address
3	Add Delay time of $2/FrameFreq$	-	-	E.g. Delay 20ms if frame freq ≈ 100Hz
4	Write RAM on the beginning column of the scrolling window			
	Write RAM on (Page0, Col 120) *(Content update in beginning column)*	0	B0h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page1, Col 120) *(Content update in beginning column)*	0	B1h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page2, Col 120) *(Content update in beginning column)*	0	B2h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
	Write RAM on (Page3, Col 120) *(Content update in beginning column)*	0	B3h	Set Page Start Address for Page Addressing Mode
		0	17h	Set Higher Column Start Address for Page Addressing Mode
		0	08h	Set Lower Column Start Address for Page Addressing Mode
		1	-	Write data to fill the RAM
5	i=i+1	-	-	Go to next "For loop"
	Delay timing	-	-	Set time interval between each scroll step if necessary
	End			

There are 3 different memory addressing mode in SSD1317: page addressing mode, horizontal addressing mode and vertical addressing mode and it is selected by command 20h. Table 2-4 is an example of content scrolling software flow under page addressing mode, while vertical addressing mode example is shown in below Table 2-5.

Table 2-5 : Content Scrolling setting example (Vertical addressing mode – command 20h, 01h)

Step	Action	D/C#	Code	Remarks
1	**For i= 1 to n**	-	-	Create "For loop" for infinite content scrolling
2	Set Content scrolling command (scrolling window : Page 0 to 3, Col 8 to Col 120)	0	2Dh	Left Horizontal Scroll by one column
		0	00h	A[6:0] : Dummy byte (Set as 00h)
		0	00h	B[3:0] : Define start page address
		0	01h	C[2:0] : Dummy byte (Set as 01h)
		0	03h	D[3:0] : Define end page address
		0	00h	E[6:0] : Dummy byte (Set as 00h)
		0	08h	F[6:0] : Define start column address
		0	78h	G[6:0] : Define end column address
3	Add Delay time of $2/FrameFreq$	-	-	E.g. Delay 20ms if frame freq ≈ 100Hz
4	Write RAM on the beginning column of the scrolling window (Page 0 to 3, Col 120) *(Content update in beginning column)*	0	21h	Set Column address
		0	78h	Set column start address for Vertical Addressing Mode
		0	78h	Set column end address for Vertical Addressing Mode
		0	22h	Set Page address
		0	00h	Set start page address for Vertical Addressing Mode
		0	03h	Set end page address for Vertical Addressing Mode
		1	-	Write data to fill the RAM
5	i=i+1	-	-	Go to next "For loop"
	Delay timing	-	-	Set time interval between each scroll step if necessary
	End			