



SH8501A

240RGBx240 / 16.7M color
AMOLED Display Driver IC

Datasheet

Preliminary Version 0.0

User Command Set

April, 2021

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Version History

April, 2021

Ver.	Date	Page	Description of Changes
Ver0.0	December. 2020		Initial Draft
Ver0.0	March. 24. 2021	p25, p26	Modify Figure 2, 3
Ver0.0	April. 1. 2021	P54, p57	Modify Figure 27, 31

1 General description

1.1 Introduction

This IC is used for driving a 240RGBx240 LTPS AMOLED for a bandable or wearable application. It supports a low voltage operation and single chip solution including 120 Source channels. All circuits are designed suitable for AMOLED display panel. For high-speed data transfer, the data for display and command are received via MIPI DSI with 2-lane. Also SH8501A supports MIPI DBI Type-B and Type-C interface. IC is connected to the Application Processor(AP) directly and stores display data into internal display GRAM which is sent from the AP. IC generates AMOLED driving signals by itself and stored display data can be performed with minimal power consumption. Also integrated Source driver, Panel Gate controller, GRAM, Power generation circuit, Voltage Regulator and Timing controller so on. The initialization settings can be partially or fully stored in the non-volatile memory(OTP) and these settings are loaded at the starting stage of display. This IC provides a high-performance and higher display quality using minimum number of external components for lower power consumption and saving design cost and space.

- MIPI: Mobile Industry Processor Interface
- DSI: Display Serial Interface
- DBI: Display Bus Interface

1.2 Ordering information

- Product Code: SH8501A
- Package: COF/COG

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1.3 Features

Features	Description	
Device Type	LTPS AMOLED Driver IC	
Display Resolution	Max. 240 RGB (H) x 240+ (V)	
	Support 1:6 MUX Operation	
	2 Line Horizontal x 2 Line Vertical Control Step	
Color Depth	16M Colors	
Display Type	Panel Type	AMOLED – Rigid & Flexible
	Pixel Arrangement	Real RGB, Delta RGB
	Source Output	120CH with MUX
	GOA for Gate Output	GOAR[16:1], GOAL[16:1]
	Support P-MOS Type Panel	
Interface	High Speed Interface	MIPI (DSI), Data 2 Lane, Clock 1 Lane Maximum bit rate: 250Mbps@1lane Maximum bit rate: 125Mbps@2lane
	D-PHY Version	v1.0
	DSI Version	v1.02
	Polarity Inversion of MIPI Pins	
	Support Command Mode and Video mode	
	MIPI DBI Type-B (MPU 8-bit) and Type-C (3/4-wire mode), Quad-SPI	
Display Features	RGB separated gamma	
	CRP, ACL, HBM	
One Time Programmable Device (OTP)	Program Voltage Supply	Only External Mode
	Size	8K x 8bit (3times Re-writable)
	Built-in	Gamma, Chip ID, MCS register
On-chip Functions	Internal DC/DC Voltage Converter	
	Timing Generator	
	Adjustable Gamma Curves (Separated R/G/B)	
External Supply Voltages	Interface Power	VDDI = 1.8 V (1.65 V to 3.3 V)
	Analog Power	VCI = 2.8 V (2.7 V to 3.6 V)
Internal Drive Supply Voltages	VDD	1.2 V
	AVDD	4.6V to 6.5V
	VCL	-5.0V to -2.7V
	VLOUT2	4.6V to 13.0V
	VLOUT3	-13.0V to -4.6V
	VGH	5.0V to 10.0V

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	VGL	-10.0V to -5.0V
	UELVD	3.0V to 5.0V
	UELVS	-4.0V to -0V
	VINT	-4.5V to -0.2V
	VREFP	0.2V to 5.0V
	VREGOUT	2.0V to 6.2V
	VGS	0.0V to 3.3V
COF/COG Package		
Operating Temperature	-40 °C to + 85 °C	
Storage Temperature	-55 °C to + 125 °C	

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1.4 PAD Description

1.4.1 Power Supply Part

Table 1 PADs for Power Supply

Symbol	I/O	Item	Function Description	Condition
VDDI	P	Voltage Range	Typ. = 1.80V (Min. = 1.65V, Max. = 3.3V)	
		Unused	Required	
		Component	Capacitor	
		Description	Power supply for I/O block provided from outside VDDI < 0.05V (When power is turned off)	
VCI	P	Voltage Range	Typ. = 2.8V (Min. = 2.70V, Max. = 3.60V)	
		Unused	Required	
		Component	Capacitor	
		Description	Power Supply for Analog Circuits VCI < 0.05V (When power is turned off)	
VOTP	P	Voltage Range	Typ. = 7.25V (Min. = 7.0V, Max. = 7.5V)	
		Unused	Open	
		Description	External Voltage Input for OTP Data Program	
VSSI	P	Description	GND for I/O Block provided from outside (VSSI = 0V)	
VSS	P	Description	GND for Logic Block (VSS = 0V)	
VSS_OSC	P	Description	GND for OSC Block (VSS_OSC = 0V)	
VSS_MIPI	P	Description	GND for MIPI DSI receiver (VSS_MIPI = 0V)	
VSSA	P	Description	GND for Analog circuits (VSSA = 0V)	
VSSS	P	Description	GND for Source Driver circuits (VSSS = 0V)	
VSSC	P	Description	GND for DCDC block (VSSC = 0V)	

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1.4.2 Analog Part

Table 2 PADs for Analog Power

Symbol	I/O	Item	Function Description	Condition
VDD	O	Voltage Range	Typ. = 1.2V	RVDD_ON = VDDI
		Unused	Required	
		Component	Capacitor	
		Description	Voltage Regulator Output for Internal Logic/Memory/DPHY Circuit Do not apply any external power to this pad.	
VREF	O	Voltage Range	2.2V	
		Unused	Required	
		Component	Capacitor	
		Description	Reference Voltage Output for Internal Test	
AVDD	O	Voltage Range	Min. = 4.6V Max. = 6.5V	AVDD-VREGOUT = Min.0.3V
		Component	Capacitor	
		Description	Power supply for Source Driver and VLOUT2/3 Booster Power	
C11P C11N	O	Voltage Range	Min. = 0.0V Max. = 6.5V	
		Unused	Open	
		Component	Capacitor	
		Description	Connect the charge-pumping capacitor for generating AVDD level.	
C12P C12N	O	Voltage Range	Min. = 0.0V Max. = 6.5V	
		Unused	Open	
		Component	Capacitor	
		Description	Connect the charge-pumping capacitor for generating AVDD level.	
VCL	O	Voltage Range	Min. = -5.0V Max. = -2.7V	
		Component	Capacitor	
		Description	Power supply for UELVSS and VINT and VLOUT3 Booster Power	
C31P C31N	O	Voltage Range	Min. = -5.0V Max. = 6.5V	
		Unused	Open	
		Component	Capacitor	
		Description	Connect the charge-pumping capacitor for generating VCL level.	
C32P C32N	O	Voltage Range	Min. = -5.0V Max. = 6.5V	
		Unused	Open	

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Symbol	I/O	Item	Function Description	Condition
		Component	Capacitor	
		Description	Connect the charge-pumping capacitor for generating VCL level.	
VLOUT2	O	Voltage Range	Min. = AVDD Max. = AVDD x 2	VLOUT2-VGH = Min.2.0V
		Component	Capacitor	
		Description	Power Supply for VGH	
C41P C41N	O	Voltage Range	Min. = 0.0V Max. = AVDD x 2	
		Unused	Open	
		Component	Capacitor	
		Description	Connect the charge-pumping capacitor for generating VLOUT2 level.	
VLOUT3	O	Voltage Range	Min. = -AVDD x 2 Max. = -AVDD	VLOUT3-VGL = Min. 2.0V
		Component	Capacitor	
		Description	Power Supply for VGL	
C51P C51N	O	Voltage Range	Min. = -AVDD x 2 Max. = AVDD x 2	
		Unused	Open	
		Component	Capacitor	
		Description	Connect the charge-pumping capacitor for generating VLOUT3 level.	
VREGOUT	O	Voltage Range	Min. = 2.0V Max. = 6.2V	lower than AVDD – 0.3V
		Unused	Required	
		Component	Capacitor(optional)	
		Description	Reference High Voltage Output for Grayscale Voltage Generator. Internal register can be used to adjust the voltage.	
VGS	O	Voltage Range	Min. = 0.0V Max. = 3.3V	
		Unused	Required	
		Component	Capacitor(optional)	
		Description	Reference Low Voltage Output for Grayscale Voltage Generator. Internal register can be used to adjust the voltage.	
VGH	O	Voltage Range	Min. = 5.0V Max. = 10.0V	–
		Unused	Required	
		Component	Capacitor	
		Description	Reference High Voltage Output for Gate Driver.	

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Symbol	I/O	Item	Function Description	Condition
			Internal register can be used to adjust the voltage.	
VGL	O	Voltage Range	Min. = -10.0V Max. = -5.0V	—
		Unused	Required	
		Component	Capacitor	
		Description	Reference Low Voltage Output for Gate Driver Internal register can be used to adjust the voltage.	
VINT	O	Voltage Range	Min. = -4.5V Max. = -0.2V	
		Unused	Required	
		Component	Capacitor	
		Description	Negative Reference Voltage Output for Pixel Initialization Internal register can be used to adjust the voltage.	
VREFP	O	Voltage Range	Min. = 0.2V Max. = 5.0V	
		Unused	Required	
		Component	Capacitor	
		Description	Positive Reference Voltage Output for Pixel Initialization Internal register can be used to adjust the voltage.	
ELVDD	O	Voltage Range	Min. = 3.0V Max. = 5.0V	
		Unused	Required	
		Component	Capacitor	
		Description	Panel Positive Power in AOD Mode Internal register can be used to adjust the voltage.	
ELVSS	O	Voltage Range	Min. = -4.0V Max. = -0.0V	
		Unused	Required	
		Component	Capacitor	
		Description	Panel Negative Power in AOD Mode Internal register can be used to adjust the voltage.	

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1.4.3 Logic Part

Table 3 PADS for Logic Interface

Symbol	I/O	Item	Function Description	Condition
CKP/CKN	I	Voltage Range	Min. = -50mV Max. = 1.30V	
		Unused	Fix to VSS_MIPi.	
		Description	Differential Clock Input Pins These pins always receive high speed clock when MIPI activates in high speed data transmission mode.	
D0P/D0N	I/O	Voltage Range	Min. = -50mV Max. = 1.30V	
		Unused	Fix to VSS_MIPi.	
		Description	Differential Data Input/Output Pins When forward link activates, these pins receive data from host. When reverse link activates, these pins transmit data to host.	
D1P/D1N	I/O	Voltage Range	Min. = -50mV Max. = 1.30V	
		Unused	Fix to VSS_MIPi.	
		Description	Differential Data Input/Output Pins When forward link activates, these pins receive data from host. When reverse link activates, these pins transmit data to host.	
S<120:1>	O	Voltage Range	Min. = 0.0V Max. = 6.5V	
		Unused	Open	
		Description	Source Driver Output Pins	
GOAR<16:1>	O	Voltage Range	Min. = -10.0V Max. = 10.0V	
		Unused	Open	
		Description	This pin used to panel control.	
GOAL<16:1>	O	Voltage Range	Min. = -10.0V Max. = 10.0V	
		Unused	Open	
		Description	This pin used to panel control.	
IM[1:0]	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	This pin used to interface mode control.	
RESX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Required	
		Description	This signal is used to reset the device and must be applied to	

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Symbol	I/O	Item	Function Description	Condition
			initialize the chip properly. Active Low	
CSX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or be left open, internal pull-up	
		Description	Chip Select Signal in MIPI DBI Type-B(MPU) and Type-C(SPI) Active Low	
DCX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Data is selected if DCX is high in MIPI DBI Type-B(MPU) and Type-C(SPI). Otherwise command is selected. Serial Data Input in Dual-SPI Serial Data Input in Quad-SPI Please reference to 4.1 Interface Type Selection	
SCL_WRX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Synchronous Clock Signal in MIPI DBI Type-B(MPU) and Type-C(SPI)	
SDI_RDX	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Serial Data Input in MIPI DBI Type-C(SPI) Synchronous Clock Signal in MIPI DBI Type-B(MPU) Please reference to 4.1 Interface Type Selection	
SDO	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Serial Data Output in MIPI DBI Type-C(SPI) Please reference to 4.1 Interface Type Selection	
DB0_SDI2	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Serial Data Input in Quad-SPI or MIPI DBI Type-B(MPU) Please reference to 4.1 Interface Type Selection	
DB1_SDI3	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Serial Data Input in Quad-SPI or MIPI DBI Type-B(MPU) Please reference to 4.1 Interface Type Selection	

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Symbol	I/O	Item	Function Description	Condition																																								
PSWAP DSWAP	I	Voltage Range	Min. = VSSI Max. = VDDI																																									
		Unused	Fix to VSSI																																									
		Description	PSWAP controls polarity of MIPI Lane and DSWAP select MIPI lane sequence																																									
			<table><tr><th>PSWAP</th><th>DSWAP</th><th>D0P</th><th>D0N</th><th>CKP</th><th>CKN</th><th>D1P</th><th>D1N</th></tr><tr><td rowspan="2">0</td><td>0</td><td>D0P</td><td>D0N</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td></tr><tr><td>1</td><td>D1P</td><td>D1N</td><td>CKP</td><td>CKN</td><td>D0P</td><td>D0N</td></tr><tr><td rowspan="2">1</td><td>0</td><td>D0N</td><td>D0P</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td></tr><tr><td>1</td><td>D1N</td><td>D1P</td><td>CKN</td><td>CKP</td><td>D0N</td><td>D0P</td></tr></table>				PSWAP	DSWAP	D0P	D0N	CKP	CKN	D1P	D1N	0	0	D0P	D0N	CKP	CKN	D1P	D1N	1	D1P	D1N	CKP	CKN	D0P	D0N	1	0	D0N	D0P	CKN	CKP	D1N	D1P	1	D1N	D1P	CKN	CKP	D0N	D0P
			PSWAP	DSWAP	D0P	D0N	CKP	CKN	D1P	D1N																																		
0	0		D0P	D0N	CKP	CKN	D1P	D1N																																				
	1		D1P	D1N	CKP	CKN	D0P	D0N																																				
1	0	D0N	D0P	CKN	CKP	D1N	D1P																																					
	1	D1N	D1P	CKN	CKP	D0N	D0P																																					
DB[7:2]	I	Voltage Range	Min. = VSSI Max. = VDDI																																									
		Unused	Open																																									
		Description	Data Input MIPI DBI Type-B																																									
ERR_FG	O	Voltage Range	Min. = VSSI Max. = VDDI																																									
		Unused	Open																																									
		Description	Purpose on Test for MIPI Status																																									
TE	O	Voltage Range	Min. = VSSI Max. = VDDI																																									
		Unused	Open																																									
		Description	Monitor Pin of TE (Tearing Effect) Logic Signal When this pad is not activated, this signal stays low.																																									
EL_CTRL	O	Voltage Range	Min. = VSSI Max. = VDDI																																									
		Unused	Open																																									
		Description	PMIC Control Signal																																									

1.4.4 Test and Dummy Part

Table 4 PADs for Test and Dummy

Symbol	I/O	Item	Function Description	Condition
RVDD_ON	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI	
		Description	Logic/Memory/DPHY Power Regulator ON/OFF Control Purpose on Internal Test	
TMODE[3:0]	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or be left open, internal pull-up	
		Description	Purpose on Internal Test	
OTP_NOLOAD	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VSSI or be left open, internal pull-down	
		Description	Purpose on Internal Test	
IM[2]	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VSSI or be left open, internal pull-down	
		Description	Purpose on Internal Test	
EXTCLK	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VSSI or be left open, internal pull-down	
		Description	Purpose on Internal Test	
BIST	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VSSI or be left open, internal pull-down	
		Description	Purpose on Internal Test	
TEST_IN	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VSSI or be left open, internal pull-down	
		Description	Purpose on Internal Test	
AVDD_MODE	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VSSI or be left open, internal pull-down	
		Description	Purpose on Internal Test	
IMON	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	

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Symbol	I/O	Item	Function Description	Condition
		Description	Purpose on Internal Test	
VMON	I	Voltage Range	Min. = V _{LOUT3} Max. = V _{CI}	
		Unused	Open	
		Description	Purpose on Internal Test	
TEST_OUT1	O	Voltage Range	Min. = V _{SSI} Max. = V _{DDI}	
		Unused	Open	
		Description	Purpose on Internal Test	
TEST_OUT2	O	Voltage Range	Min. = V _{SSI} Max. = V _{DDI}	
		Unused	Open	
		Description	Purpose on Internal Test	
OSC_FUSE	O	Voltage Range	Min. = V _{SSI} Max. = V _{DDI}	
		Unused	Open	
		Description	Purpose on Internal Test	
EL_EN	O	Voltage Range	Min. = V _{SSI} Max. = V _{DDI}	
		Unused	Open	
		Description	Purpose on Internal Test	
DB[15:8]	I	Voltage Range	Min. = V _{SSI} Max. = V _{DDI}	
		Unused	Open	
		Description	Purpose on Internal Test	
DUMMY	I	Voltage Range	floating	
		Unused	Tied to V _{INT} or V _{GL} or V _{GH} on COF film.	
		Description	Dummy PAD	
SD_PASS_L1 SD_PASS_L2 SD_PASS_R1 SD_PASS_R2	I	Voltage Range	floating	
		Unused	Open	
		Description	Dummy PAD	

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

It defines the maximum operating conditions. The reliability of IC is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage for I/O Block	VDDI-VSS	– 0.3 to + 3.6	V
Supply Voltage for Step-up Circuit	VCI-VSS	– 0.3 to + 4.0	V
AMOLED Supply Voltage Range	AVDD-VSS	– 0.3 to + 6.5	V
	VSS-VCL	– 0.3 to + 5.5	V
	VSS-VINT	– 0.3 to + 5.0	V
	VLOUT2-VSS	– 0.3 to + 16.5	V
	VSS-VLOUT3	– 0.3 to + 16.5	V
	VGH-VSS	– 0.3 to + 11	V
	VSS-VGL	– 0.3 to + 11	V
	ELVDD – VSS	– 0.3 to + 5.5	V
	VSS- ELVSS	– 0.3 to + 4.4	V
	VLOUT2-VLOUT3	– 0.3 to + 33	V
Supply Voltage for OTP	VOTP-VSS	– 0.3 to + 7.5	V
Input Voltage Range	V _{in}	– 0.3 to VDDI + 0.3	V
Storage Temperature	T _{stg}	– 55 to + 125	°C

NOTE: Conditions outside the range listed in the above table may cause permanent damage to the device, may not be recovered. It is strongly recommended to use the IC within the limits of its electrical characteristics during normal operation. Absolute voltages are referenced to ground. The functional operation of the device is not implied for these conditions.

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2.2 DC Electrical Characteristics

2.2.1 DC Characteristics for Power Supply

Table 6 DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Application Pin	Unit	Note
			Min.	Typ.	Max.			
Power supply voltage	VDDI		1.65	1.8	3.3	VDDI	V	
	VCI		2.7	2.8	3.6	VCI		
	VOTP		7.0	7.25	7.5	VOTP		

NOTE: TA = -40 to 85 °C

2.2.2 DC Characteristics for Generated Voltage

Table 7 DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit	Note
			Min.	Typ.	Max.		
Operation voltage	VREGOUT	$VREGOUT < AVDD - 0.3 V$	2.0	—	6.2	V	
	VGS		0	—	3.3		
	VINT	$VINT > VCL + 0.5V$	-4.5	—	-0.2		
	VREFP	$VREFP < AVDD - 0.3 V$	0.2	—	5.0		
	VGH	$VGH < VLOUT2 - 2.0V$	5.0	—	10.0		
	VGL	$VGL > VLOUT3 + 2.0V$	-10.0	—	-5.0		
	AVDD	$VCI \times 2$	4.6	—	6.5		
	VCL	$-VCI, -VCI \times 2$	-5.0	—	-2.7		
	VLOUT2	$ VLOUT2 - VLOUT3 < 30 V$	4.6	—	13		
	VLOUT3		-13	—	-4.6		

NOTE: TA = -40 to 85 °C

2.2.3 DC Characteristics for Interface

Table 8 DC Characteristic for Interface Signals

Parameter	Symbol	Condition	Specification			Pin	Unit
			Min.	Typ.	Max.		
Logic high level input voltage	VIH_IO1	–	$0.8 \times VDDI$	–	VDDI	RESX	V
Logic low level input voltage	VIL_IO1	–	0.0	–	$0.2 \times VDDI$		
Logic high level output voltage	VOH_IO1	IOUT = – 1 mA	$0.8 \times VDDI$	–	VDDI	TE	
Logic low level output voltage	VOL_IO1	IOUT = + 1 mA	0.0	–	$0.2 \times VDDI$		
Input high level leakage current	IIH	VIN = VDDI	–	–	1	RESX	μA
Input low level leakage current	IIL	VIN = VSS	– 1	–	–		

NOTE: TA = – 40 to 85 °C

2.2.4 Power Consumption

Table 9 Power Consumption

Parameter	Symbol	Condition	Specification			Unit	Note
			Min.	Typ.	Max.		
Operating current (DSI, dynamic display)	IVDDI _{op}	Frame frequency = 60 Hz No load SR_SET = 5'b10110 SPR Function OFF	—	—	2.0	mA	(NOTE)
	IVCI _{op}		—	—	4.0		
Sleep current	IVDDI _{LP}	LP11 mode	—	—	200	uA	
	IVCI _{LP}		—	—	20		
	IVDDI _{ULPS}	ULPS mode	—	—	180	uA	
	IVCI _{ULPS}		—	—	20		
Deep standby current	IVDDI _{DSLP}		—	—	4	uA	
	IVCI _{DSLP}		—	—	2		

NOTE: The table above shows only driver IC's power consumption. (MIPI I/F @0.25Gbps, white pattern).
 VCI = 2.8V, VDDI = 1.8V, TA = 25 °C.

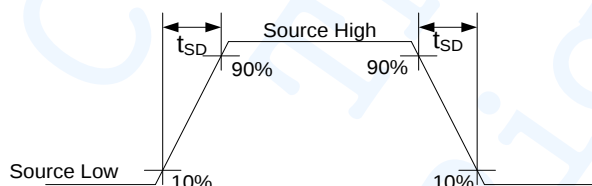
2.2.5 DC Characteristics for Internal Circuits

Table 10 DC Characteristics for Internal Circuits

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency	$F_{oscTA25}$	$T_A = 25\text{ }^{\circ}\text{C}$	10.67	11	11.3 3	MHz	
Voltage efficiency of Step-up output	AVDD	$I_{AVDD} = -5.0\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	90	—	—	%	
	VCL	$I_{VCL} = +3.0\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	90	—	—		
	VLOUT2	$I_{VLOUT2} = -0.5\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	90	—	—		
	VLOUT3	$I_{VLOUT3} = +0.5\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	90	—	—		
Panel driving voltage	VGH	$I_{VGH} = -0.5\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	Target - 0.1	Target	—	V	
	VGL	$I_{VGL} = +0.5\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	Target - 0.1	Target	—		
	VINT	$I_{VINT} = +0.5\text{mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	Target - 0.1	Target	—		
Output on resistance of Gate driver	R_{onvgh}	$VGH = 6.6\text{ V}$	—	—	2	$k\Omega$	
	R_{onvgl}	$VGL = -8.0\text{ V}$	—	—	2		
Delay, Source driver	t_{SD}	AVDD = 5.6 V VREGOUT = 5.0 V VGS = 2.0 V SR_SET = 5'b101110	—	—	1.8	μs	(1)
Source output voltage deviation: mean value (channel to channel)	ΔV_o	$VSS + 1.0\text{V} < V_{so} < AVDD - 1.0\text{ V}$	—	—	± 5	mV	(2)

NOTE: $T_A = -40$ to $85\text{ }^{\circ}\text{C}$ Unless Otherwise Specified

1. Measurement condition (Delay Measurement of Source Driver), EDS load (0.1k,100pF)



2. SR_SET=5b'101110, Offset cancellation condition=ON

2.2.6 DC Characteristics for Reset

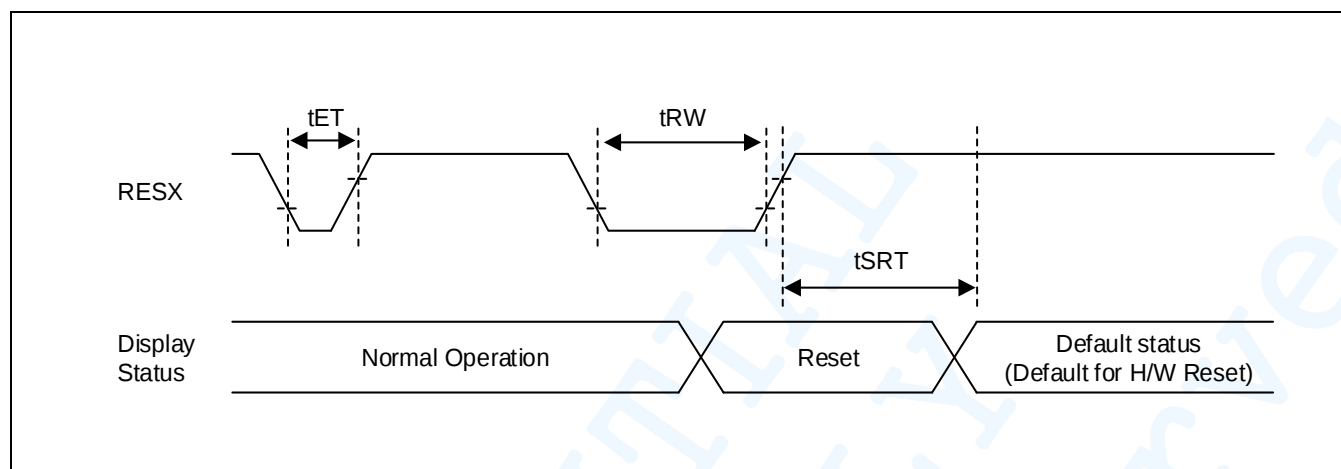


Figure 1 Reset Input Timing

Table 11 Reset Input Timing

Parameter	Symbol	Pad	Min.	Typ.	Max.	Unit	Note
Reset low pulse width	t_{RW}	RESX	10	—	—	μs	—
Secure reset completion time	t_{SRT}	RESX	—	—	5	ms	Reset during Sleep In mode
		RESX	—	—	150		Reset during Sleep Out mode
Reset un-reacted pulse width	t_{ET}	RESX			5	μs	—

NOTE:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Table 12 RESX Pulse

RESX Pulse	Action
Shorter than 5 μs	Reset rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset start

2. During the reset period, the display will be blanked (The display is entering blanking sequence, for which the maximum time is 60ms, when Reset starts in Sleep Out-mode. The display remains in the blank state in Sleep In-mode) and then return to Default condition for H/W reset.
3. During Reset Completion Time, ID bytes (or similar) value in OTP will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (t_{SRT}) within 5ms after a rising edge of RESX.

2.3 AC Characteristics

2.3.1 MIPI DBI Type-C – Option1 (SPI 3 Wire)

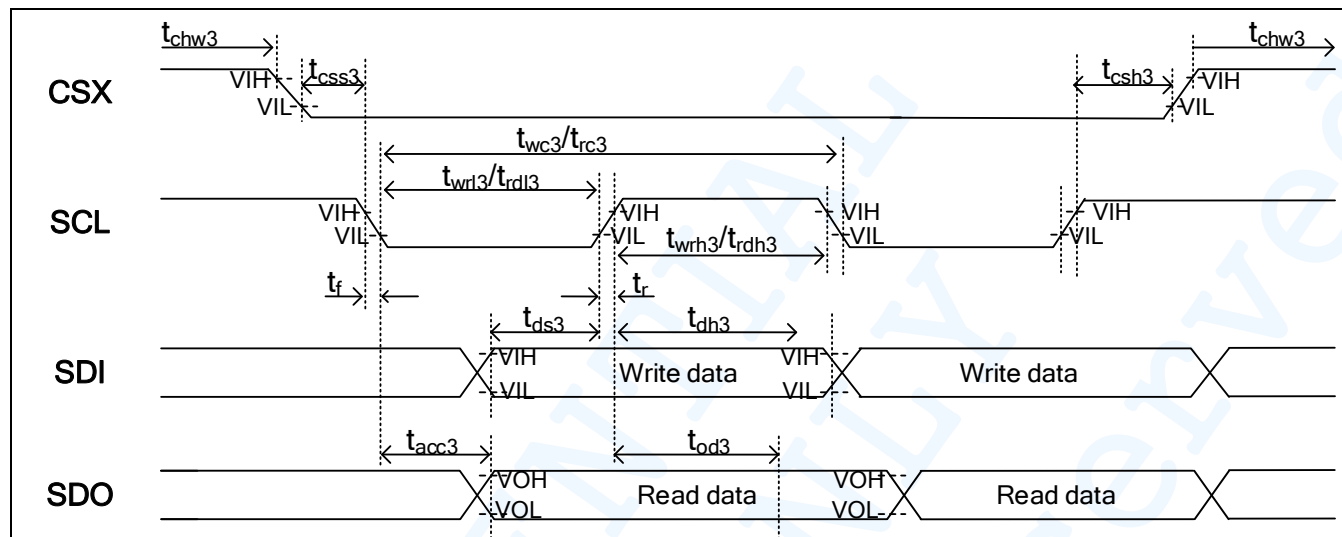


Figure 2 3 Wire 9bit Serial Interface Characteristics

Table 13 AC Characteristics of MIPI DBI Type-C – Option1 (SPI 3 Wire)

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{css3}	10	–	ns
Chip select hold time		t_{csh3}	10	–	ns
Chip select “High” pulse width		t_{chw3}	20	–	ns
Write cycle time	SCL (Write)	t_{wc3}	20	–	ns
SCL “High” period (Write)		t_{wrh3}	10	–	ns
SCL “Low” period (Write)		t_{wrl3}	10	–	ns
Read cycle time	SCL (Read)	t_{rc3}	100	–	ns
SCL “High” period (Read)		t_{rdh3}	50	–	ns
SCL “Low” period (Read)		t_{rdl3}	50	–	ns
Data setup time	SDI	t_{ds3}	10	–	ns
Data hold time		t_{dh3}	10	–	ns
Access time	SDO	t_{acc3}	–	40	ns
Output disable time		t_{od3}	20	–	ns
Rise/Fall time	–	t_r/t_f	–	1	ns

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2.3.2 MIPI DBI Type-C – Option3 (SPI 4 Wire)

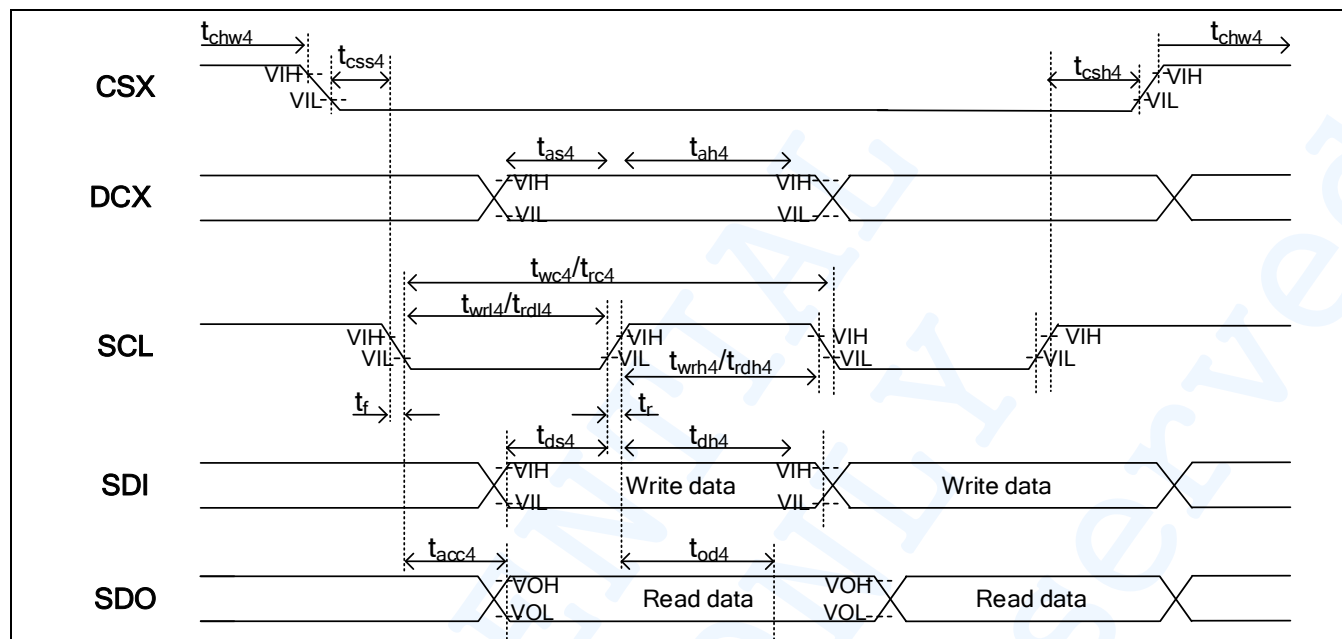


Figure 3 4 Wire 8bit Serial Interface Characteristics

Table 14 AC Characteristics of MIPI DBI Type-C – Option3 (SPI 4 Wire)

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{css4}	10	–	ns
Chip select hold time		t_{csh4}	10	–	ns
Chip select “High” pulse width		t_{ch4}	20	–	ns
Address setup time	DCX	t_{as4}	10	–	ns
Address hold time(Write/Read)		t_{ah4}	10	–	ns
Write cycle time	SCL (Write)	t_{wc4}	20	–	ns
SCL “High” period (Write)		t_{wrh4}	10	–	ns
SCL “Low” period (Write)		t_{wr4}	10	–	ns
Read cycle time	SCL (Read)	t_{rc4}	100	–	ns
SCL “High” period (Read)		t_{rdh4}	50	–	ns
SCL “Low” period (Read)		t_{rd4}	50	–	ns
Data setup time	SDI	t_{ds4}	10	–	ns
Data hold time		t_{dh4}	10	–	ns
Access time	SDO	t_{acc4}	–	40	ns
Output disable time		t_{od4}	20	–	ns
Rise/Fall time	–	t_r/t_f	–	1	ns

2.3.3 Quad SPI

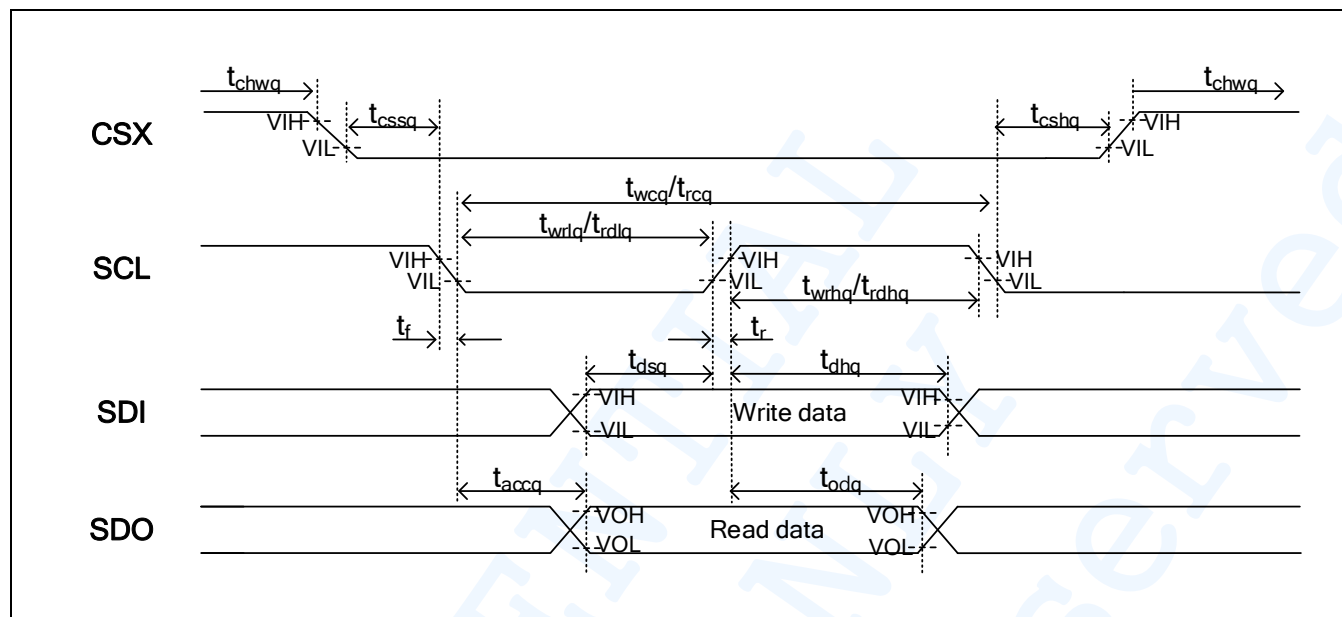


Figure 4 Quad Serial Interface Characteristics

Table 15 AC Characteristics of Quad SPI

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{cssq}	10	—	ns
Chip select hold time		t_{cshq}	10	—	ns
Chip select "High" pulse width		t_{chwq}	20	—	ns
Write cycle time	SCL (Write)	t_{wcq}	20	—	ns
SCL "High" period (Write)		t_{wrhq}	10	—	ns
SCL "Low" period (Write)		t_{wrlq}	10	—	ns
Read cycle time	SCL (Read)	t_{rcq}	100	—	ns
SCL "High" period (Read)		t_{rdhq}	50	—	ns
SCL "Low" period (Read)		t_{rdlq}	50	—	ns
Data setup time	SDI	t_{dsq}	10	—	ns
Data hold time		t_{dhq}	10	—	ns
Access time	SDO	t_{accq}	—	40	ns
Output disable time		t_{odq}	20	—	ns
Rise/Fall time	—	t_r/t_f	—	1	ns

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2.3.4 MIPI DBI Type-B (MPU 8bit)

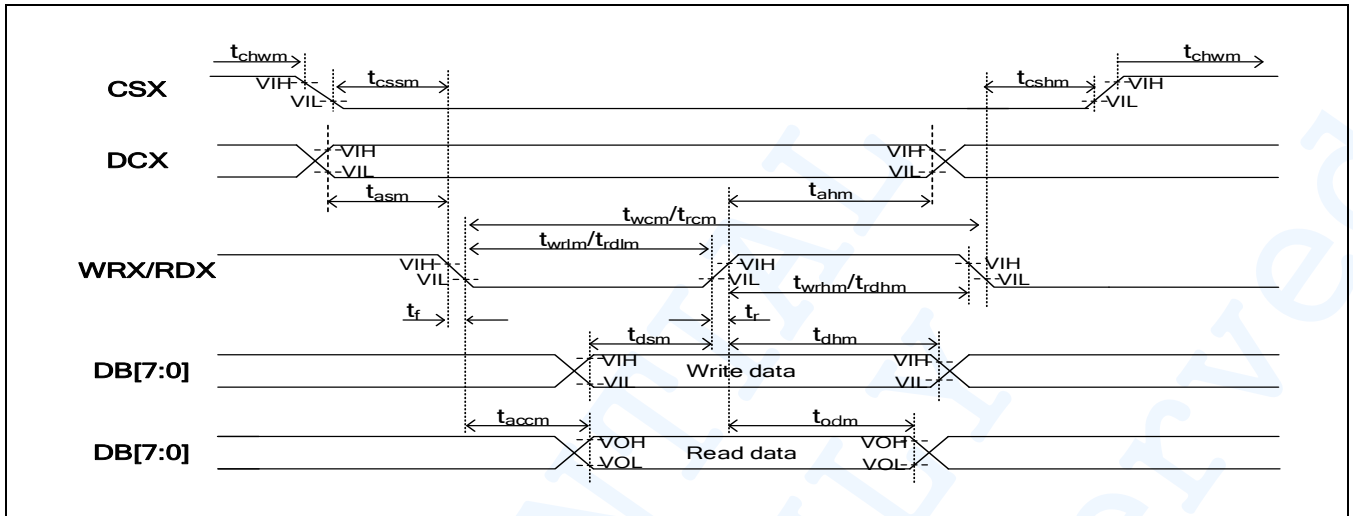


Figure 5 MPU Interface Characteristics

Table 16 AC Characteristics of MPU

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{cssm}	10	—	ns
Chip select hold time		t_{cshw}	10	—	ns
Chip select "High" pulse width		t_{chwm}	20	—	ns
Address setup time	DCX	t_{asm}	10	—	ns
Address hold time(Write/Read)		t_{ahm}	10	—	ns
Write cycle time	WRX (Write)	t_{wcm}	20	—	ns
WRX "High" period (Write)		t_{wrhm}	10	—	ns
WRX "Low" period (Write)		t_{wrlm}	10	—	ns
Read cycle time (Register Read)	RDX (Register Read)	t_{rcm}	100	—	ns
RDX "High" period (Register Read)		t_{rdhm}	50	—	ns
RDX "Low" period (Register Read)		t_{rdlm}	50	—	ns
Data setup time	DB[7:0]	t_{dsm}	10	—	ns
Data hold time		t_{dhm}	10	—	ns
Access time	DB[7:0]	t_{accm}	—	40	ns
Output disable time		t_{odm}	20	—	ns
Rise/Fall time	-	t_r/t_f	—	1	ns

2.4 MIPI Characteristics

2.4.1 DC Characteristics for MIPI DSI

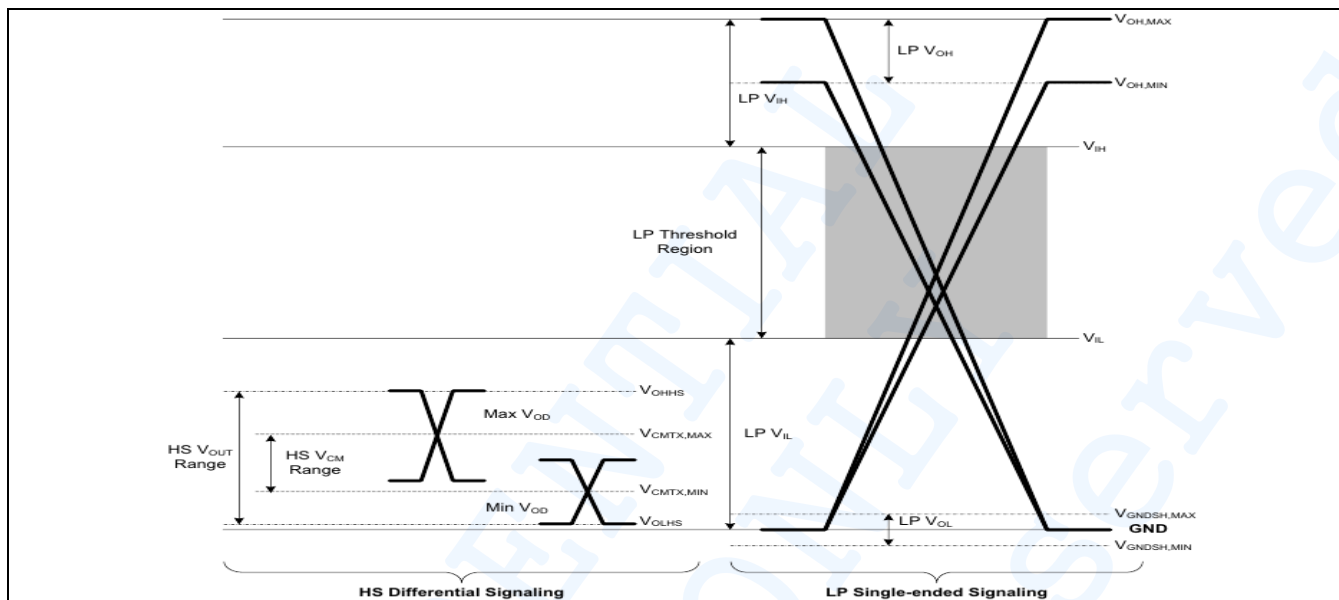


Figure 6 MIPI D-PHY Signaling Levels

Table 17 MIPI DSI DC Characteristic

Item		Symbol	Min.	Typ.	Max.	Unit	Note
HS_RX	Differential input high threshold	V_{IDTH}	–	–	70	mV	
	Differential input low threshold	V_{IDTL}	– 70	–	–		
	Single-ended input high voltage	V_{IHHS}	–	–	460		
	Single-ended input low voltage	V_{ILHS}	– 40	–	–		
	Single-ended threshold for HS termination enable	$V_{TERM-EN}$	–	–	450		
	Common-mode voltage HS receive mode	$V_{CMRX (DC)}$	70	–	330		1
	Differential input impedance	Z_{ID}	80	100	125	Ω	2
LP_RX	Logic0 voltage not in ULP State	V_{IL}	–	–	550	mV	
	Logic1 input voltage	V_{IH}	880	–	–		
	I/O leakage current	I_{LEAK}	-10	–	10	μA	
LP_TX	Thevenin output low level	V_{OL}	– 50	–	50	mV	
	Thevenin output high level	V_{OH}	1.1	–	1.3	V	
	Output impedance of LP transmitter	Z_{OLP}	110	–	–	Ω	2

NOTE:

- $V_{CMRX (DC (DC))} = (V_{DP} + V_{DN}) / 2$
- COG resistance is excluded (contact resistance and ITO wiring resistance). The values are tentative.

2.4.2 MIPI Line Contention Detection

The Low-Power receiver and a separate contention detector shall be used in a bi-directional data Lane to monitor the line voltage on each low-power signal. The low-power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than V_{IL} . The contention detector shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD} . An LP low fault shall not be detected when the pin voltage is less than V_{ILCD} .

The LP-CD threshold voltages (V_{ILCD} and V_{IHCD}) are shown along with the normal signaling voltages as below. After contention has been detected, the protocol shall take proper measures to resolve the situation.

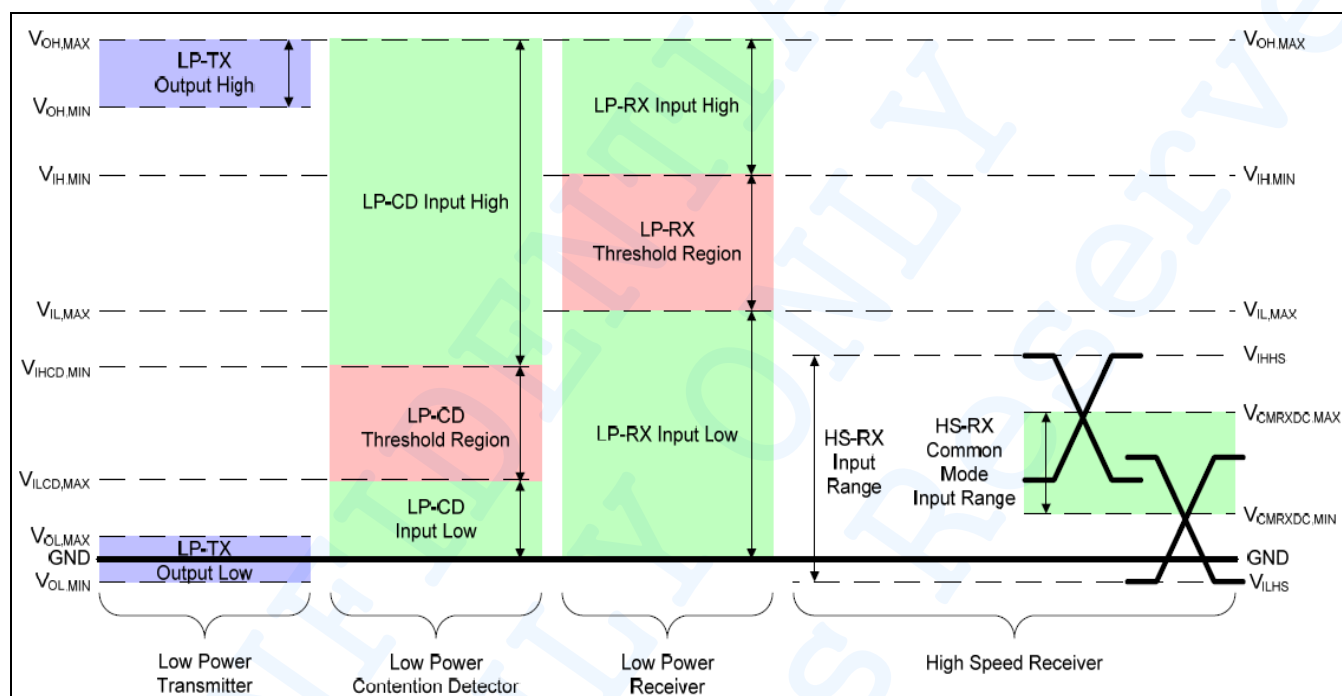


Figure 7 Signaling and Contention Voltage Levels

Table 18 MIPI Contention Detector (LP-CD) DC Characteristic

Item		Symbol	Min.	Typ.	Max.	Unit	Note
CD_RX	Logic0 contention threshold	V_{ILCD}	—	—	200	mV	
	Logic1 contention threshold	V_{IHCD}	450	—	—		

2.4.3 MIPI DSI High-Speed RX Clock and Data-Clock Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in following figure. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

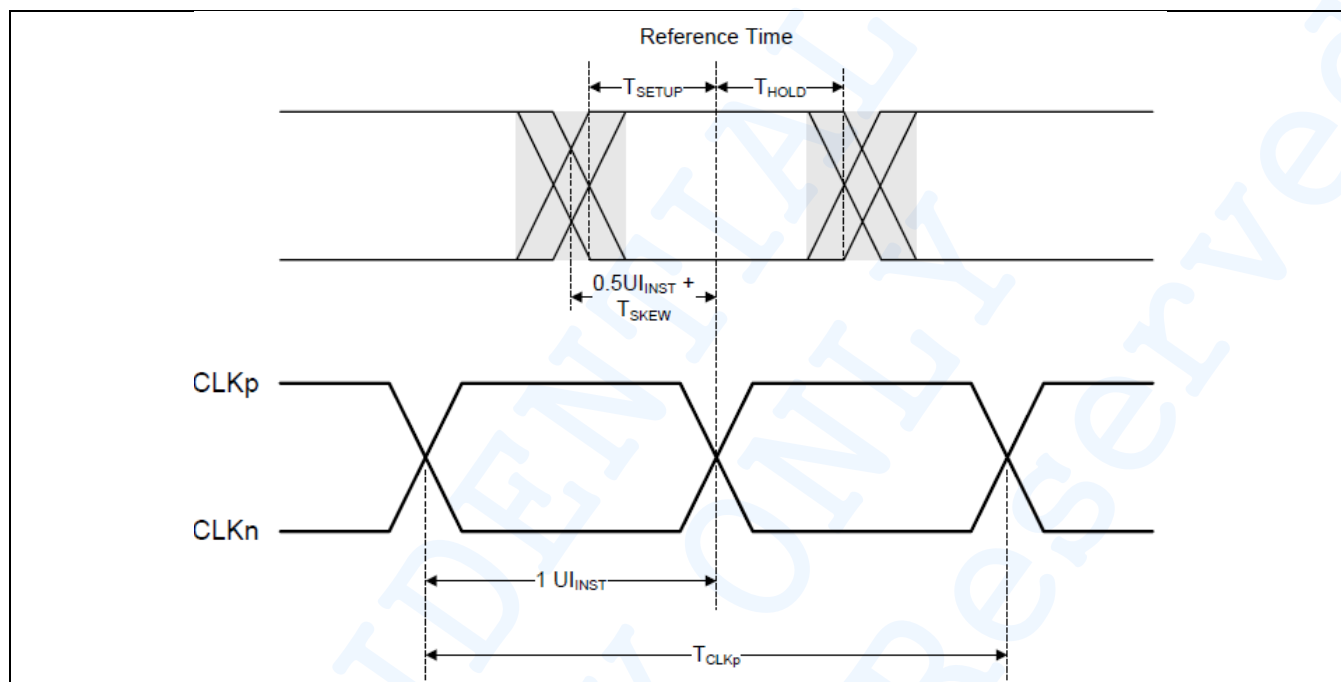


Figure 8 Data to Clock Timing Definitions

Table 19 Data to Clock Signal Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
DSI Data Transfer Rate	T_{DSIR}		80		250	Mbps	
Data to Clock Skew	$T_{SKEW[TX]}$		-0.15		0.15	UI_{INST}	3
Data to Clock Setup time	T_{SETUP}		0.15	—	—	UI_{INST}	1,2
Data to Clock Hold time	T_{HOLD}		0.15	—	—	UI_{INST}	1,2,4
UI instantaneous	UI_{INST}		4	—	12.5	ns	

NOTE:

1. Min. $T_{SETUP[RX]}/T_{HOLD[RX]}$ time is 0.15UI. (May change depends on DSI transfer rate)
2. $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$ are measured without HS-TX jitter and FPC circuit.
3. Total silicon and package delay budget of $0.3 \cdot UI_{INST}$.
4. Total setup and hold window for receiver of $0.3 \cdot UI_{INST}$.

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2.4.4 High Speed Clock and Data Timing

Below Figure shows the sequence of the high speed data transmission.

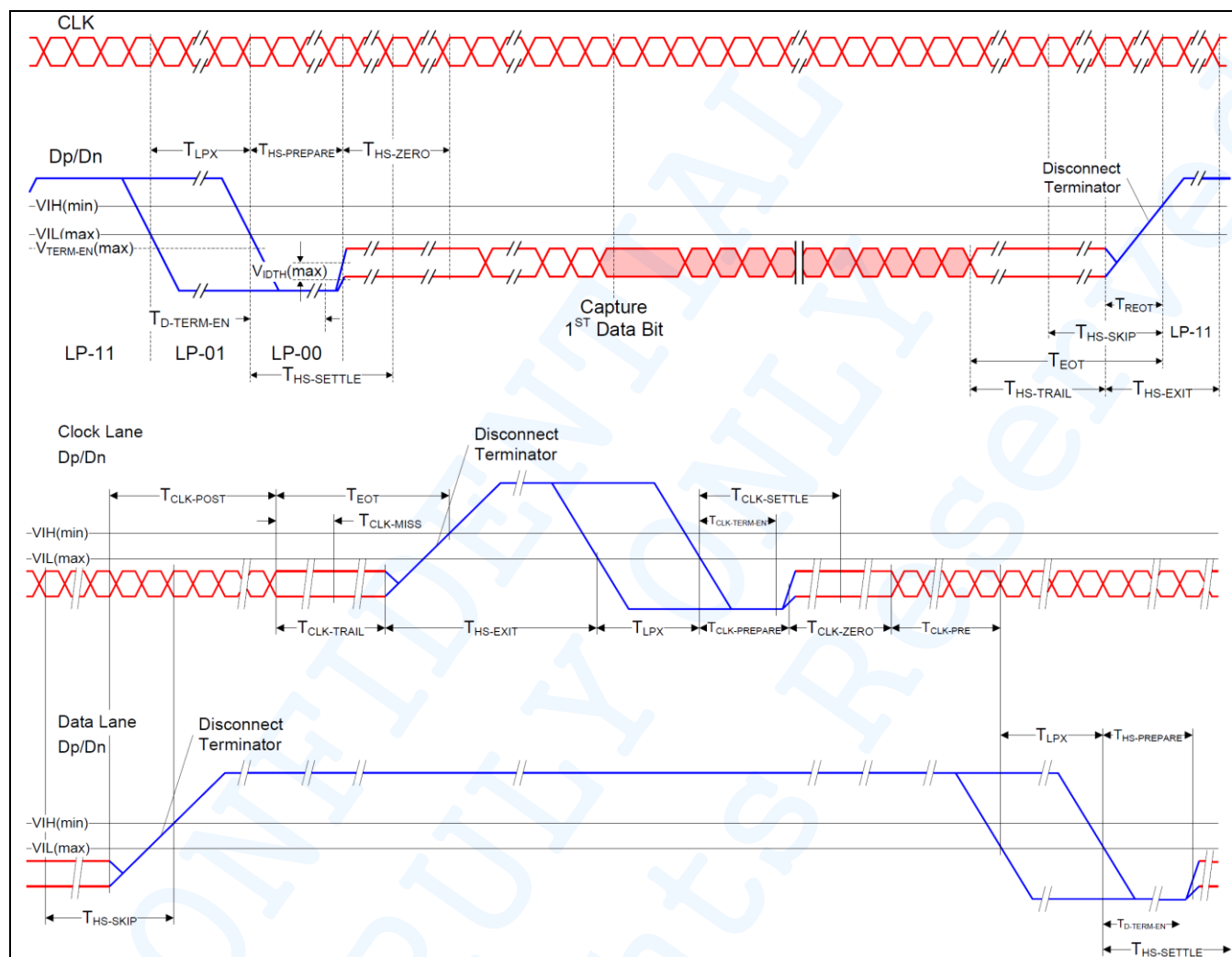


Figure 9 High Speed Clock and Data timing

The values in the following table require a clock tolerance no worse than $\pm 10\%$ for implementation.

Table 20 Global Operation Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-Rx.	—	—	60	ns	(1) (6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52 × UI	—	—		(5)

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Symbol	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	–	–	UI	
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	–	95	ns	
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95	–	300		(6)
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	–	38		
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	–	–		(5)
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	–	–		
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	–	35 ns + $4 \times UI$	–	(6)
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.	–	–	105 ns + $n \times 12 \times UI$	–	(3) (5)
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	–	–	ns	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + $4 \times UI$	–	85 ns + $6 \times UI$		(5)
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + $10 \times UI$	–	–		
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$.	85 ns + $6 \times UI$	–	145 ns + $10 \times UI$		(6)
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	–	55 ns + $4 \times UI$		
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max ($n \times 8 \times UI$, 60 ns + $n \times 4 \times UI$)	–	–		(2) (3) (5)

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Symbol	Description	Min.	Typ.	Max.	Unit	Note
T _{L_{LPX}}	Transmitted length of any Low-Power state period	45.5	–	–	ns	(4) (5)
Ratio T _{L_{LPX}}	Ratio of T _{L_{LPX}} (MASTER)/ T _{L_{LPX}} (SLAVE) between Master and Slave side	2/3	–	3/2	–	
T _{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5 × T _{L_{LPX}}			ns	(5)
T _{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4 × T _{L_{LPX}}				
T _{TA-SURE}	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T _{L_{LPX}}	–	2 × T _{L_{LPX}}		
T _{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	(5)

NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If $a > b$ then $\text{Max.}(a, b) = a$, otherwise $\text{Max.}(a, b) = b$
3. Where $n = 1$ for Forward-direction HS mode and $n = 4$ for Reverse-direction HS mode
4. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

3 Functional Description

3.1 Tearing Effect Information

The Tearing Effect output line supplies a Panel synchronization signal to the external AP. This signal can be enabled or disabled by the TE control commands.

3.1.1 Tearing Effect Control

TE signal is controlled by TEM (35h) and TESCAN (44h) commands. In TE Mode 1 (TEON and TEM=0), the Tearing Effect output signal is generated by V-Sync information or by the only one H-Sync information designated by TESCAN. In TE Mode 2 (TEON and TEM=1), the Tearing Effect output signal consists of V-Sync & H-Sync information.

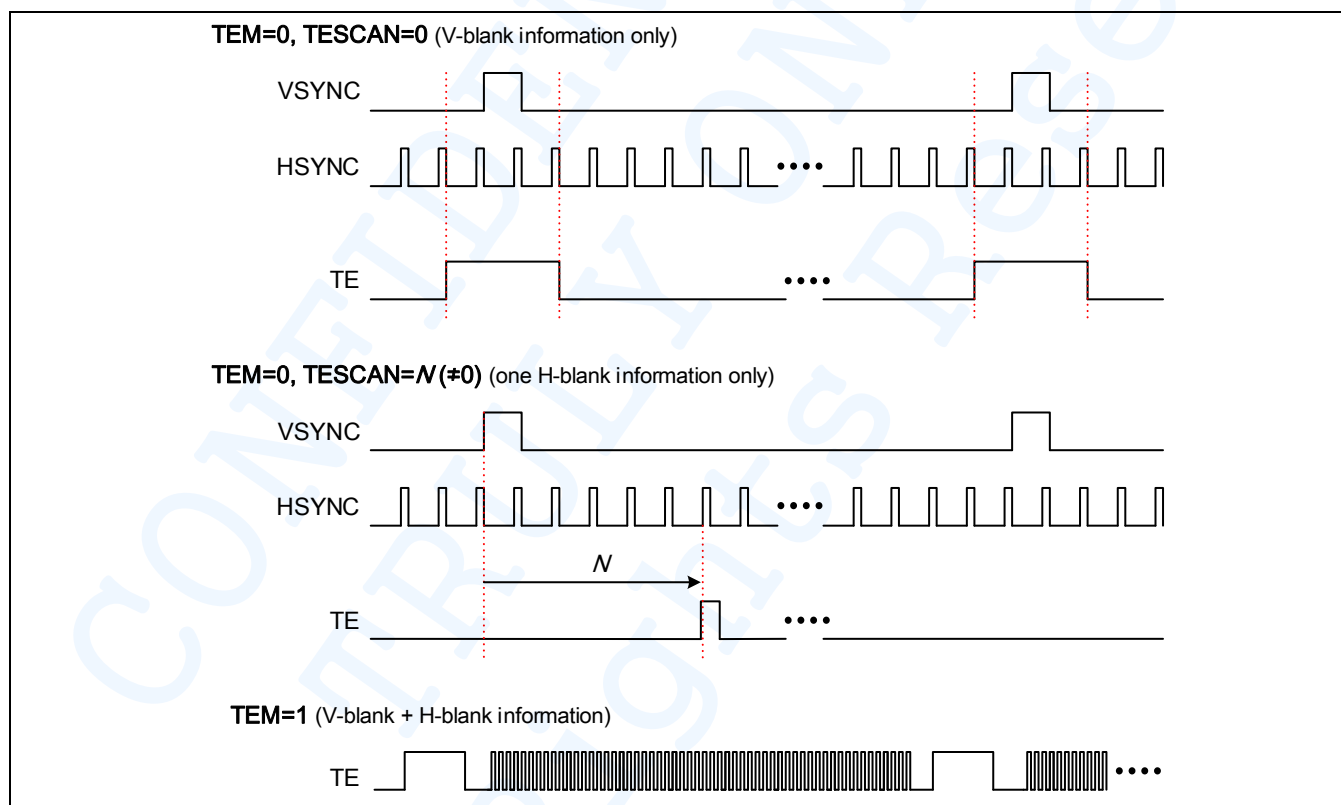


Figure 10 Tearing Effect Line Modes

NOTE: During sleep in mode, the Tearing Effect output pin is active low.

3.1.2 Tearing Effect Line Timings

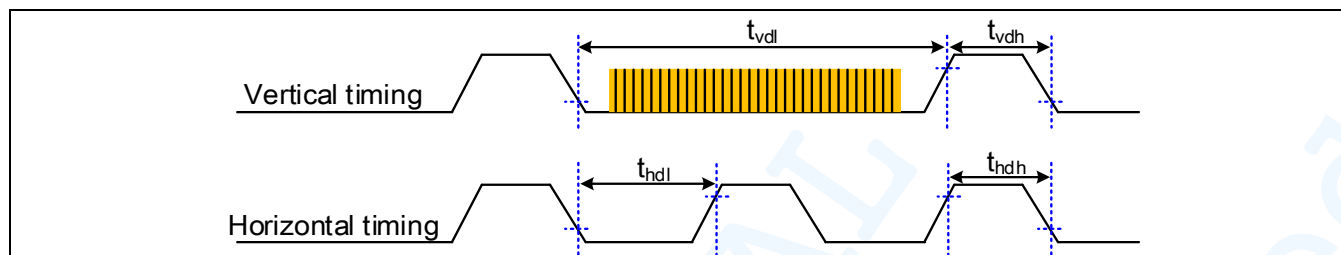


Figure 11 Tearing Effect Line Timings

Table 21 AC Characteristics of Tearing Effect Signal

Parameter	Symbol	Specification			Unit	Description
		Min.	Typ.	Max.		
Vertical timing low duration	tvdl	–	240	–	Line	Note2
Vertical timing high duration	tvdh	–	16	–	Line	Note2
Horizontal timing low duration	thdl	–	240	–	Pixel	Note2
Horizontal timing high duration	thdh	–	32	–	Pixel	Note2
Rise time	tr	–	–	15	ns	Note1
Fall time	tf	–	–	15	ns	

NOTE:

1. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15 ns.
2. Condition: Resolution 240x240, HACTIVE = 240 pixels, HBP = 16 pixels, HFP = 16 pixels, VACTIVE = 240 lines, VBP = 8lines, VFP = 8lines.

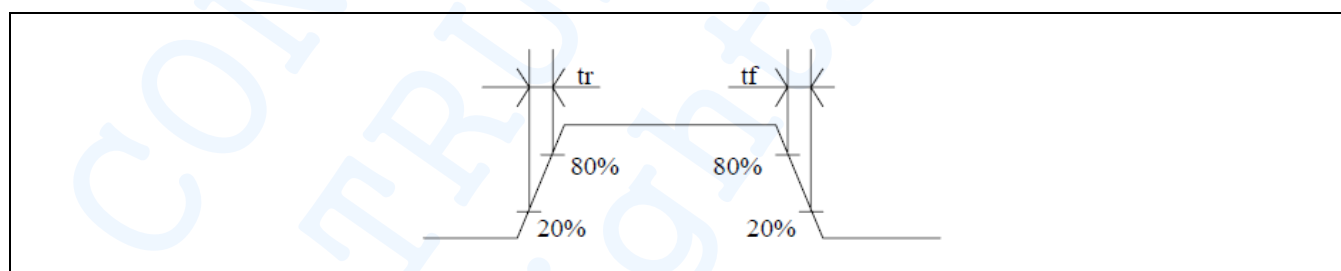


Figure 12 Rise and Fall Times

3.2 Sleep Out Command and Self-Diagnostic Functions

3.2.1 Register Loading Detection

Sleep out command is a trigger for an internal function of the display module which indicates, if the display module loading function of factory default values from OTP to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller (1st step: Compares register and OTP) values, 2nd step: Loads OTP value to register. If those both values (OTP and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0FH)" (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following.

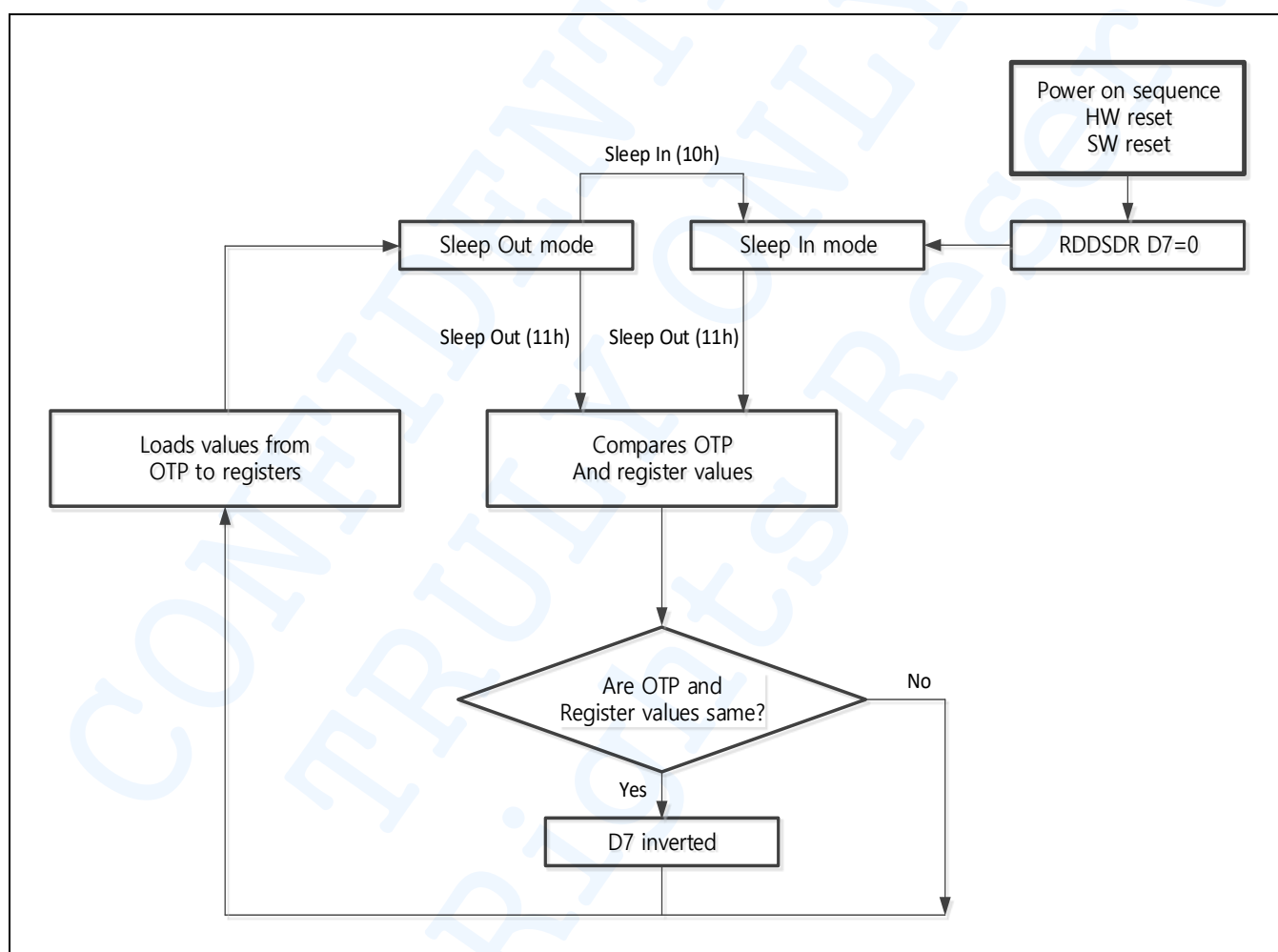


Figure 13 Flow Chart of Register Loading Detection

3.2.2 Functionality Detection

Sleep out command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (=the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. Step up circuit voltage levels, timings, etc.). If functionality requirement is met, there is inverted (=Increased by 1) a bit, which defined in command "Read Display Self-Diagnostic Result (0FH)" (= RDDSDR) (the used bit of this command is D6). If functionality requirement is not met, this bit (D6) is not inverted (= Not increased by 1)

The flow chart for this internal function is following:

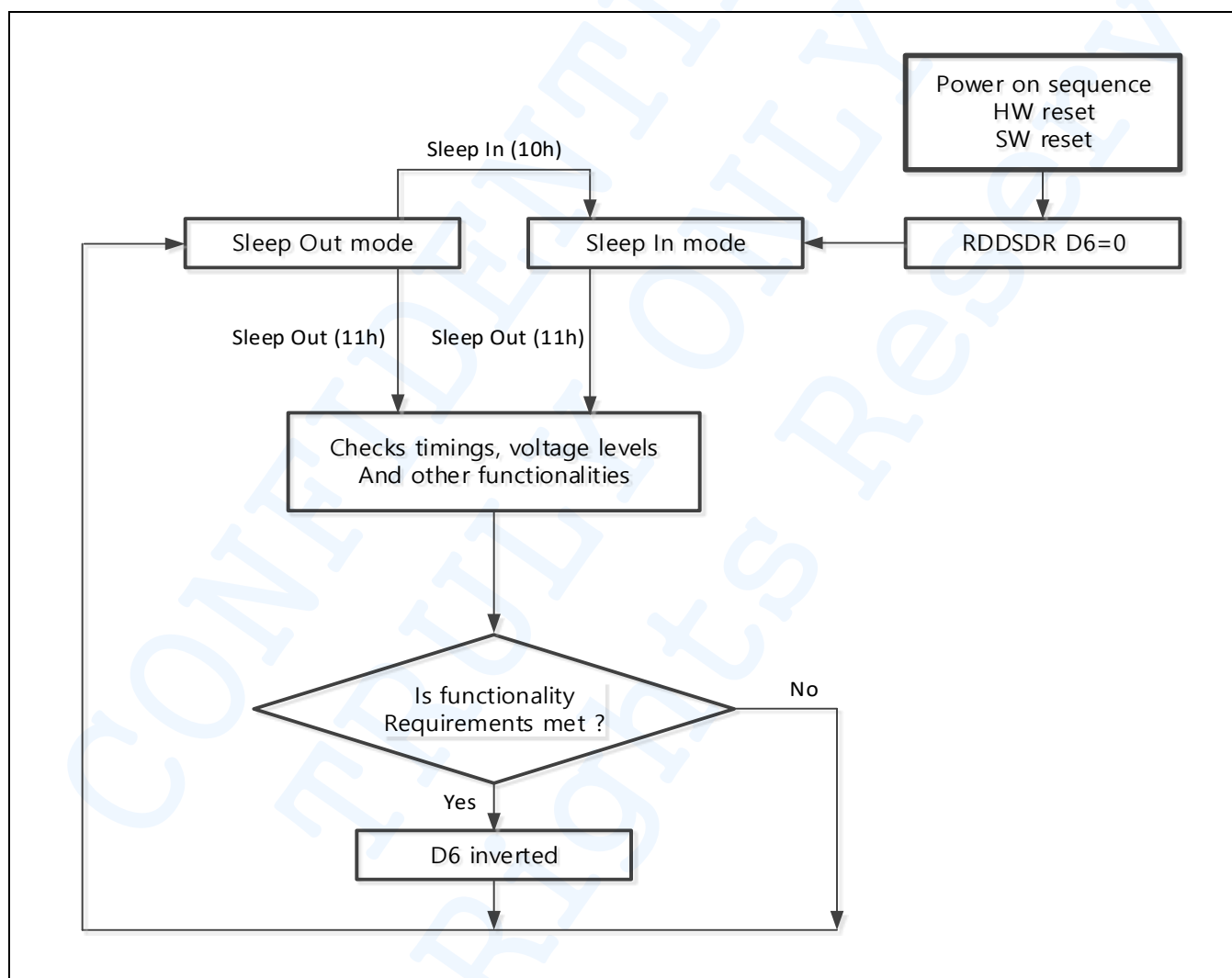


Figure 14 Flow Chart of Functionality Detection

NOTE: There is needed 60ms after sleep out command, when there is changing from Sleep in mode to sleep out mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise there is 10ms delay for D6's value when Sleep out command is sent in Sleep out mode.

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3.3 Power

3.3.1 Power On/Off Sequence

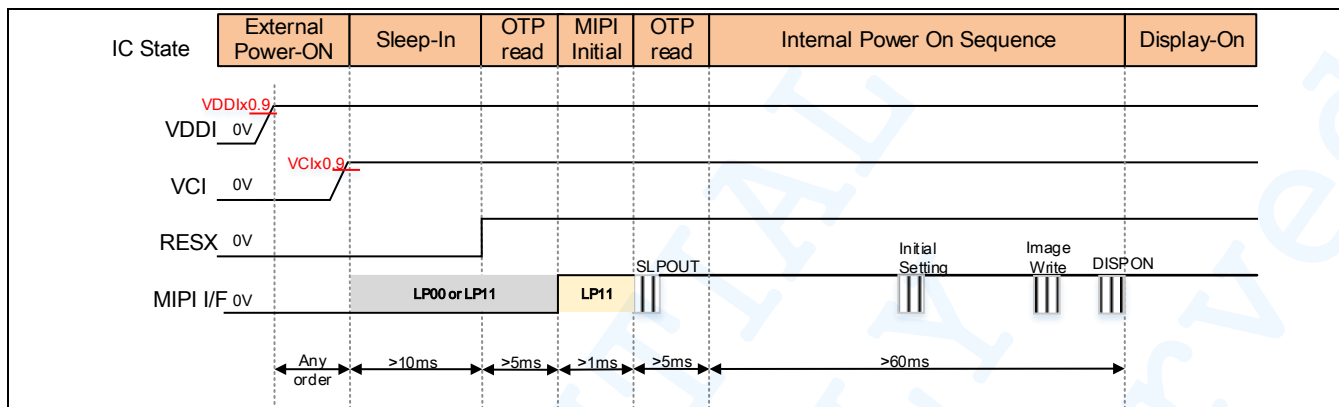


Figure 15 Power-On Sequence

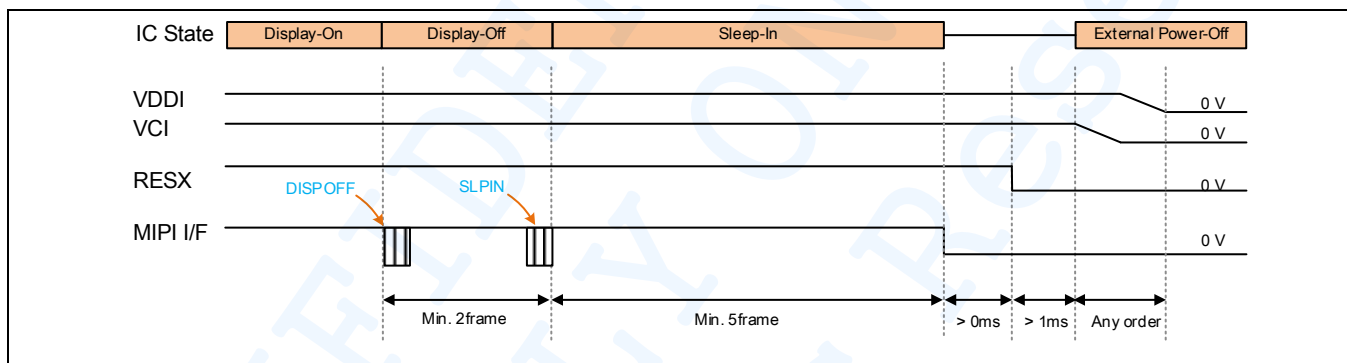


Figure 16 Power-Off Sequence

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3.3.1.1 Power On to Display On / Display Off to Power Off Sequence

The power on to display-on sequence & display-off to power-off sequence are illustrated in the following figures.

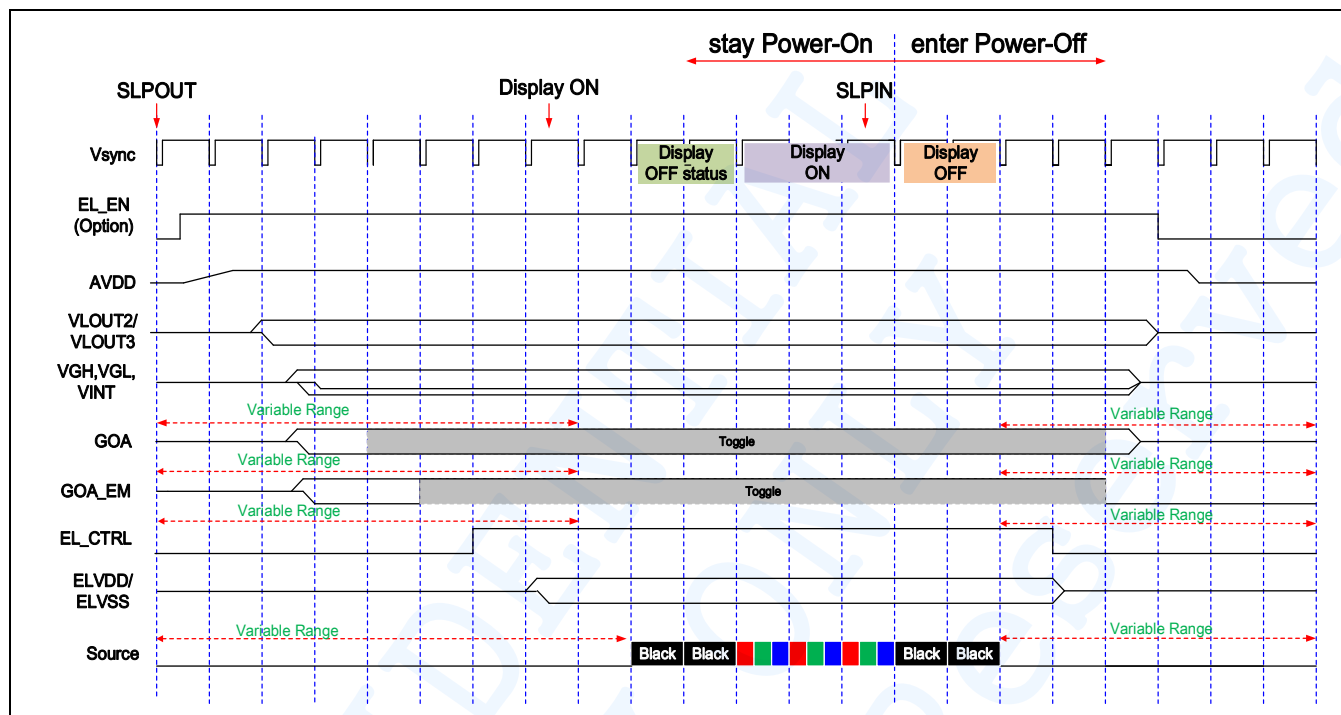


Figure 17 Power-On to Display-On & Display-Off to Power-Off Sequence

3.3.1.2 Power Ramp Up/Down

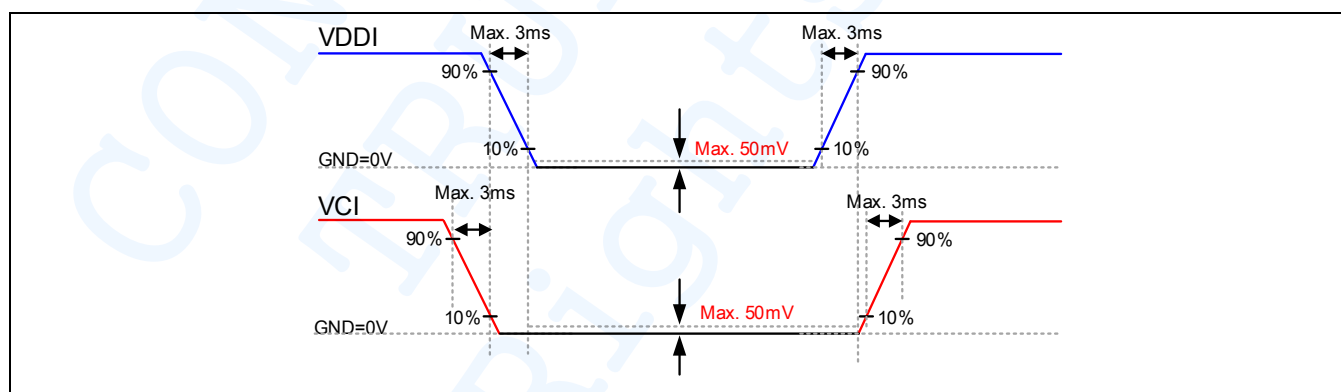


Figure 18 Power Ramp Up/Down

3.3.2 Power Levels

SH8501A supports 4 types of power-consumption modes. Each mode is described as follows:

1. Normal Mode On (full display), Sleep Out.
In this mode, the display is able to show maximum 16,777,216 colors.
2. Sleep In Mode.
In this mode, the booster, internal oscillator and panel driver circuit are stopped.
3. DSTB Mode.
In this mode, the booster, internal oscillator and panel driver circuit are stopped.
Interface and registers are not working.
4. Power off Mode.
In this mode, VCI and VDDI are removed.

NOTE:

1. Transitions between modes 1-2 are controllable by register control.
2. Mode 3 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by Hardware reset only(RESX=Low)
3. Mode 4 is entered only when both Power supplies are removed.

3.3.3 Discharge Status of Power Block and I/O PADs

Table 22 Discharge Status of Power Block and I/O PADs

Power	After H/W or S/W Reset Sleep In Mode	Deep Standby Mode	Abrupt Power Off
VDD	VDD	GND	GND
AVDD	GND	GND	GND
VCL	GND	GND	GND
VLOUT2	GND	GND	GND
VLOUT3	GND	GND	GND
VGH	GND	GND	GND
VGL	GND	GND	GND
VREGOUT	GND	GND	GND
VGS	GND	GND	GND
VREF	GND	GND	GND
VINT	GND	GND	GND
VREFP	GND	GND	GND
SOURCE	Floating	Floating	Floating
GOA	GND	Floating	User defined NOTE

NOTE:

1. Refer to "GOACKL_CTL(B5h)" Description
2. When IC enters to Deep standby mode & Abrupt power off, please set MIPI Pin(=D0P/N & D1P/N & CKP/N) state to GND.

3.3.4 Deep Standby Flow

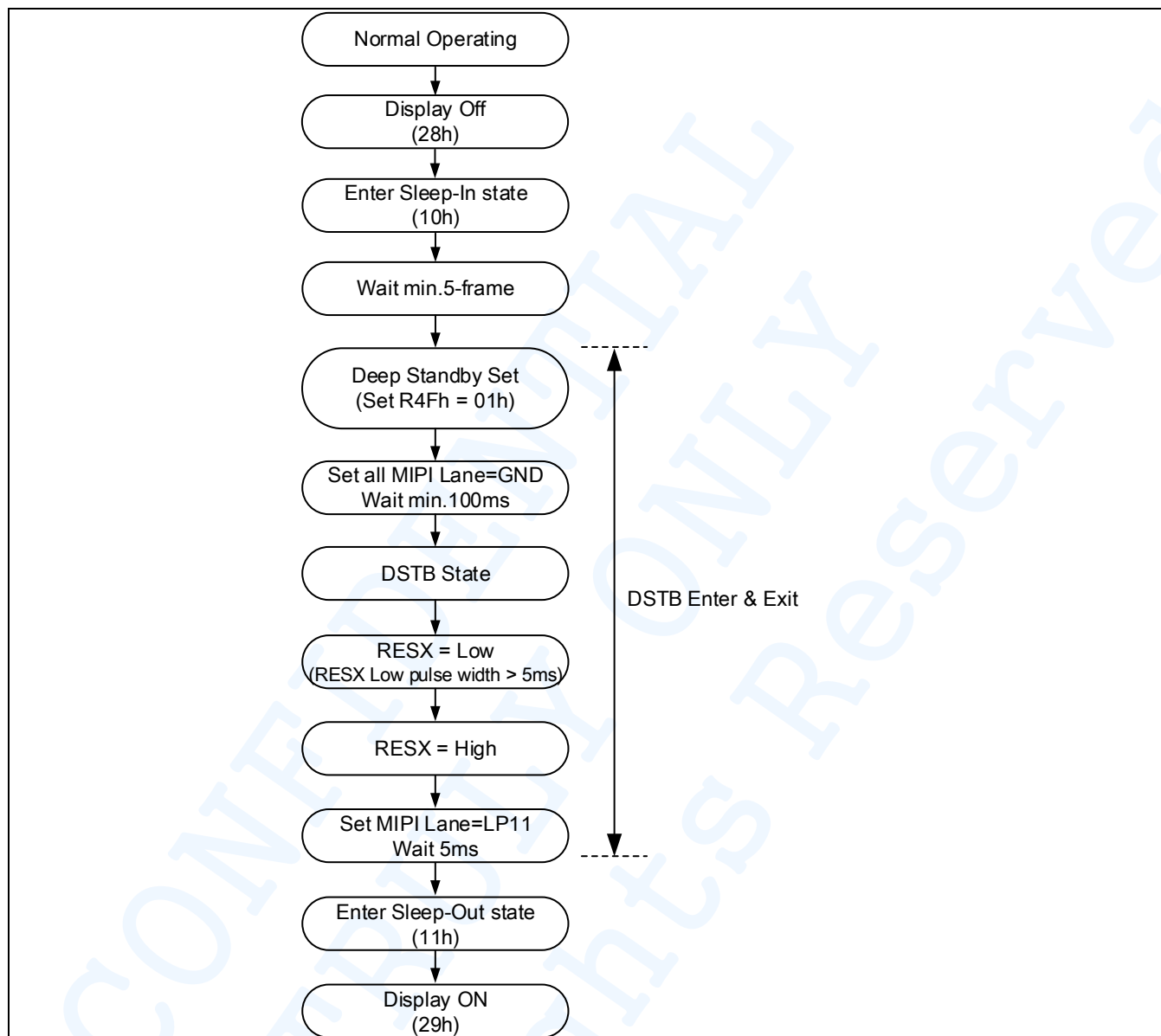


Figure 19 Flow Chart of Deep Standby Mode

NOTE: For MIPI IF, If DSTB mode is used, please set CKP/N, D0P/N, D1P/N state to GND after executing DSTB command.

3.3.5 Sleep In/Out Flow

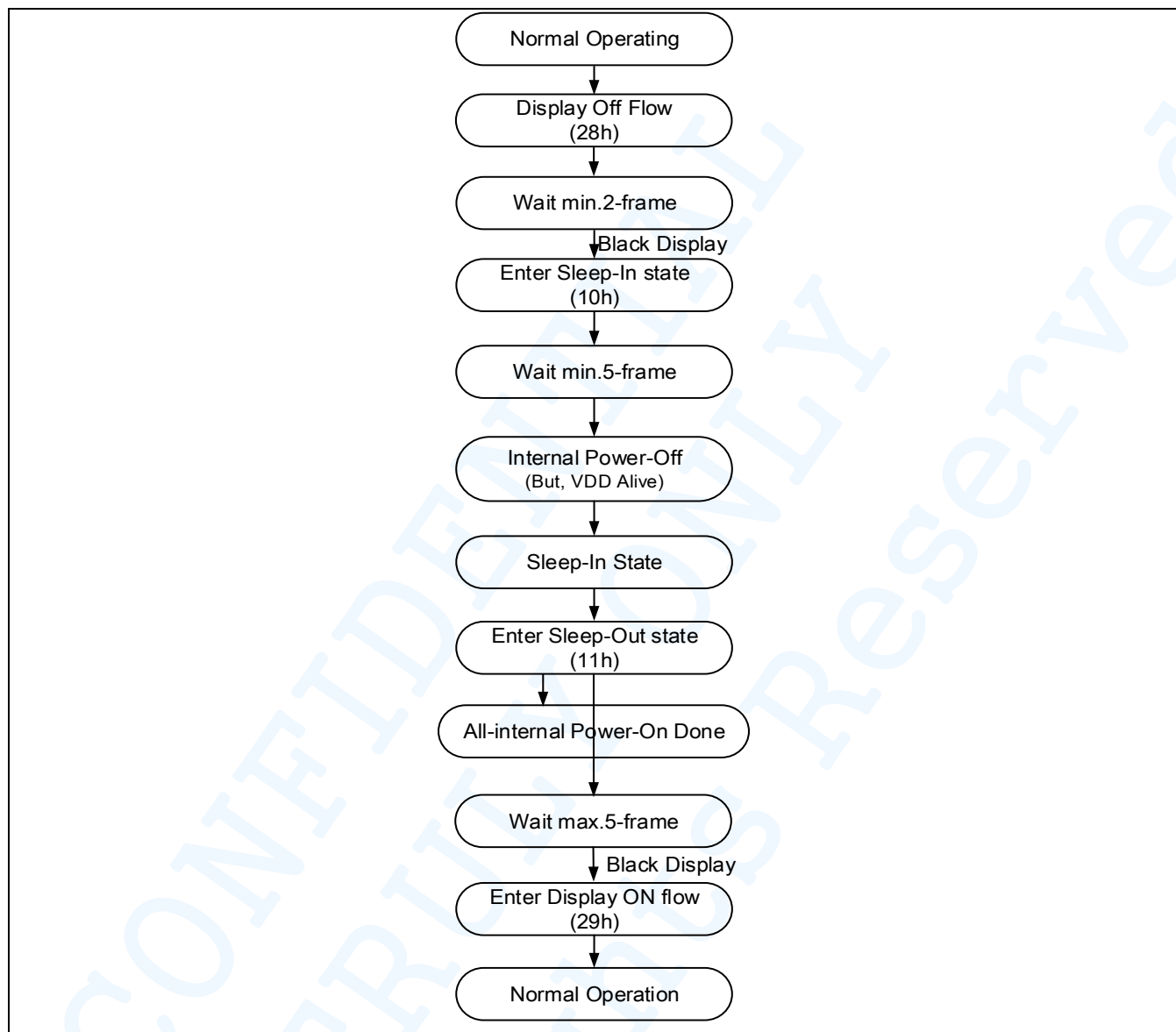


Figure 20 Flow chart of Sleep-In & Sleep-Out Mode

3.4 Operation Sequence

3.4.1 Display Operating Sequence

The below chart is one of the reference for display operation.

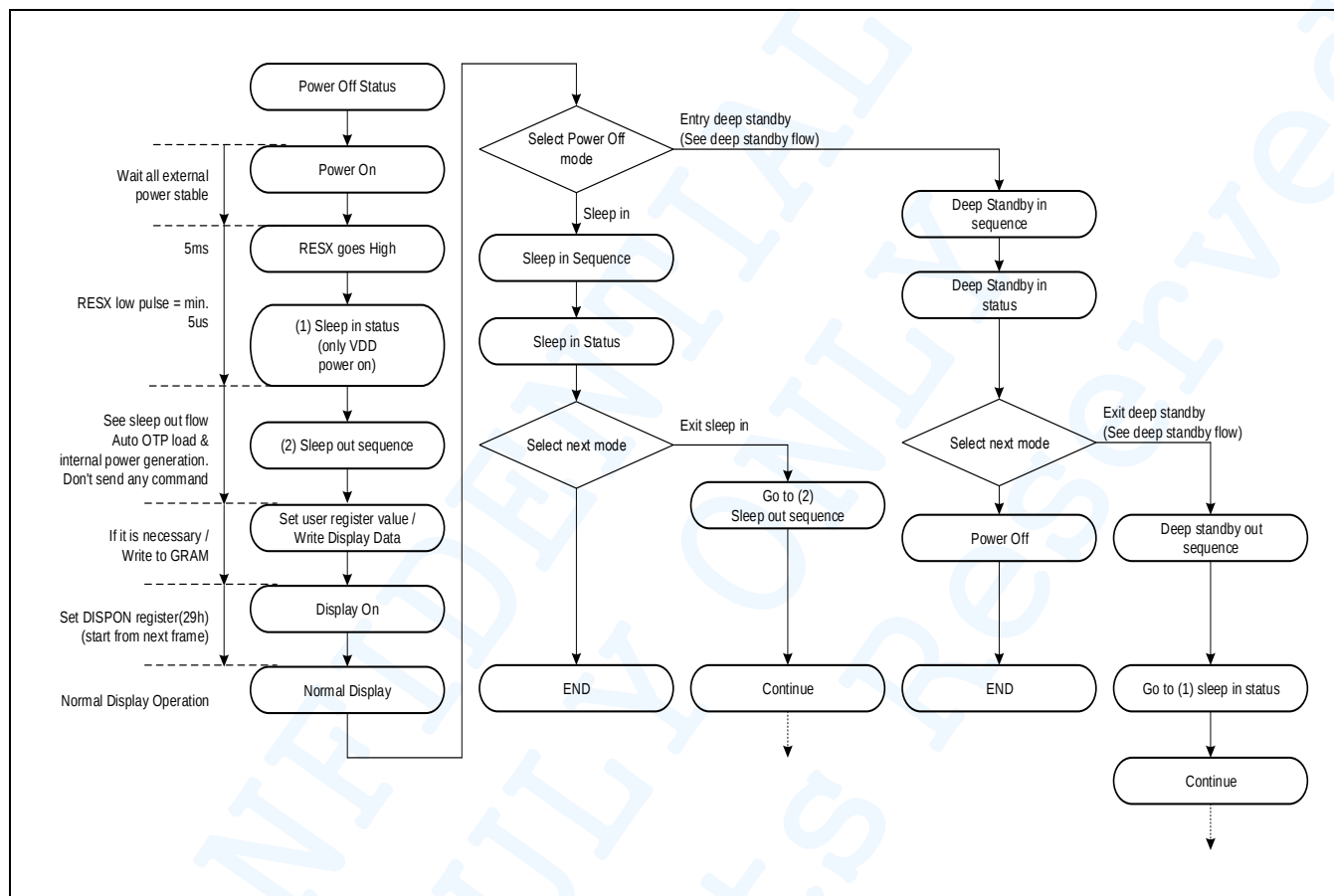


Figure 21 Flow Chart of Display Operation

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3.5 Reset

3.5.1 Register Value

Table 23 The Default Value of the Register – User Command Set

Item	After Power On	After Hardware Reset	After Software Reset
SWRESET(01h)	Off	Off	Off
RDDIDIF(04h)	OTP value	OTP value	OTP value
RDDNUMED(05h)	00h	00h	00h
RDDPDM(0Ah)	08h	08h	08h
RDDMADCTL(0Bh)	00h	00h	00h
RDDCOLMOD(0Ch)	77h	77h	77h
RDDIM(0Dh)	00h	00h	00h
RDDSM(0Eh)	00h	00h	00h
RDDSDR(0Fh)	00h	00h	00h
SLPIN(10h) / SLPOUT(11h)	SLPIN	SLPIN	SLPIN
PTLON(12h)	Off	Off	Off
NORON(13h)	On	On	On
INVOFF(20h) / INVON(21h)	Off / Off	Off / Off	Off / Off
ALLOFF(22h) / ALLON(23h)	Off / Off	Off / Off	Off / Off
DISPOFF(28h) / DISPON(29h)	Off / Off	Off / Off	Off / Off
CASET(2Ah) : SC/EC	0000h/00EFh	0000h/00EFh	0000h/00EFh
PASET(2Bh) : SP/EP	0000h/013Fh	0000h/013Fh	0000h/013Fh
RAMWR(2Ch)	Contents of memory is set randomly		
PTLAR(30h) : PSR / PER	0000h/013Fh	0000h/013Fh	0000h/013Fh
PTLAC(31h) : PSC / PEC	0000h/00EFh	0000h/00EFh	0000h/00EFh
TEOFF(34h) / TEON(35h)	Off / Off	Off / Off	Off / Off
Tearing Line Mode (35h)	00h	00h	00h
MADCTL (36h)	00h	00h	00h
IDMOFF(38h) / IDMON(39h)	Off / Off	Off / Off	Off / Off
COLMOD(3Ah)	77h	77h	77h
RAMWRC(3Ch)	Contents of memory is set randomly		
TESCAN(44h) / RDSCL(45h)	0000h / 0000h	0000h / 0000h	0000h / 0000h
AODOFF(48h) / AODON(49h)	Off / Off	Off / Off	Off / Off
AOD_WRDISBV(4Ah)	FFh	FFh	FFh
AOD_RDDISBV(4Bh)	FFh	FFh	FFh
Deep Standby Control(4Fh)	Off	Off	Off
WRDISBV(51h)	FFh	FFh	FFh
RDDISBV(52h)	FFh	FFh	FFh
WRCTRLD1(53h)	28h	28h	28h

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Item	After Power On	After Hardware Reset	After Software Reset
RDCTRLD1(54h)	28h	28h	28h
WRCTRLD2(55h)	00h	00h	00h
RDCTRLD2(56h)	00h	00h	00h
WR_CE(58h)	00h	00h	00h
RD_CE(59h)	00h	00h	00h
HBM_WRDISBV(63h)	FFh	FFh	FFh
HBM_RDDISBV(64h)	FFh	FFh	FFh
RDHBMCTRL(65h)	00h	00h	00h
HBMCTRL(66h)	00h	00h	00h
COLSET0(70h)	000000h	000000h	000000h
COLSET1(71h)	0000FFh	0000FFh	0000FFh
COLSET2(72h)	00FF00h	00FF00h	00FF00h
COLSET3(73h)	00FFFFh	00FFFFh	00FFFFh
COLSET4(74h)	FF0000h	FF0000h	FF0000h
COLSET5(75h)	FF00FFh	FF00FFh	FF00FFh
COLSET6(76h)	FFFF00h	FFFF00h	FFFF00h
COLSET7(77h)	FFFFFFh	FFFFFFh	FFFFFFh
COLSET8(78h)	000000h	000000h	000000h
COLSET9(79h)	0000FFh	0000FFh	0000FFh
COLSET10(7Ah)	00FF00h	00FF00h	00FF00h
COLSET11(7Bh)	00FFFFh	00FFFFh	00FFFFh
COLSET12(7Ch)	FF0000h	FF0000h	FF0000h
COLSET13(7Dh)	FF00FFh	FF00FFh	FF00FFh
COLSET14(7Eh)	FFFF00h	FFFF00h	FFFF00h
COLSET15(7Fh)	FFFFFFh	FFFFFFh	FFFFFFh
COLOPT(80h)	07h	07h	07h
RDDDBS(A1h)	(OTP values)	(OTP values)	(OTP values)
RDDDBC(A8h)	(OTP values)	(OTP values)	(OTP values)
RDFCS(AAh)	00h	00h	00h
RDCCS(AFh)	00h	00h	00h
SPI_MODE(C4h)	00h	00h	00h
RDID1(DAh)	(OTP values)	(OTP values)	(OTP values)
RDID2(DBh)	(OTP values)	(OTP values)	(OTP values)
RDID3(DCh)	(OTP values)	(OTP values)	(OTP values)

NOTE: There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Internal PoR (Power-on Reset) circuit generates a reset signal within 1ms after VDDI and VCI rise up to 90% of their typical value. It is necessary to wait 5msec after Power-on reset before sending commands. this is to allow time for OTP loading.

3.6 Modules Input/output/Bi-direction (I/O) PADS

3.6.1 Output or Bi-directional (I/O) PADS

Table 24 Reset States of Output and Bi-direction PADS

Output or Bi-directional PADS	When RESX is Low	After Power On	After Hardware Reset	After Software Reset
D0P	High-Z	High-Z	High-Z	High-Z
D0N	High-Z	High-Z	High-Z	High-Z
D1P	High-Z	High-Z	High-Z	High-Z
D1N	High-Z	High-Z	High-Z	High-Z
SDI_RDx	High-Z	High-Z	High-Z	High-Z
SDO	Low	Low	Low	Low
DB0_SDI2	Low	Low	Low	Low
DB1_SDI3	Low	Low	Low	Low
DB[7:2]	Low	Low	Low	Low
ERR_FG	Low	Low	Low	Low
EL_EN	Low	Low	Low	Low
EL_CTRL	Low	Low	Low	Low
TE	Low	Low	Low	Low
TEST_OUT1/2	Low	Low	Low	Low

NOTE: There will be no output from TE during power on/off sequence, hardware reset and software reset

3.6.2 Input PADS

Table 25 Reset States of Input PADS

Input PADS	When RESX is Low	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	–	See Section	Input valid	Input valid	Input valid	See Section
CKP	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
CKN	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
CSX	High	High	High	High	High	High
DCX	High	High	High	High	High	High
SCL_WRX	High	High	High	High	High	High

4 Interface

Terminology used in this section

- Mobile Industry Processor Interface(MIPI): MIPI Alliance has defined DBI, DSI, and D-PHY
- Display Bus Interface(DBI): Type-B 8-bit / Type-C Option1 SPI3W/ Option3 SPI4W
- Dual mode in SPI3W and SPI4W (register option)
- Quad SPI: Quad serial interface
- DSI: Display serial interface. DSI is usually called as MIPI
- D-PHY: Physical layer

4.1 Interface Type Selection

Interface type is decided by input IM[2:0].

Table 26 Interface Type Selection

IM[2:0]	Command Interface	Display Data Interface
000	SPI 3-wire / MIPI	SPI 3-wire / MIPI
001	SPI 4-wire / MIPI	SPI 4-wire / MIPI
010	Quad SPI / MIPI	Quad SPI / MIPI
011	MPU 8-bit	MPU 8-bit

In-Out pad mapping for each interface mode is shown below.

MPU I/E

Table 27 MPU Interface PAD Assignment

PAD name	IO	DBI Type-B (80-series 8bit MPU)		
		Signal Name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low
SCL_WRX	I	WRX	I	Write clock, Rising edge
DCX	I	DCX	I	0:Command, 1:Data
SDI_RDX	IO	RDX	I	Read clock, Falling edge
DB[7:2], DB1_SDI3,DB0_SDI2	IO	DB[7:0]	IO	Bi-direction data bus

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SPI 3-Wire

Table 28 SPI 3-Wire PAD Assignment

PAD name	IO	DBI Type-C – SPI 3-wire			DBI Type-C – SPI 3-wire Dual		
		Signal Name	IO	Description	Signal name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low	CSX	I	Chip selection, Active Low
SCL_WRX	I	SCL	I	SPI clock, Rising edge	SCL	I	SPI clock, Rising edge
SDI_RDX	IO	SDA	IO	Serial Data in-out or	SDIO	IO	Serial Data in 0, Data out
		SDI	I	Serial Data input			
SDO	IO	SDO	O	Serial Data output	SDO	O	Serial Data output
DCX	I	-	-	-	SDI1	I	Serial Data in 1

SPI 4-Wire

Table 29 SPI 4-Wire PAD Assignment

PAD name	IO	DBI Type-C – SPI 4-wire			DBI Type-C – SPI 4-wire Dual		
		Signal Name	IO	Description	Signal name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low	CSX	I	Chip selection, Active Low
SCL_WRX	I	SCL	I	SPI clock, Rising edge	SCL	I	SPI clock, Rising edge
DCX	I	DCX	I	0:Command, 1:Data	DCX	I	0:Command, 1:Data
					SDI1	I	Serial Data in 1
SDI_RDX	IO	SDA	IO	Serial Data in-out or	SDIO	IO	Serial Data in 0, Data out
		SDI	I	Serial Data input			
SDO	IO	SDO	O	Serial Data output	SDO	O	Serial Data output

QUAD SPI

Table 30 Quad SPI PAD Assignment

PAD name	IO	Quad SPI		
		Signal Name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low
SCL_WRX	I	SCL	I	Serial clock, Rising edge
SDI_RDX	IO	SDIO	IO	Serial Data in 0, Data out
DCX	IO	SDI1	I	Serial Data input 1
DB0_SDI2	IO	SDI2	I	Serial Data input 2
DB1_SDI3	IO	SDI3	I	Serial Data input 3

4.2 MIPI DBI Type-B and Type-C Interface Configuration

SH8501A driver IC supports parallel interface DBI Type-B. 8bits data transmitted from Host to SH8501A driver IC. And supports serial interface DBI Type-C (Option1 and Option3). 8/9bits data transmitted from Host to SH8501A driver IC. It is possible to suspend data transfer if the Chip select(CSX) and clock signal (WRX or SCL) are held in their current state until data transfer can resume. Host can read SH8501A register value from DB[7:0] or SDIA (or SDO) output. Also SH8501A can support Quad SPI mode.

4.3 MIPI DBI Interface Data Transfer Ignore and Pause

SH8501A stores the command/parameters into the register file. The command and parameters transferred from Host Application processor (AP) to SH8501A are stored in the register file of SH8501A before transmission break occurred. e.g.) such as CSX to “High” during data transmission. If transmission break is occurred before the last parameter is transmitted, only the last transmitted parameters are stored. If a new command is transferred before the last parameter is done, SH8501A begins to store a new parameter. And previous left parameters are ignored even they are resent. SH8501A does not support data transmission pause operation during Write/Read sequence.

4.4 MIPI DBI Type-B (MPU 8bit) Interface

In MIPI DBI Type-B interface, SH8501A supports 8-bit interface mode. Register write-read timing diagram is shown below. Using this mode, user also can send RGB image data with command 0x2C and 0x3C.

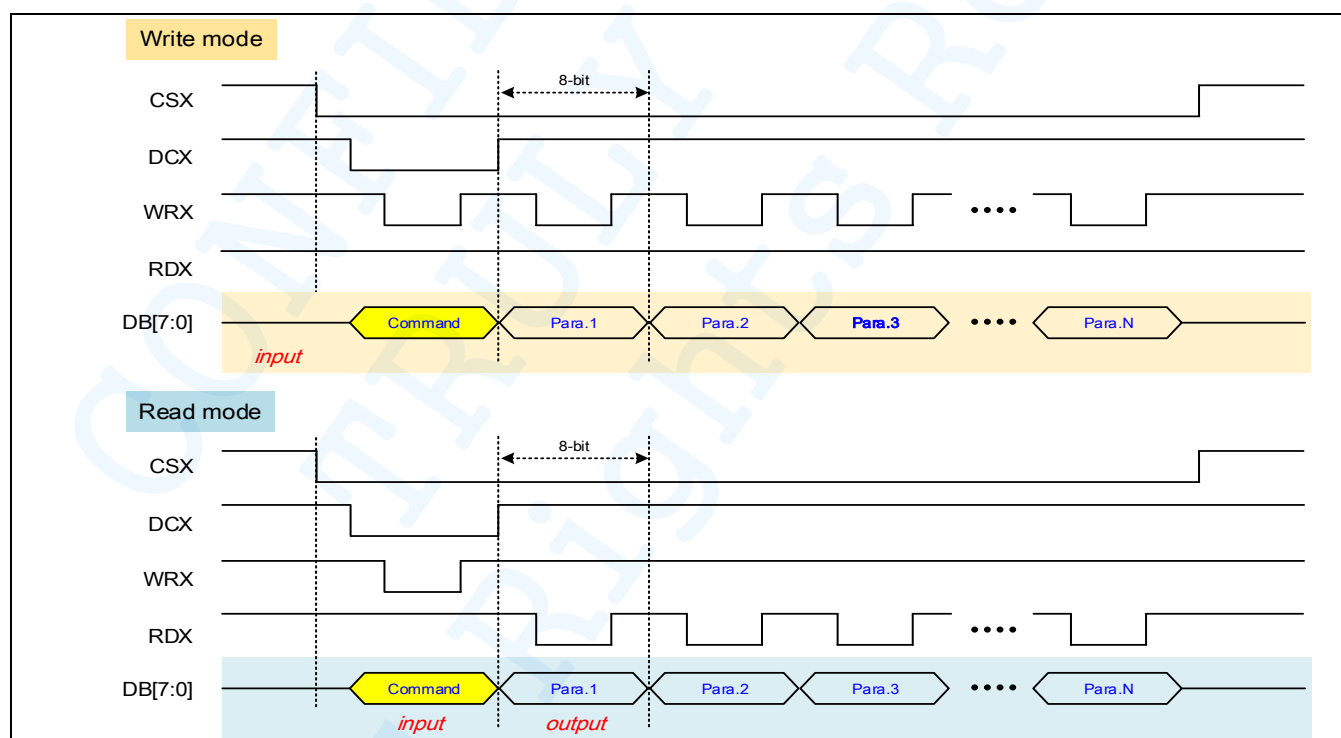


Figure 22 MPU 8-bit Interface Protocol – Register Read and Write

SH8501A

240x240 AMOLED Display Driver IC

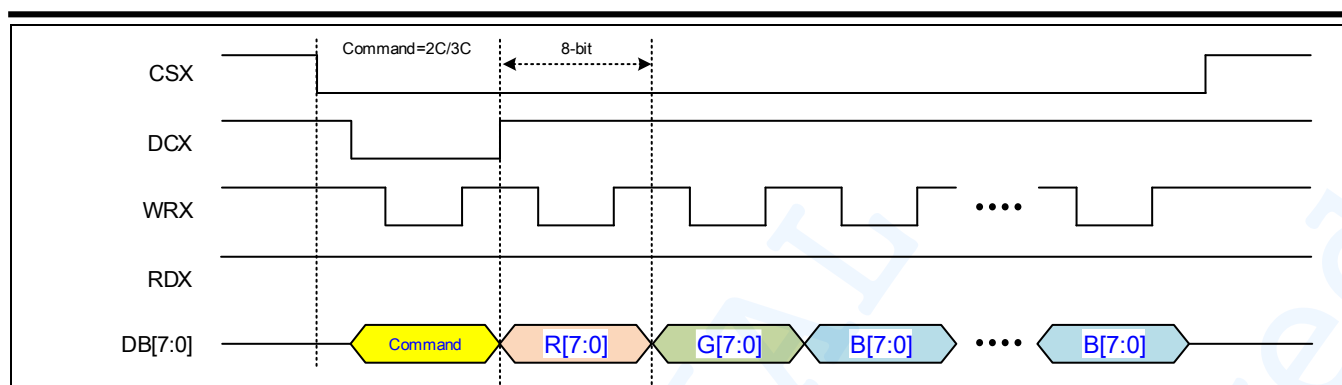


Figure 23 MPU 8-bit Interface – Pixel Interface

4.5 MIPI DBI Type-C (3-Wire 9-Bit) Interface

This serial interface is MIPI DBI Type-C (3-wire 9-bit) bi-directional interface for communication between the Host Application Processor (AP) and the SH8501A. CSX, SCL, SDIO (or SDI, SDO) are used for interface with AP only, so it can be stopped when communication is not necessary. In read protocol, SDIO or SDI+SDO condition is decided by register SDIO_MODE setting in command SPI_MODE(C4h). UCS read is divided into 8 bit para mode and 24 bit para mode. MCS read is the same as the 24 bit para mode of UCS, but SPI READ should be set to '1' with the command SPI_RDON (47h). SPI_READ must be reset to '0' with the command SPI_RDOFF (46h).

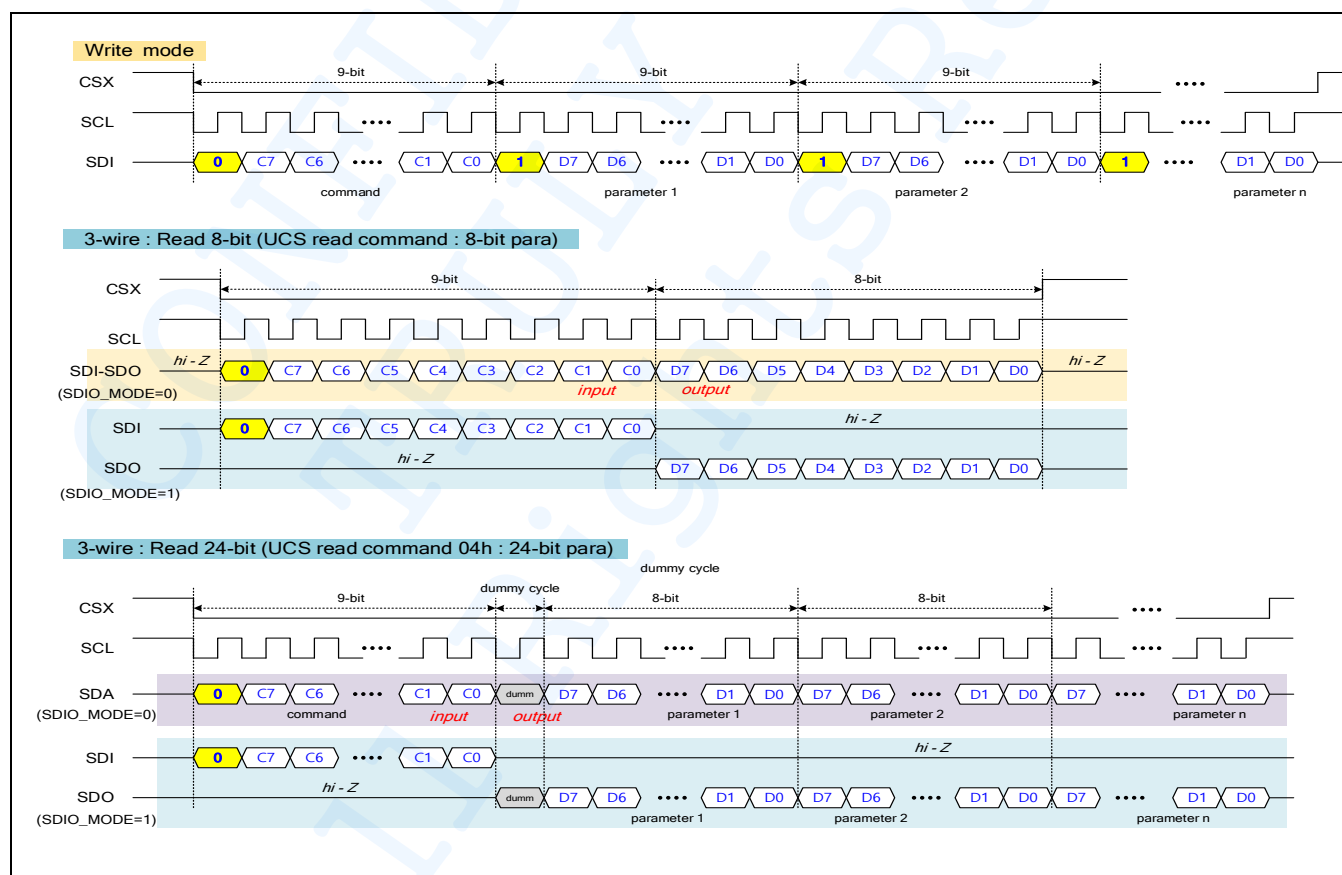


Figure 24 MIPI DBI Type-C Interface – Register Write and Read

4.6 MIPI DBI Type-C (4-Wire 8-Bit) Interface

This serial interface is MIPI DBI Type-C (4-wire 8-bit) bi-directional interface for communication between the Host Application Processor (AP) and the SH8501A. CSX, DCX, SCL, SDIO (or SDI, SDO) are used for interface with AP only, so it can be stopped when communication is not necessary. In read protocol, SDIO or SDI+SDO condition is decided by register SDIO_MODE setting in command SPI_MODE(C4h). UCS read is divided into 8 bit para mode and 24 bit para mode. MCS read is the same as the 24 bit para mode of UCS, but SPI_READ should be set to '1' with the command SPI_RDON (47h). SPI_READ must be reset to '0' with the command SPI_RDOFF (46h).

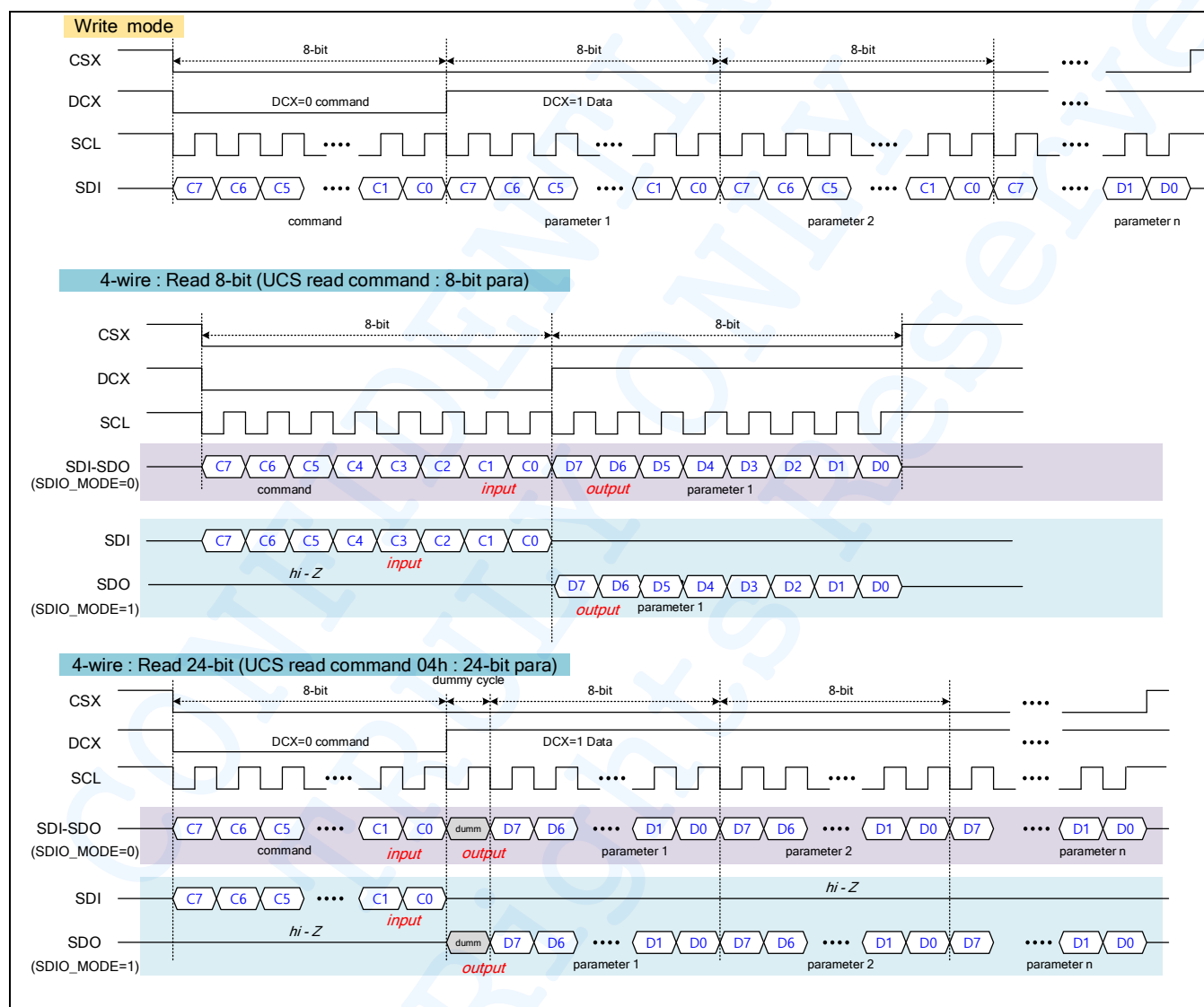


Figure 25 MIPI DBI Type-C (4-Wire 8-Bit) Interface Protocol – Register Write and Read

4.7 SPI Pixel Format

This interface is optional for SPI 3-wire and SPI 4-wire to send RGB image data. All of RGB image transfer formats are explained below. Transfer types 1P/1T 1 line, 1P/1T 2 line, and 2P/3T 2 line are selected by register SPI_MODE(C4h).

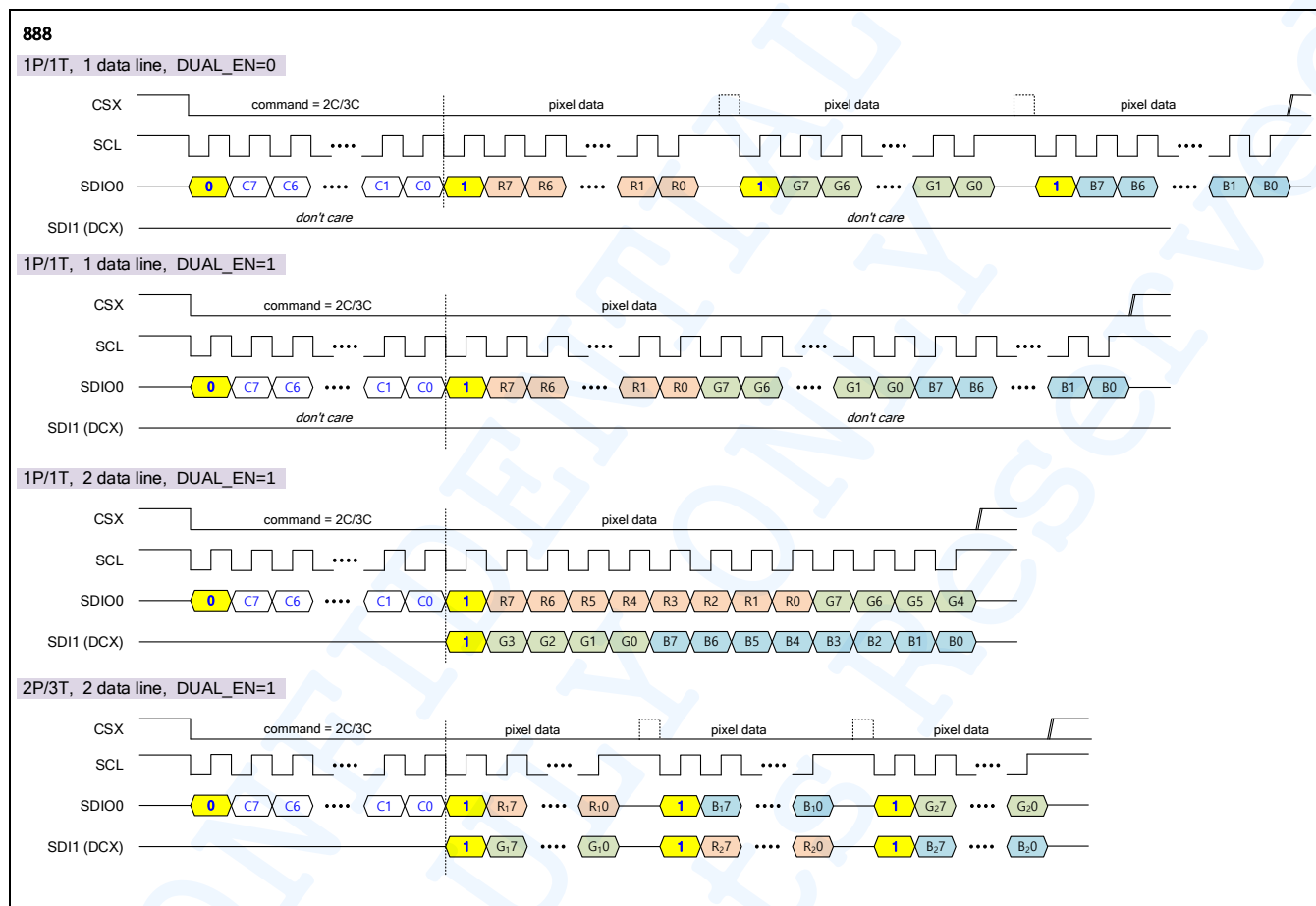


Figure 26 SPI 3-Wire 888 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

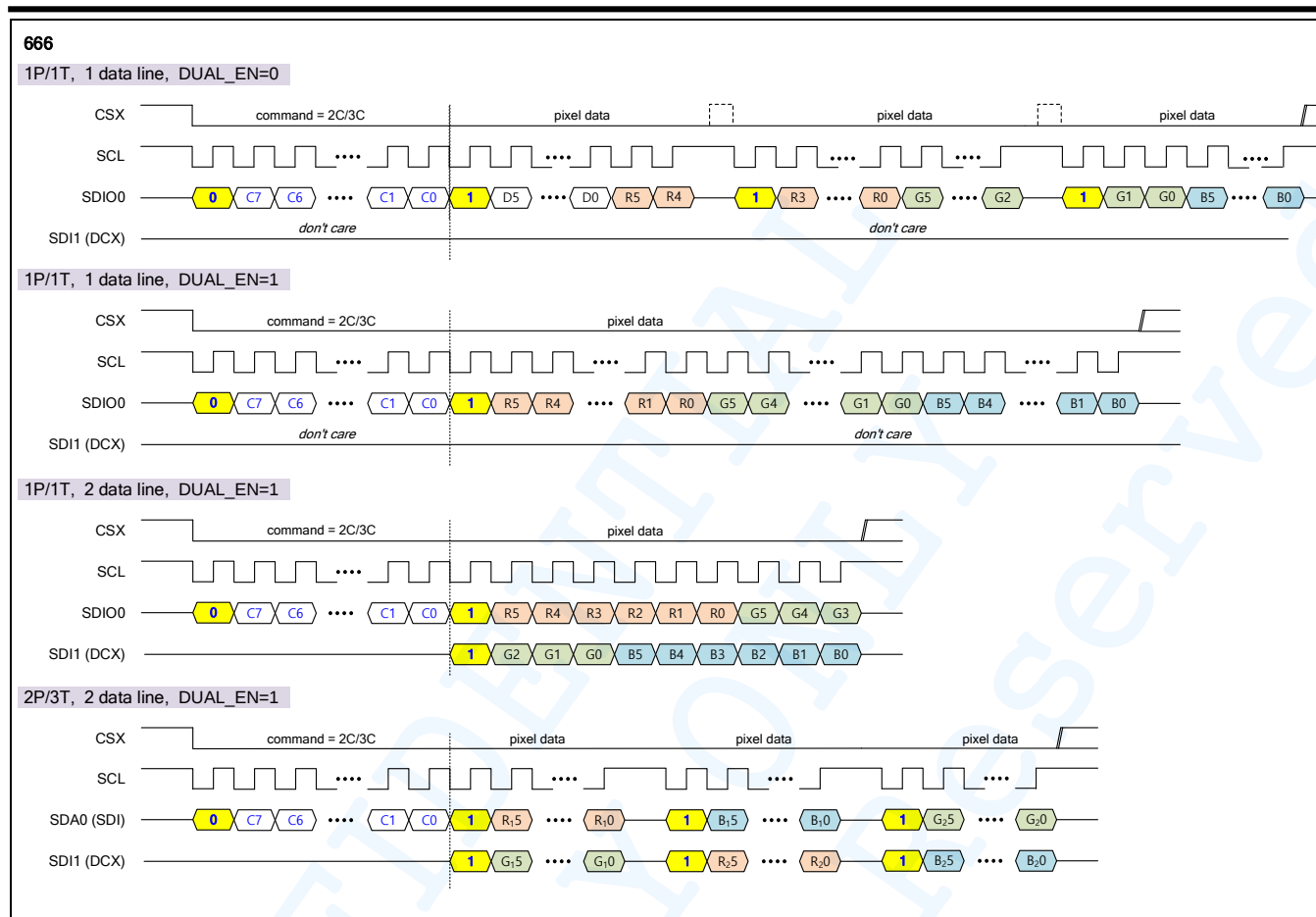


Figure 27 SPI 3-Wire 666 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

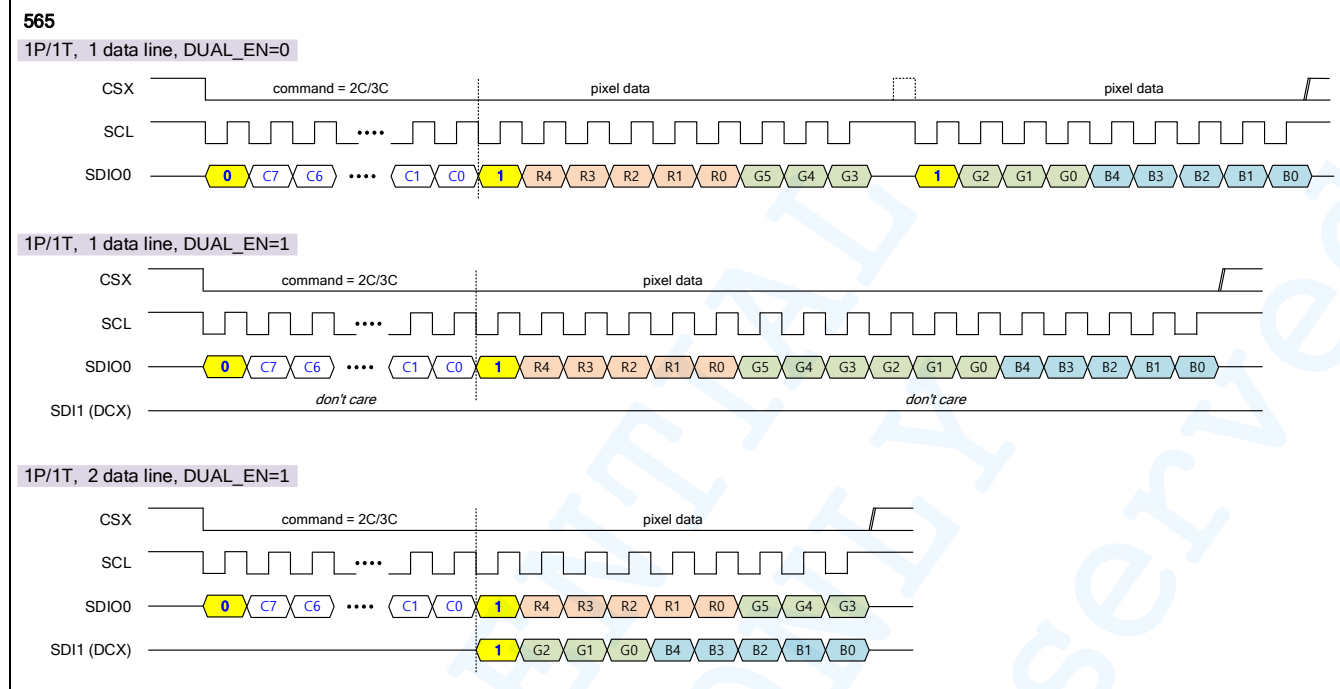


Figure 28 SPI 3-Wire 565 Pixel Format

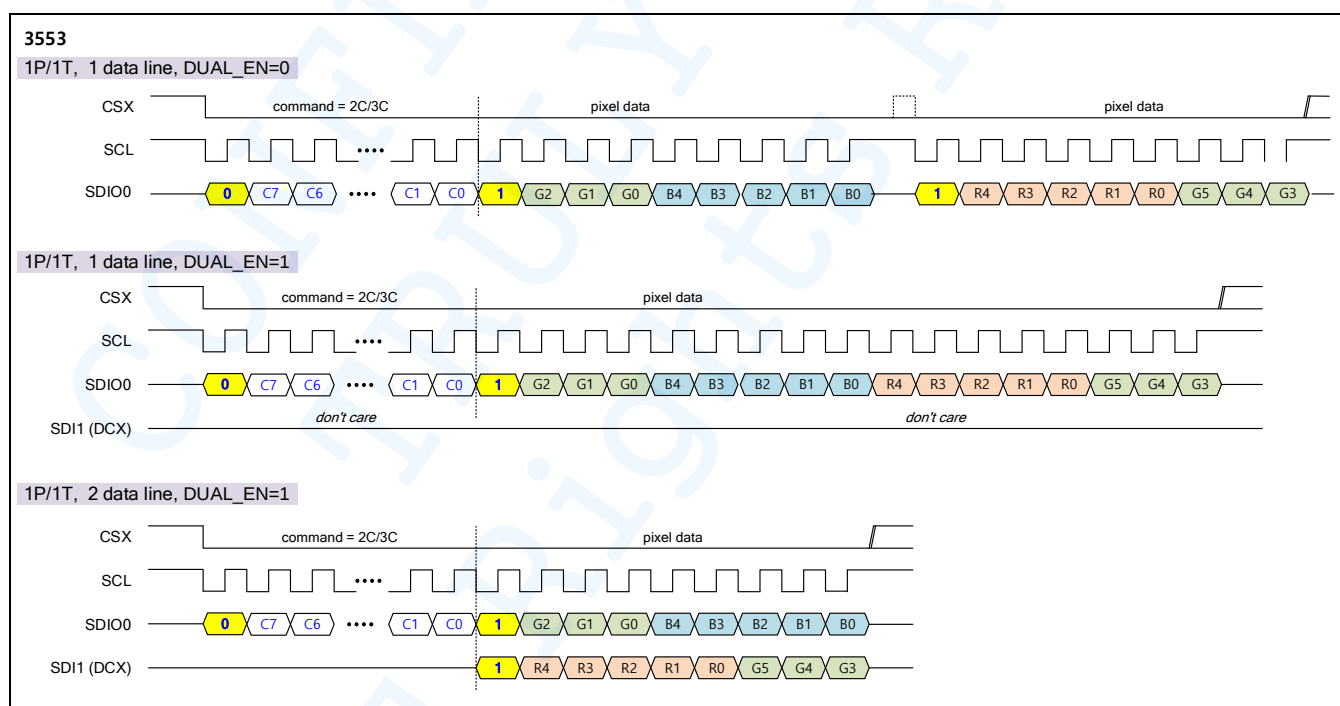


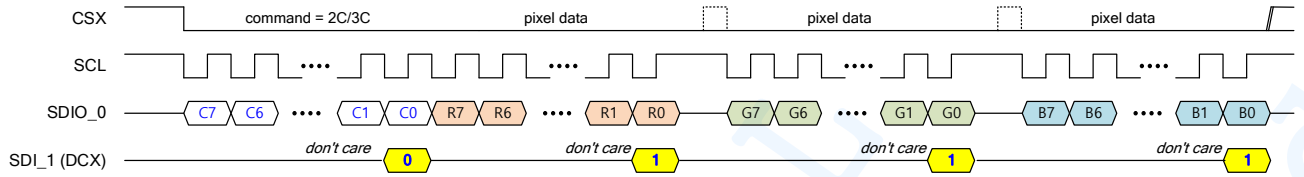
Figure 29 SPI 3-Wire 3553 Pixel Format

SH8501A

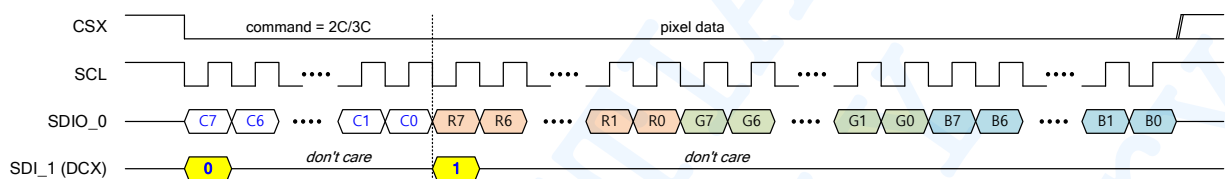
240x240 AMOLED Display Driver IC

888

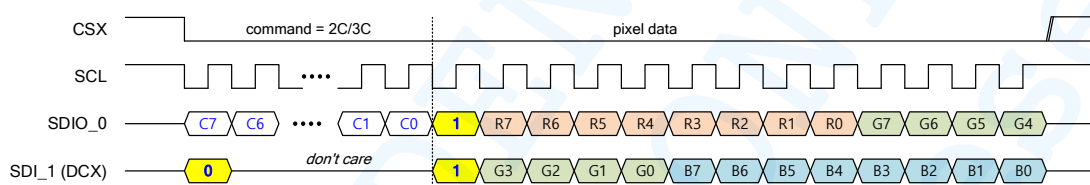
1P/1T, 1 data line, DUAL_EN=0



1P/1T, 1 data line, DUAL_EN=1



1P/1T, 2 data line, DUAL_EN=1



2P/3T, 2 data line, DUAL_EN=1

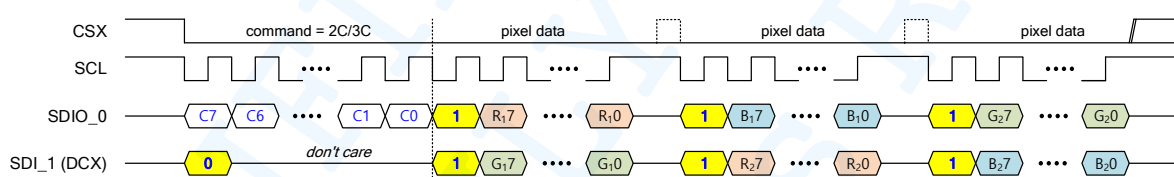


Figure 30 SPI 4-Wire 888 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

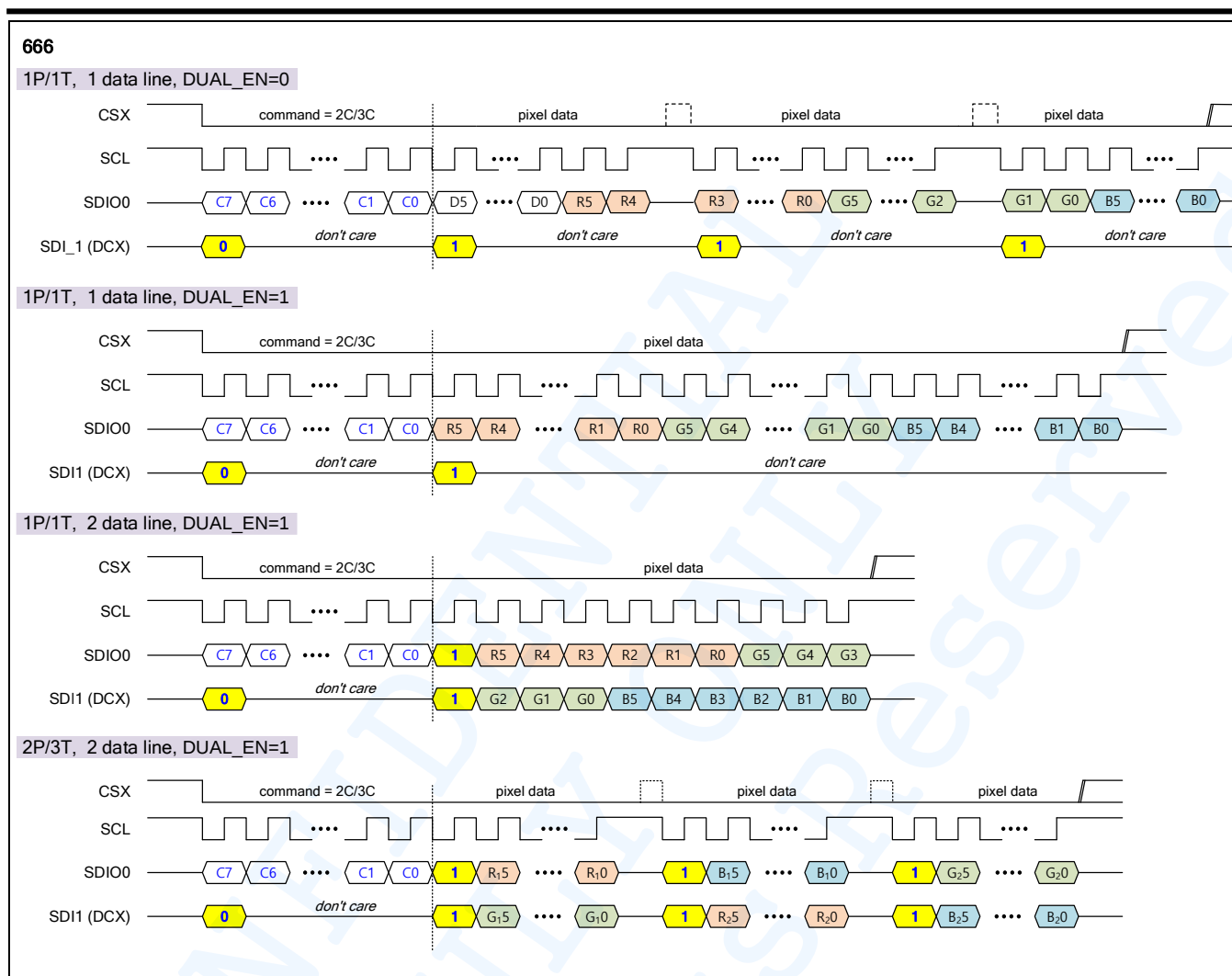


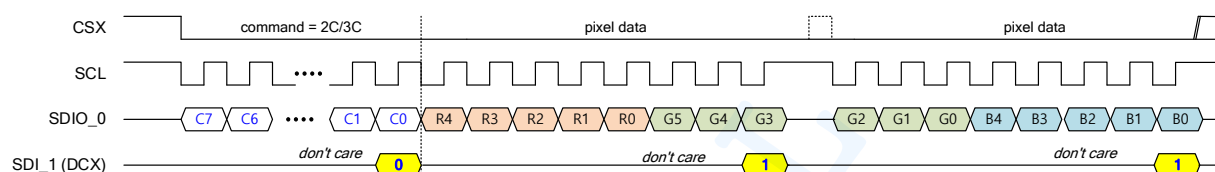
Figure 31 SPI 4-Wire 666 Pixel Format

SH8501A

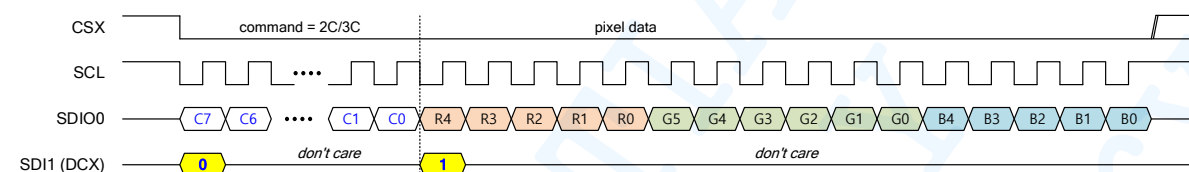
240x240 AMOLED Display Driver IC

565

1P/1T, 1 data line, DUAL_EN=0



1P/1T, 1 data line, DUAL_EN=1



1P/1T, 2 data line, DUAL_EN=1

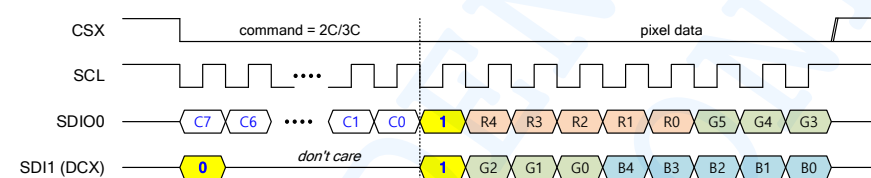
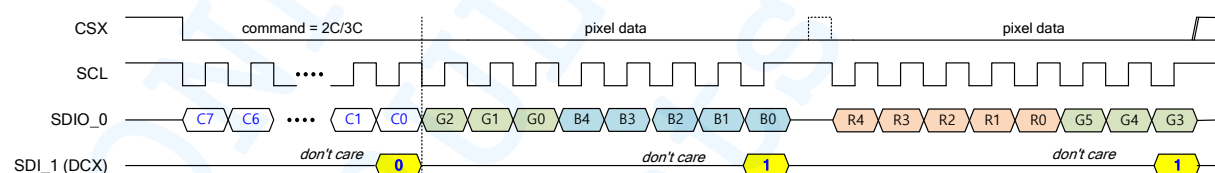


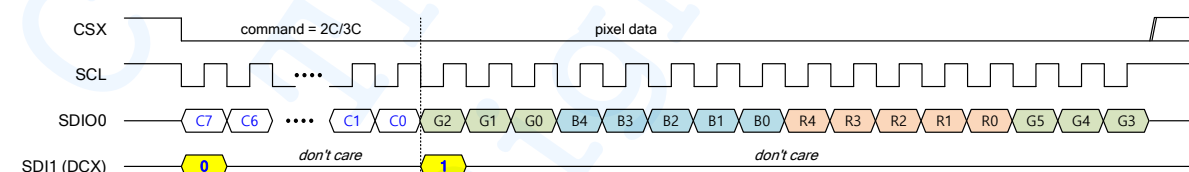
Figure 32 SPI 4-Wire 565 Pixel Format

3553

1P/1T, 1 data line, DUAL_EN=0



1P/1T, 1 data line, DUAL_EN=1



1P/1T, 2 data line, DUAL_EN=1

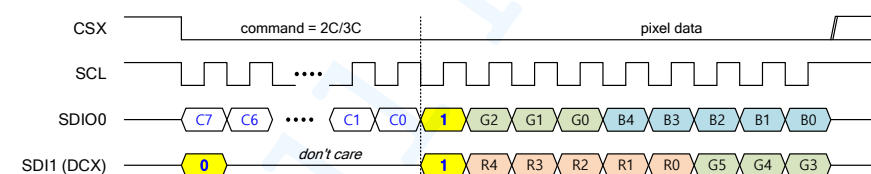


Figure 33 SPI 4-Wire 3553 Pixel Format

4.8 Quad SPI Interface

In addition to MIPI DBI Type-C interface, SH8501A supports Quad-SPI interface. Register read, write interface and RGB pixel interface timing diagrams are shown below. 1-wire or 4-wire option is selected by register SPI_MODE(C4h).

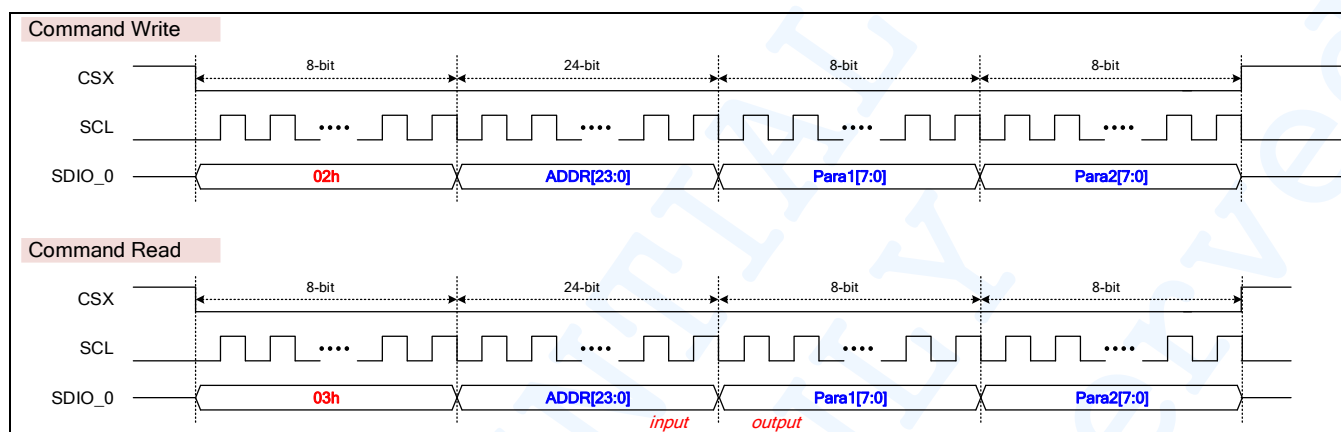


Figure 34 Quad SPI Interface Protocol – Register Read and Write

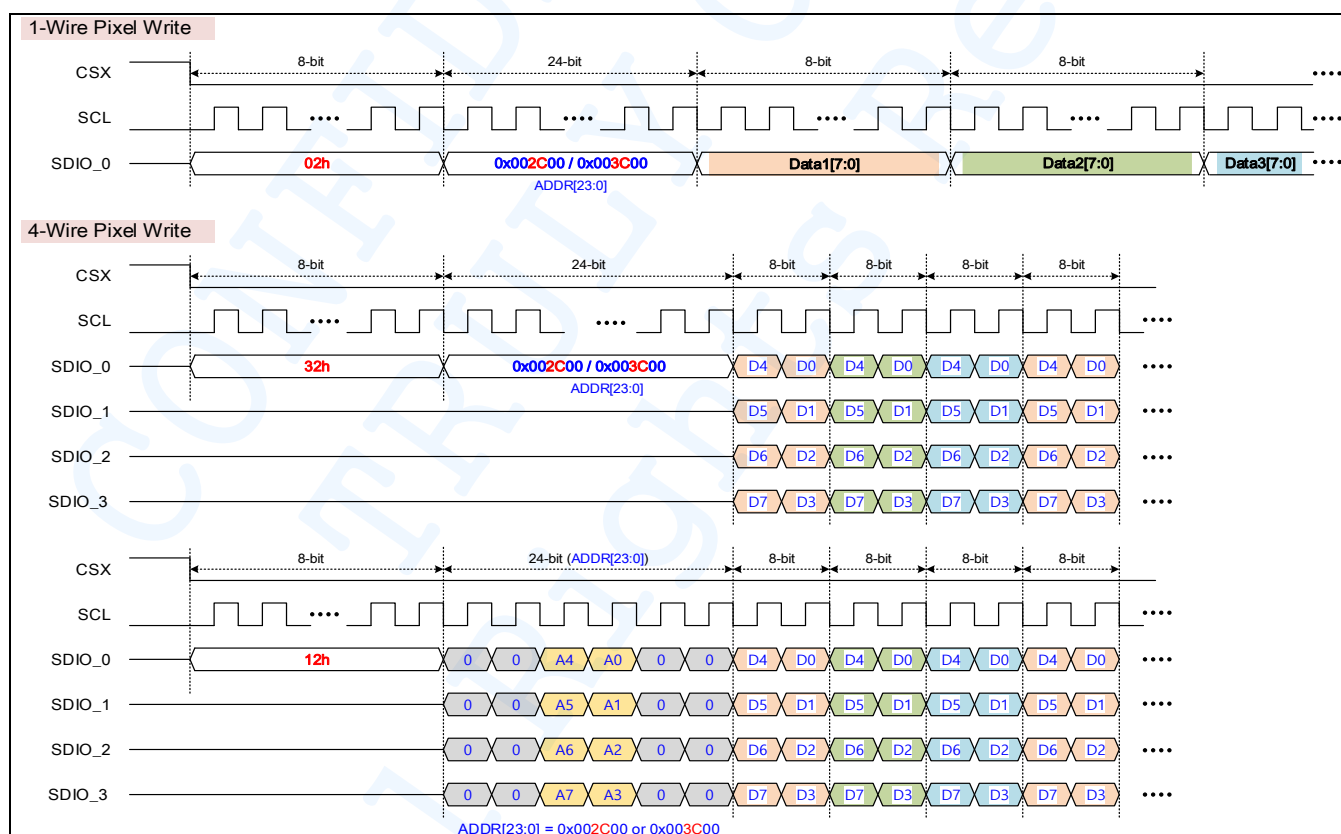


Figure 35 Quad SPI Interface Protocol – 888 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

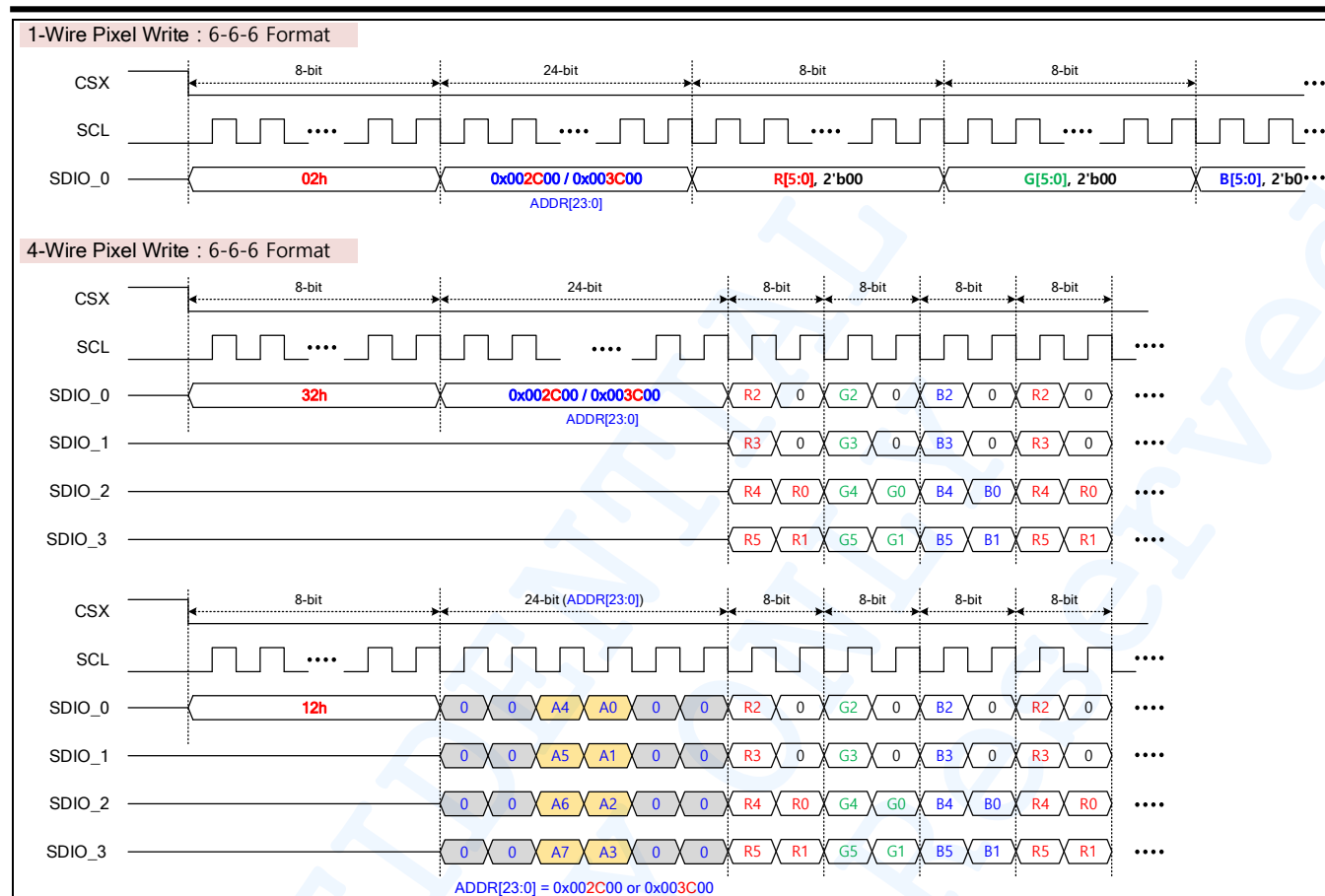


Figure 36 Quad SPI Interface Protocol – 666 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

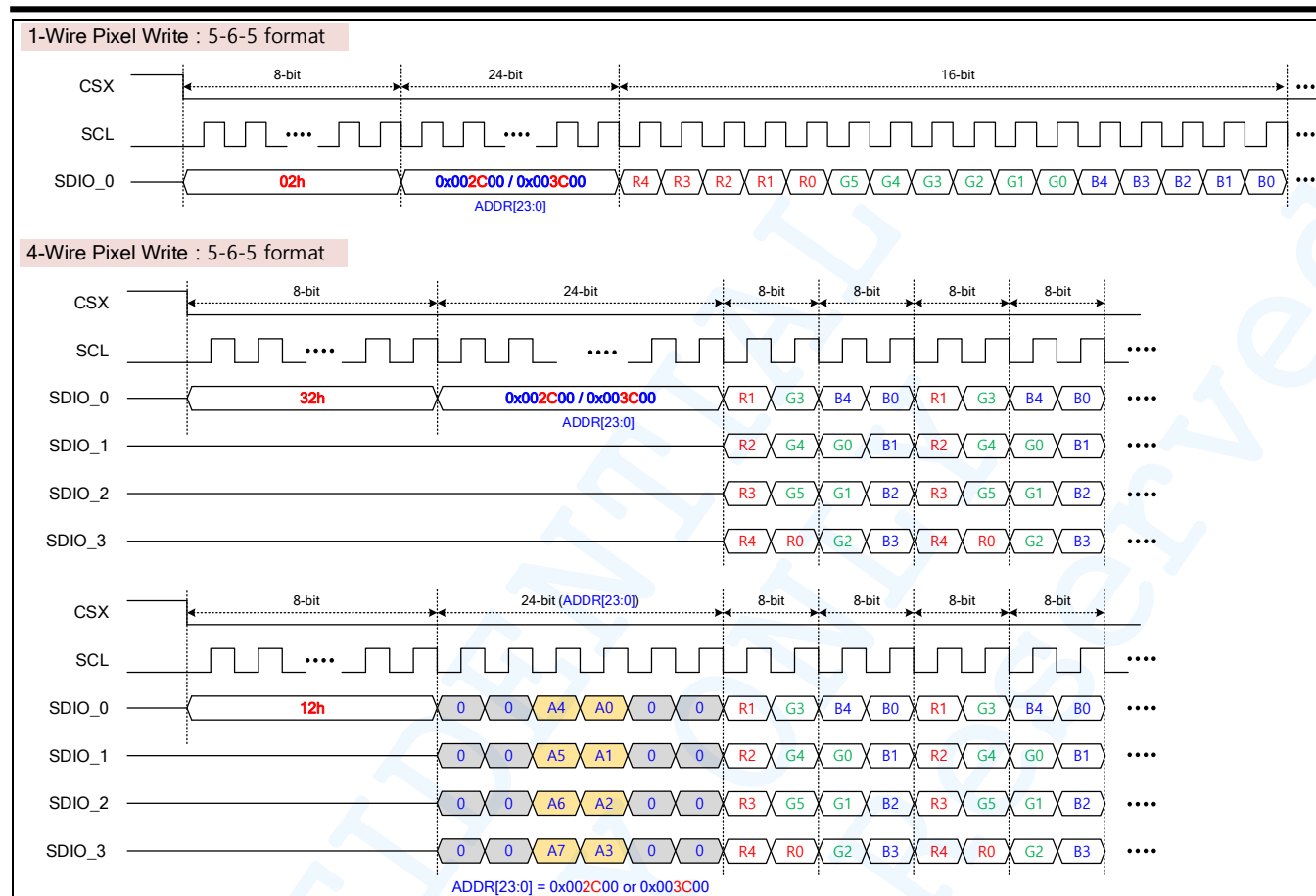


Figure 37 Quad SPI Interface Protocol – 565 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

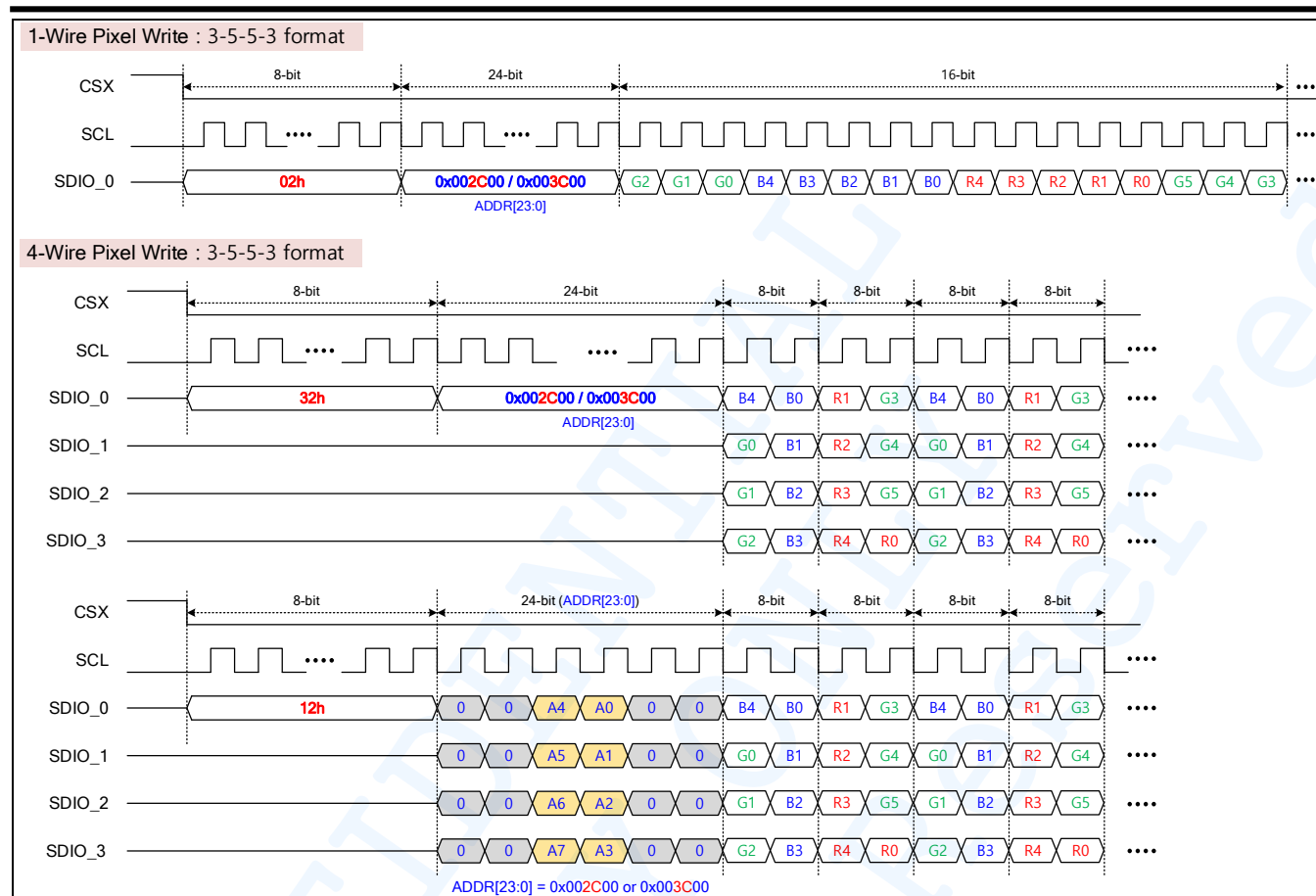


Figure 38 Quad SPI Interface Protocol – 3553 Pixel Format

SH8501A

240x240 AMOLED Display Driver IC

4.9 Extra Pixel Format for SPI Interface

SH8501A supports various pixel formats through SPI interface. Target pixel format is decided by IFPF in COLMOD(0x3A). For 111, 332, and 256-gray pixel formats, SPI transfer RGB image data using register write command (0x2C or 0x3C), not RGB image interface. 8-bit data format for this interface is shown below.

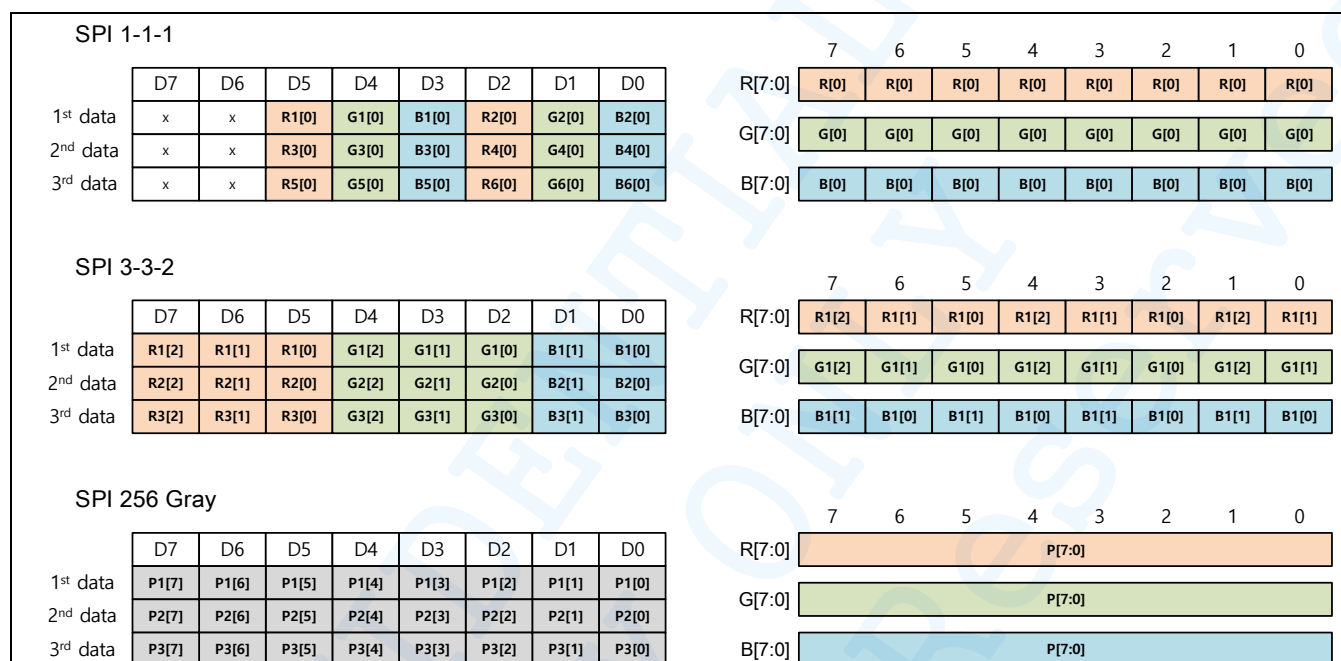


Figure 39 SPI Extra RGB Pixel Format

4.10 MIPI DSI

MIPI (Mobile Industry Processor Interface) DSI (Display Serial Interface) standard defines protocols between a Host (Application Processor) and Client peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards. It builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards. Figure58 shows a simplified DSI interface configuration. From a conceptual viewpoint, a DSI-compliant interface performs the same functions as interfaces based on DBI-2 and DPI-2 standards or similar parallel display interfaces. It sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals. From a system or software point of view, the serialization and deserialization operations should be transparent. The most visible, and unavoidable, consequence of transformation to serial data and back to parallel is increased latency for transactions that require a response from the peripheral. For example, reading a pixel from the frame buffer on a display module has a higher latency using DSI than DBI. Another fundamental difference is the host processor's inability during a read transaction to throttle the rate, or size, of returned data.

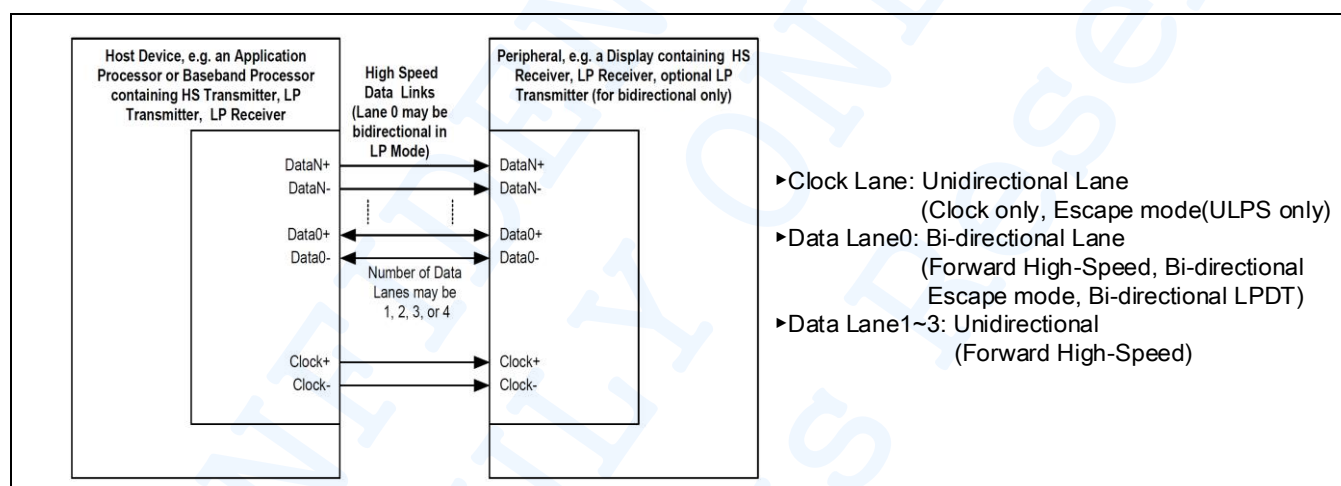


Figure 40 DSI Tx and Rx Interface Configuration

4.10.1 DSI Feature

- Support One Data lane and Clock lane.
- High speed(HS) transmissions(uni-direction) and Low Power(LP) transmission(bi-direction)
- Clock lane supports ULPS mode
- Support Command and Video mode
- Support Tearing effect (TE) signal
- Diagnostic function - Checksum and ECC error
- Functionality supported by Escape mode
- Packet-Based Protocol

	MIPI Alliance Specification for D-PHY	MIPI Alliance Specification for DSI
Version	1.0	1.02
Date	Sep 22, 2009	Oct 20, 2010

4.10.2 DSI Layer Definitions

A conceptual view of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 25 and it consists of 4 types such as Application Layer, Low level protocol Layer, Lane management Layer and PHY Layer.

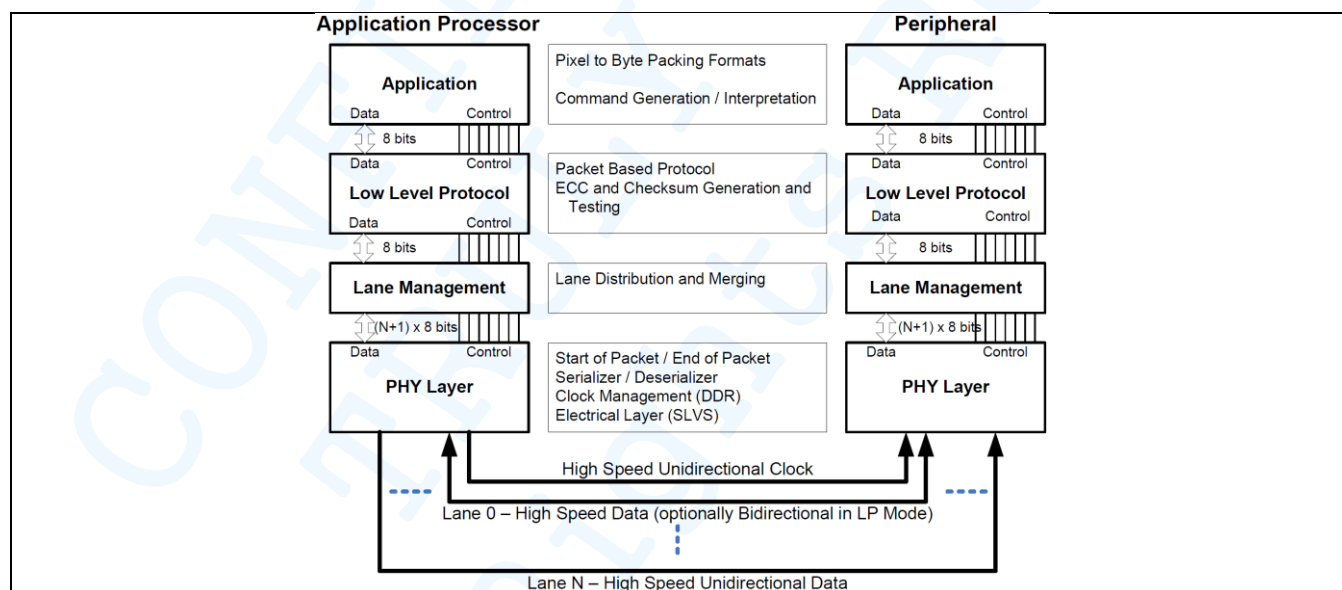


Figure 41 MIPI DSI Layers

4.10.3 Command and Video Mode

DSI-compliant peripherals support either of two basic modes of operation, Command mode and Video mode. The mode used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other

applications. Typically, a peripheral is capable of Command mode operation or Video mode operation. Some Video mode display modules also include a simplified form of Command mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

4.10.4 DSI Physical Layer (D-PHY)

The D-PHY provides a synchronous connection between master and slave. A practical PHY configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the master and terminating at the slave. The data signals can be either unidirectional or bi-directional, depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the link.

4.10.4.1 Lane State Definition

Display module uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power(LP) mode or High Speed(HS) mode. The State Codes of the High Speed(HS) mode and Low Power(LP) mode lane pair are defined Table 27. All LP state periods shall be at least T_{LPX} in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines.

Table 31 MIPI Lane State Description

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

NOTE:

1. During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.
2. If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

4.10.4.2 Global Operation Flow Diagram

Below figure shows the operational flow diagram for a Data Lane Mode. Within both Tx and Rx four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization.

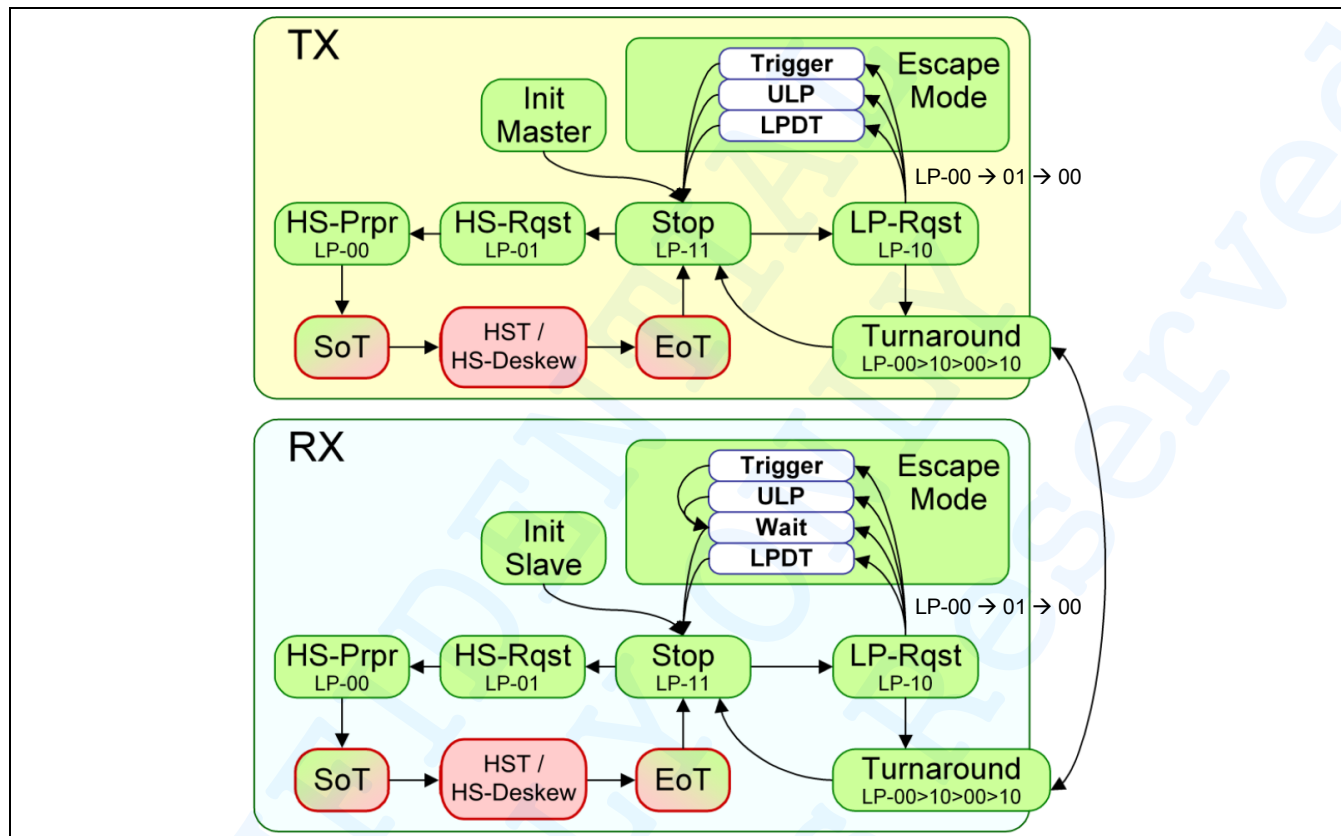


Figure 42 MIPI PHY Data Lane Mode State Diagram

4.10.4.3 Clock Lane Mode State Diagram

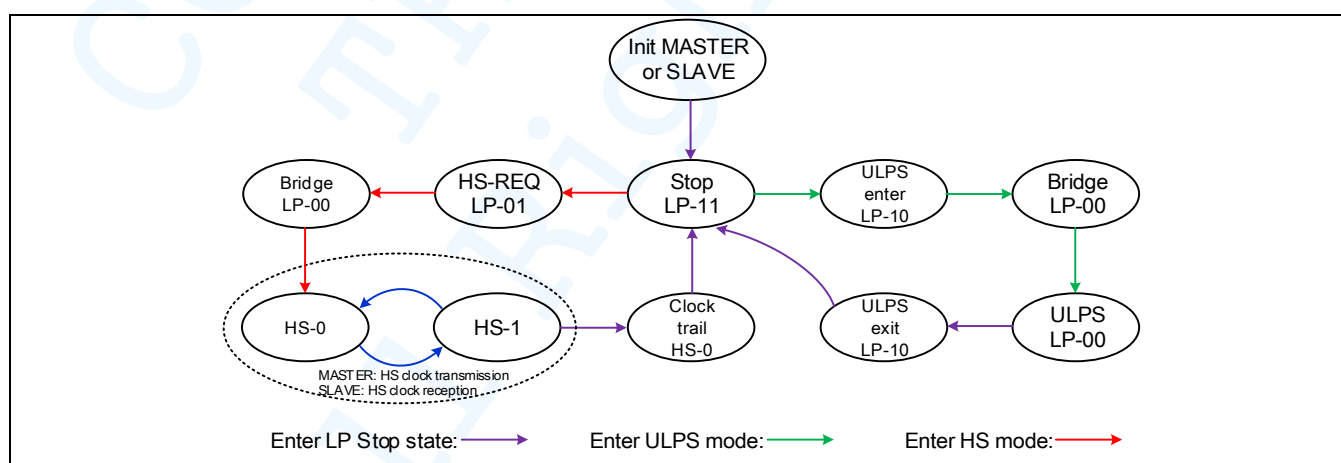


Figure 43 Clock Lane Module State Diagram

4.10.4.3.1 Clock Lane Switching

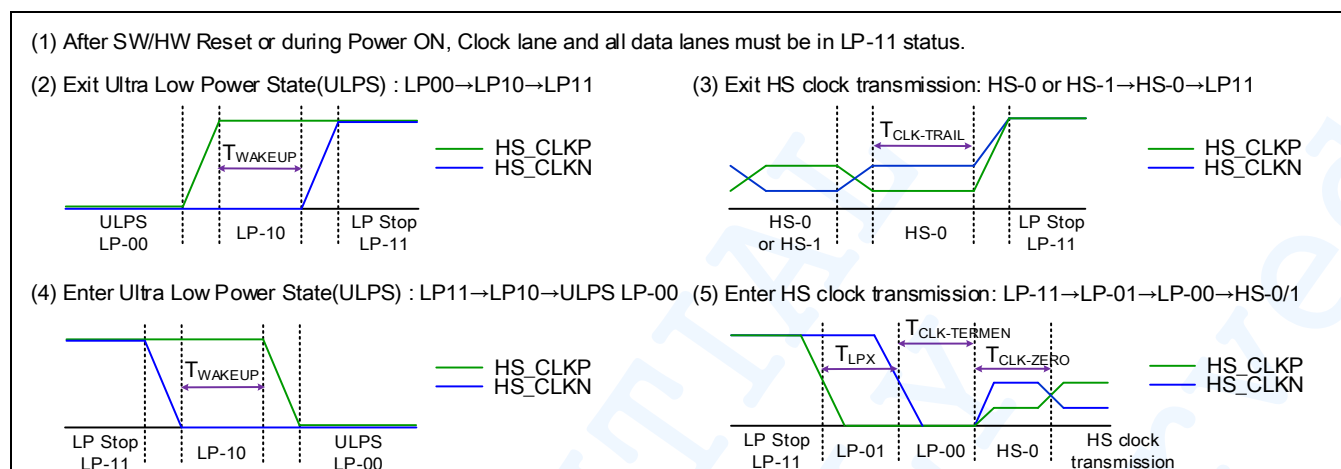


Figure 44 Clock Lane Switching State Diagram

4.10.4.4 HS (High Speed) Data Transmission Burst

The [Figure 45](#) shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

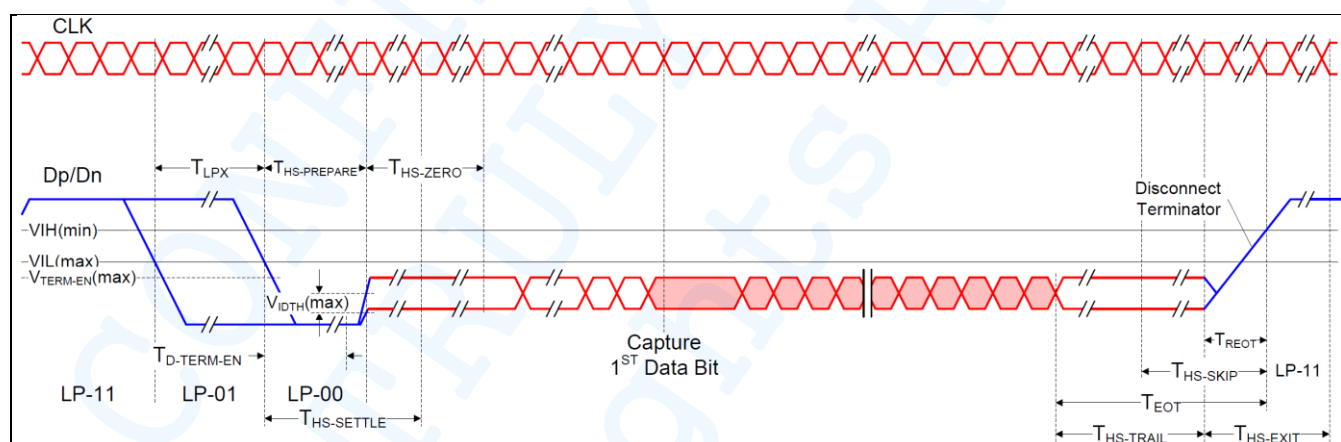


Figure 45 High-Speed Data Transmission in Bursts

4.10.4.5 High Speed Clock Transmission

The [Figure 46](#) shows the sequence of the high speed clock transmission. In high speed mode the clock lane provides a low-swing differential DDR clock signal from Master to Slave for high speed data transmission.

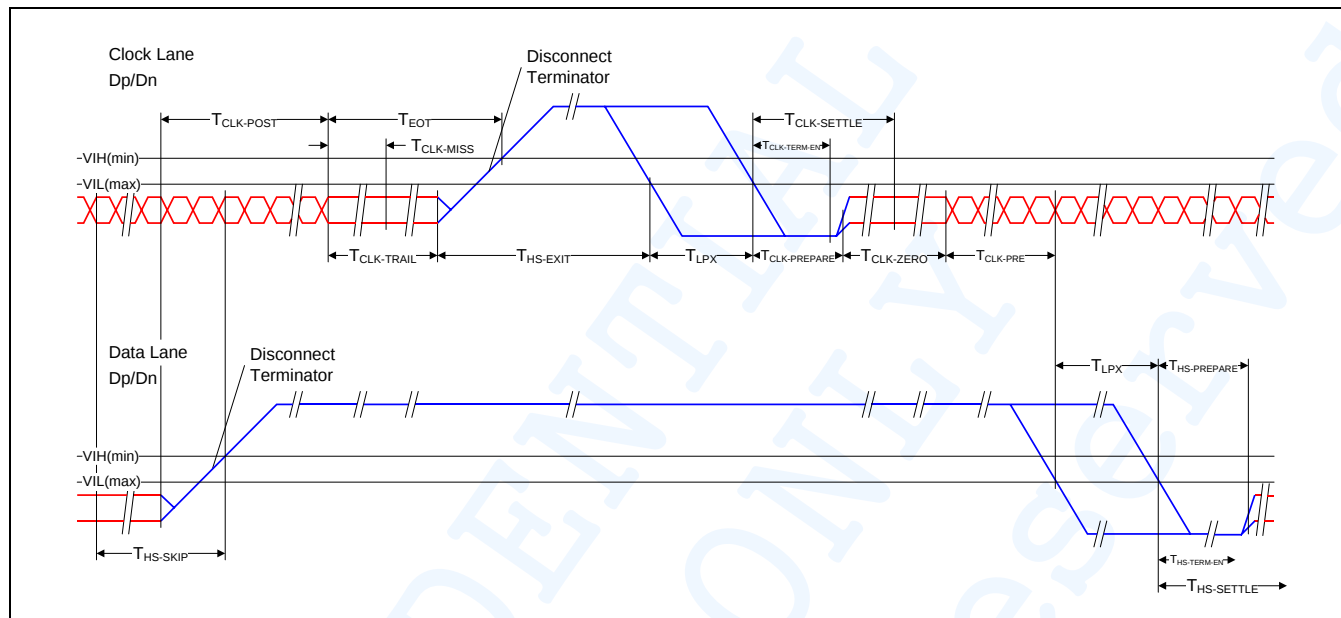


Figure 46 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

4.10.4.6 Bi-Directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Master and Slave side shall not be changed by Turnaround. Link Turnaround shall be handled completely in Control mode. The low power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low Power State Periods, T_{LPX} is constrained to ensure proper Turnaround behavior. The $T_{LPX}(\text{master})/T_{LPX}(\text{slave})$ shall be between $2/3$ (0.667) and $3/2$ (1.50). The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between a host processor and a peripheral.

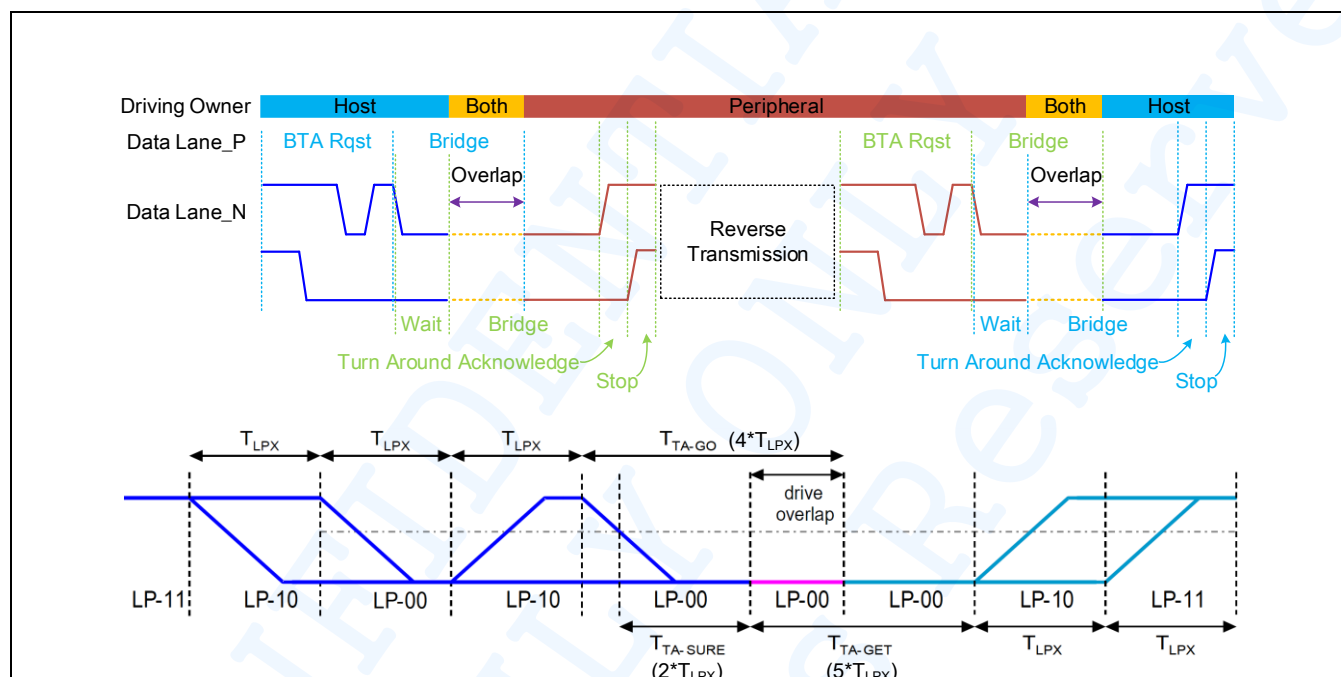


Figure 47 Bus Turn Around procedure

Figure 48 shows an example of BTA operations. The SLAVE get the lane controllability by BTA procedure to send the acknowledge packet on the successful data reception if there is no Error and send the acknowledge with error packet on the data reception if Error is occurred.

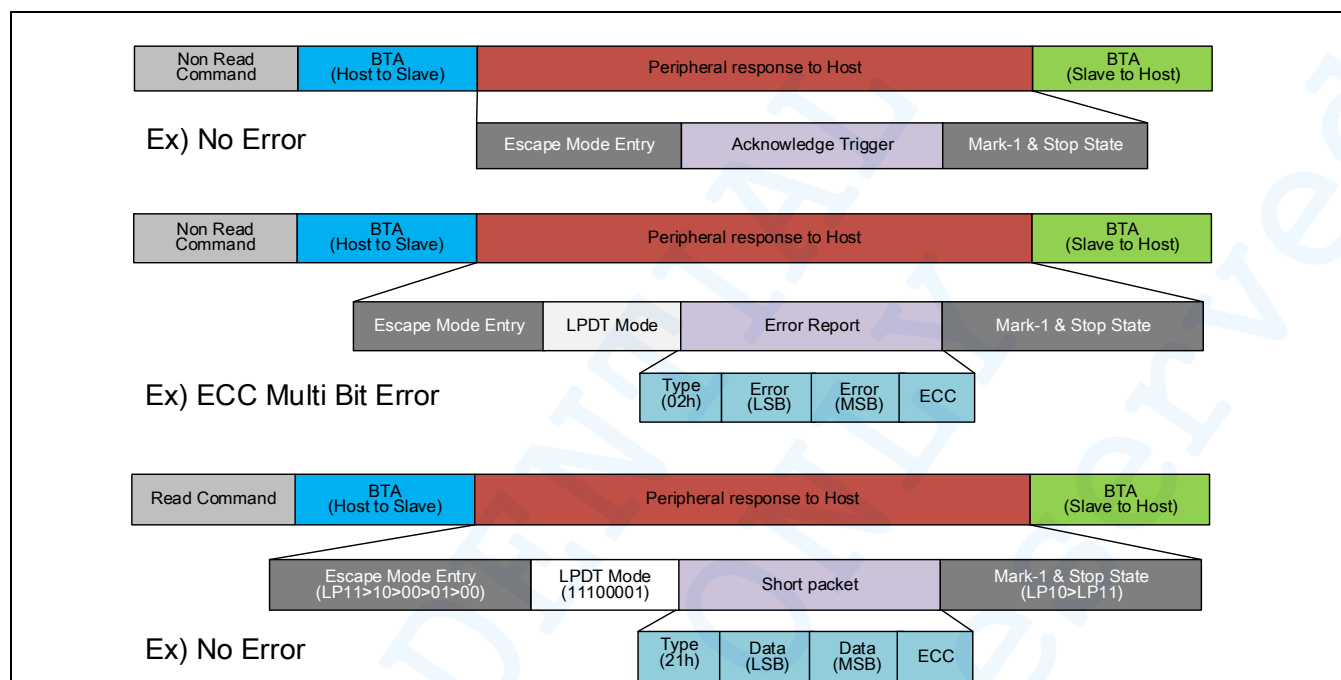


Figure 48 BTA Operation – No Error/Error after Non-Read Command

4.10.4.7 Escape Mode

Escape Mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and is optional in the Reverse direction. If supported, Escape mode does not have to include all available features. A Data Lane shall enter Escape Mode via an Escape Mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape Mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape Mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state. Once Escape Mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Below table lists all currently available Escape Mode commands and actions. All unassigned commands are reserved for future expansion.

Table 32 MIPI Escape Mode Entry Code

Escape Mode Action	Command Type	Entry Command Pattern (First Bit Transmitted to Last Bit Transmitted)	SH8501A	
			LP-Rx	LP-Tx
Low-power data transmission	mode	11100001 (87h)	O	O
Ultra-low power state	mode	00011110 (78h)	O	–
Undefined-1	mode	10011111 (F9h)	–	–
Undefined-2	mode	11011110 (7Bh)	–	–
Reset-trigger (Remote Application)	Trigger	01100010 (46h)	O	–
TE trigger	Trigger	01011101 (BAh)	–	O
Unknown-4 (Acknowledge trigger)	Trigger	00100001 (84h)	–	O
Unknown-5	Trigger	10100000 (05h)	–	–

The complete Escape mode action for a Trigger-Reset command is shown as follows. It shows the sequence of the low power data transmission.

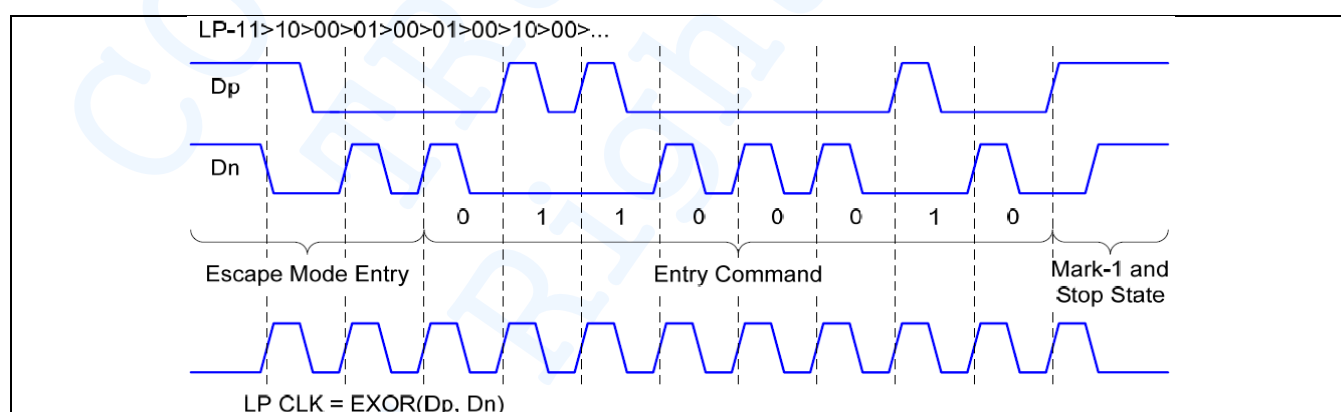


Figure 49 Trigger-Reset Command in Escape Mode

4.10.4.7.1 Escape mode Low-Power Data Lane Operation

If the Escape Mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. The PHY in Escape mode shall apply Spaced-One-Hot bit encoding for asynchronous communication. Therefore, operation of a Data Lane in this mode does not depend on the Clock Lane.

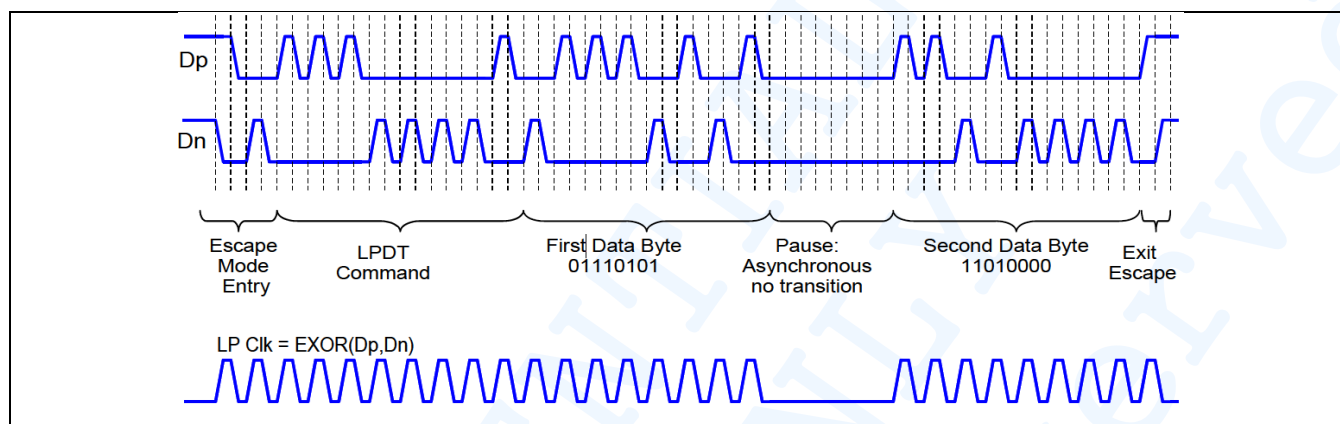


Figure 50 Data Byte Low-Power Data Transmission

4.10.4.7.2 Remote Application Reset

Remote Application Reset Command is used in case of transmission from the host processor to the peripheral. If the Entry Command Pattern matches the Remote Application Reset Command a Trigger is flagged to the protocol at the peripheral side via the logical PPI. The host processor can send software reset trigger by Remote Application Reset Packet.



Figure 51 Remote Application Reset

4.10.4.7.3 TE Signaling in DSI

A Command Mode display module has its own timings controller and local frame buffer for display refresh. In some cases, the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bi-directional Data Lane. The PHY for DSI has no inherent interrupt capability from peripheral to host processor so the host processor shall give bus ownership to the peripheral for extended periods, as it does not know when the peripheral will send the TE message. Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or request to the display module, because it does not have bus possession. The TE Signaling function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_off. After sending set_tear_on to enable this function, the host processor ends the transmission with BTA asserted, giving bus possession to the display module. Since the display module's DSI protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession. To enable TE Reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE Signaling has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode which gives bus possession to the display module. This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

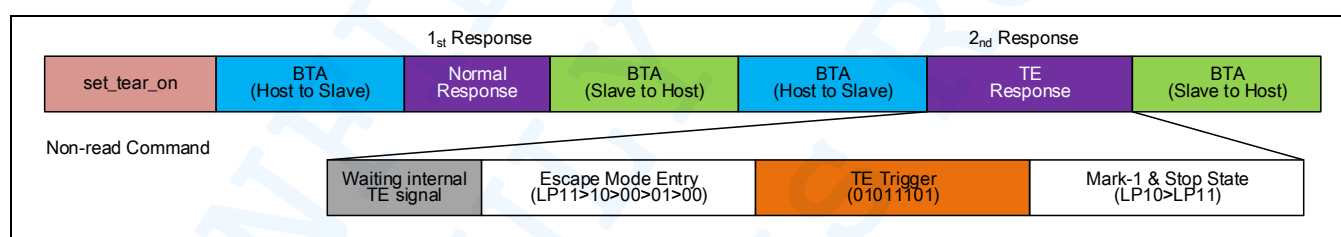


Figure 52 BTA Mode-TE Signaling

4.10.5 MIPI DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. If there are multiple Lanes, the Lane Management layer distributes bytes to separate PHYs, one PHY per Lane. Packet protocol and formats are independent of the number of Lanes used.

4.10.5.1 Multiple Packets per Transmission

The MIPI CORE of SH8501A supports four data transmission defined in MIPI DSI specification. And in order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp packet can be enabled or disabled with register.

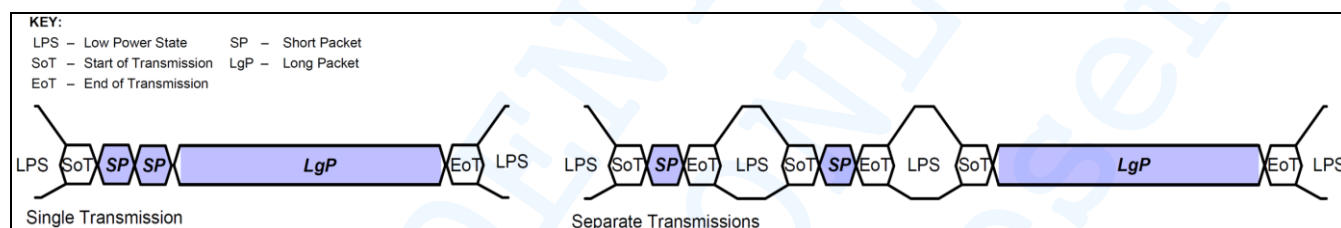


Figure 53 HS Transmission Examples with EoTp disabled

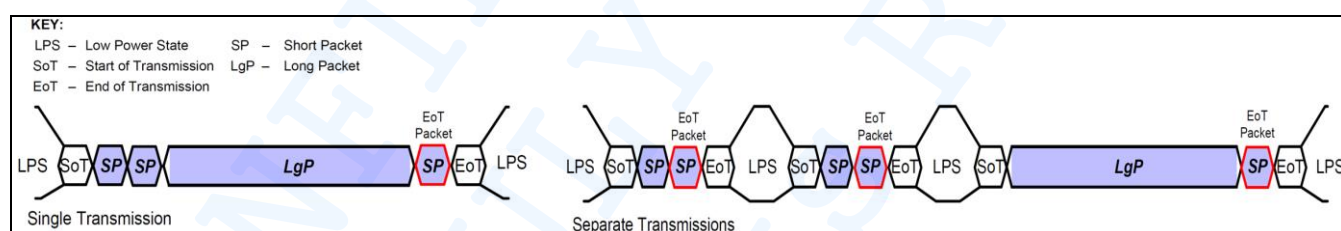


Figure 54 HS Transmission Examples with EoTp enabled

4.10.5.2 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. [Figure 55](#) shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

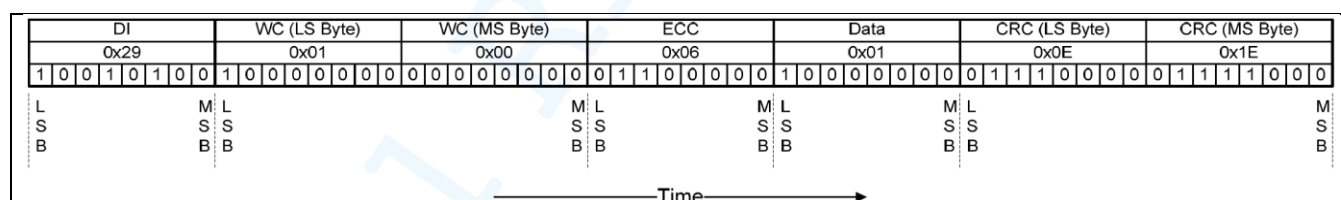


Figure 55 Endian Example (Long Packet)

4.10.5.3 General Packet Structure

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet.

4.10.5.3.1 Long Packet Format

Figure 44 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. In the Long Packet, Packet Footer is added after Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

The Checksum (2 bytes) shall be realized as a 16bit CRC (Packet Data): $\text{Polynomial} = X^{16} + X^{12} + X^5 + X^0$

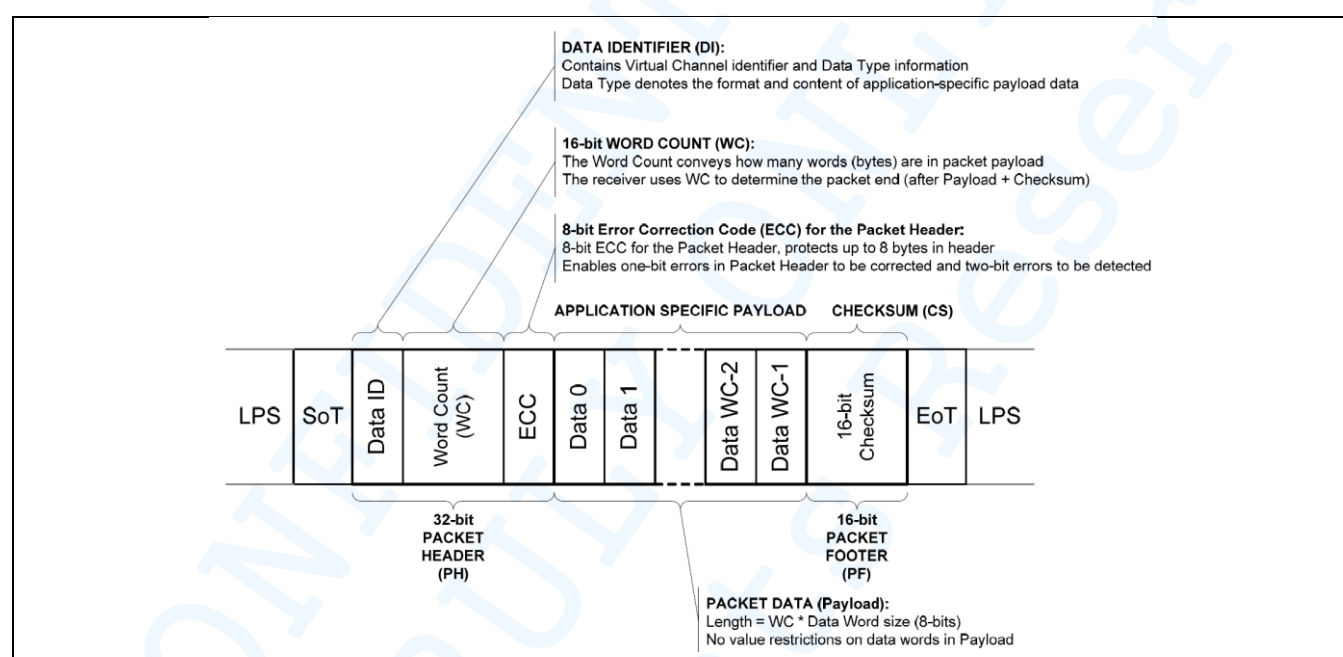


Figure 56 Long Packet Structure

4.10.5.3.2 Short Packet Structure

Figure 75 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC. a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

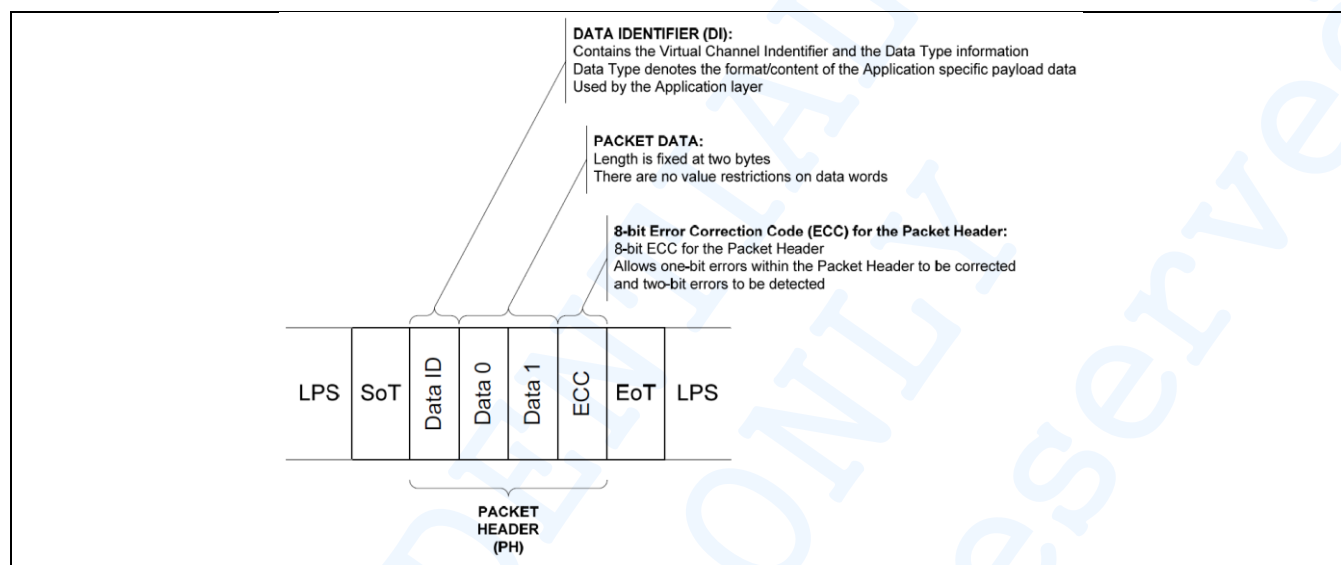


Figure 57 Short Packet Structure

4.10.5.4 Common Packet Element

Long and Short packets have several common elements.

4.10.5.4.1 Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 45 shows the composition of the Data Identifier (DI) byte.

DI[7:6] - These two bits identify the data as directed to one of four virtual channels.

DI[5:0] - These six bits specify the Data Type.

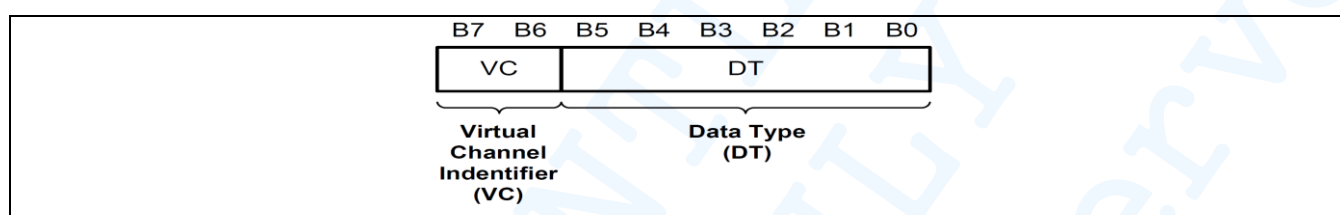


Figure 58 Data Identifier Byte

4.10.5.4.1.1 Virtual Channel Identifier – VC field DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

4.10.5.4.1.2 Data Type Field – DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start/end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

4.10.5.4.2 Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications. ECC is generated from the twenty-four data bits within the Packet Header as illustrated in Figure 46.

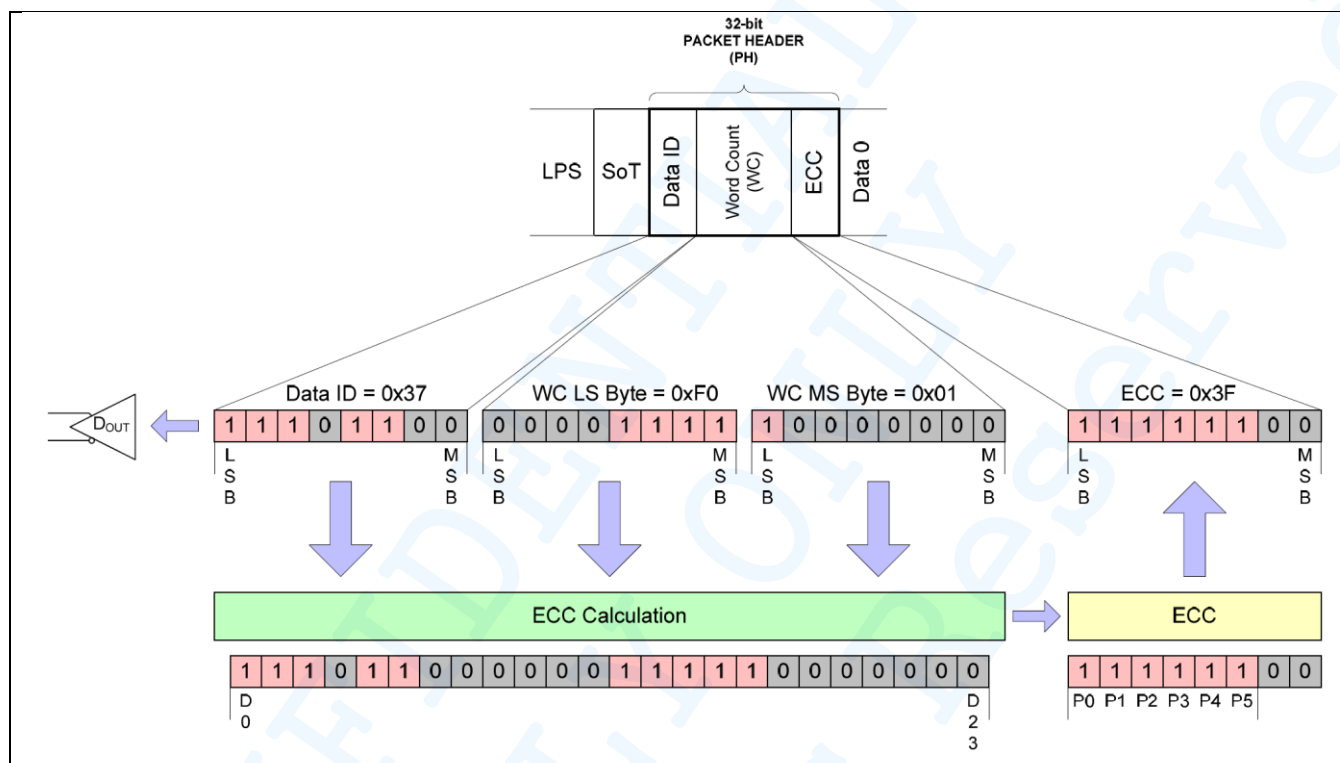


Figure 59 24bit ECC generation on TX side

P7=0

P6=0

$P5 = D10 \oplus D11 \oplus D12 \oplus D13 \oplus D14 \oplus D15 \oplus D16 \oplus D17 \oplus D18 \oplus D19 \oplus D21 \oplus D22 \oplus D23$

$P4 = D4 \oplus D5 \oplus D6 \oplus D7 \oplus D8 \oplus D9 \oplus D16 \oplus D17 \oplus D18 \oplus D19 \oplus D20 \oplus D22 \oplus D23$

$P3 = D1 \oplus D2 \oplus D3 \oplus D7 \oplus D8 \oplus D9 \oplus D13 \oplus D14 \oplus D15 \oplus D19 \oplus D20 \oplus D21 \oplus D23$

$P2 = D0 \oplus D2 \oplus D3 \oplus D5 \oplus D6 \oplus D9 \oplus D11 \oplus D12 \oplus D15 \oplus D18 \oplus D20 \oplus D21 \oplus D22$

$P1 = D0 \oplus D1 \oplus D3 \oplus D4 \oplus D6 \oplus D8 \oplus D10 \oplus D12 \oplus D14 \oplus D17 \oplus D20 \oplus D21 \oplus D22 \oplus D23$

$P0 = D0 \oplus D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7 \oplus D10 \oplus D11 \oplus D13 \oplus D16 \oplus D20 \oplus D21 \oplus D22 \oplus D23$

4.10.5.5 Processor to Peripheral Direction (Processor – Sourced) Packet Data Type

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 28.

Table 33 Data Types for Processor-Sourced Packets

Data Type		Description	Packet Size
(Hex)	(Binary)		
01h	00 0001	Sync event, V sync start	Short
11h	01 0001	Sync event, V sync end	Short
21h	10 0001	Sync event, H sync start	Short
31h	11 0001	Sync event, H sync end	Short
08h	00 1000	End of transmission packet	Short
02h	00 0010	Color mode (CM) off command	Short
12h	01 0010	Color mode (CM) on command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS WRITE, no parameters	Short
15h	01 0101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set maximum return packet size	Short
09h	00 1001	Null packet, no data	Long
19h	01 1001	Blanking packet, no data	Long
29h	10 1001	Generic long write	Long
39h	11 1001	DCS long write/write_LUT command packet	Long
0Eh	00_1110	Packet pixel stream, 16-bit RGB 565 format	Long
1Eh	01_1110	Packet pixel stream, 18-bit RGB 666 format	Long
2Eh	10_1110	Packet pixel stream, 18-bit RGB Loosely 666 format	Long
3Eh	11 1110	Packed pixel stream, 24-bit RGB, 888 format	Long
x0h&Fh	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	—

NOTE: Unspecified codes are reserved.

4.10.5.6 Peripheral to Processor Direction (Processor – Sourced) Packet Data Type

Table 29 presents the complete set of peripheral to processor data types.

Table 34 Data Types for Peripheral-Sourced Packets

Data Type		Description	Packet Size
(Hex)	(Binary)		
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge with error report	Short
03h – 07h	00 0011 – 00 0111	Reserved	–
08h	00 1000	End of transmission packet	Short
09h – 10h	00 1001 – 01 0000	Reserved	–
11h	01 0001	Generic Short READ response, 1 byte returned	Short
12h	01 0010	Generic Short READ response, 2 bytes returned	Short
13h – 18h	01 0011 – 01 1000	Reserved	–
1Ah	01 1010	Generic long READ response	Long
1Bh	01 1011	Reserved	–
1Ch	01 1100	DCS long READ response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	–
21h	10 0001	DCS Short READ response, 1 byte returned	Short
22h	10 0010	DCS Short READ response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	–

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4.10.5.7 Color Format

There are several data packet structure for pixel data transmission, 16-bit (5-6-5) format, two 18-bit (6-6-6) formats, 24-bit format (8-8-8) and the data packet structures.

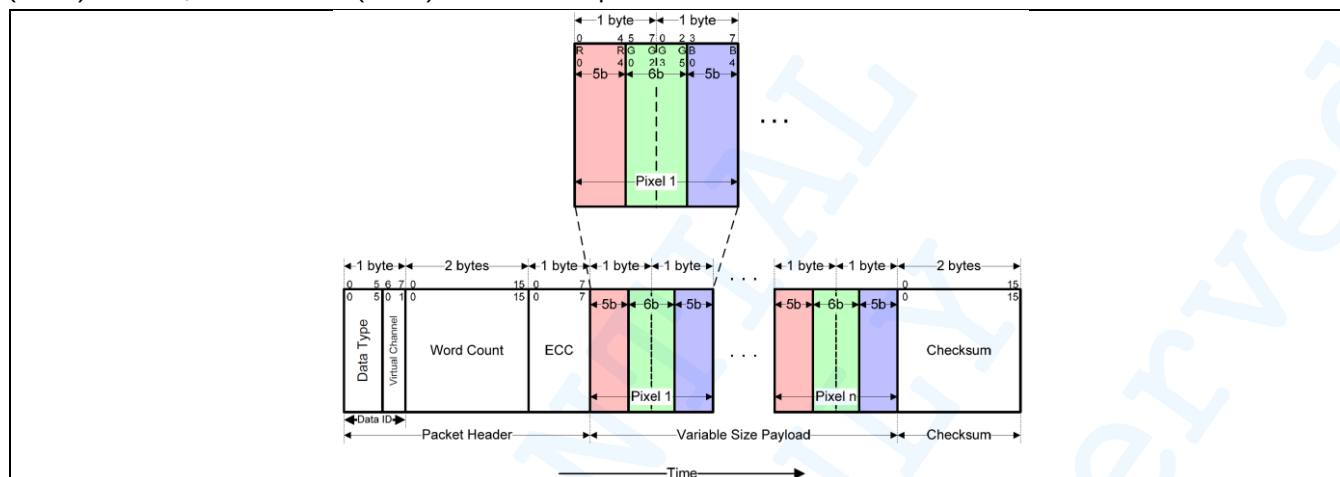


Figure 60 16-bit per Pixel - RGB Color Format, Long Packet

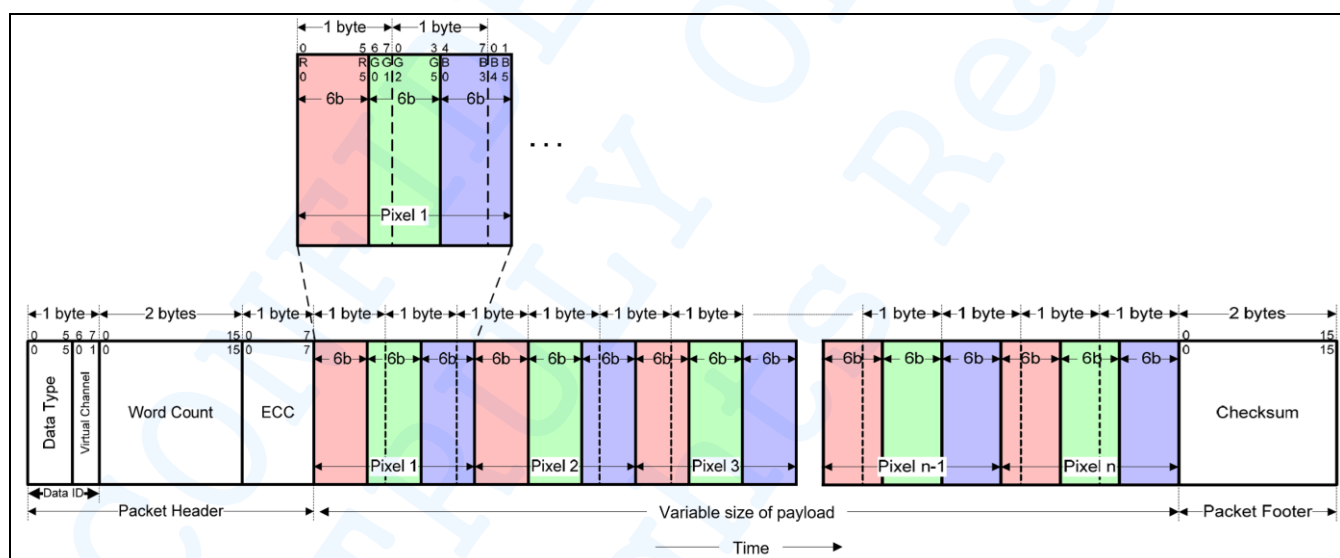


Figure 61 18-bit per Pixel (Packed) - RGB Color Format, Long Packet

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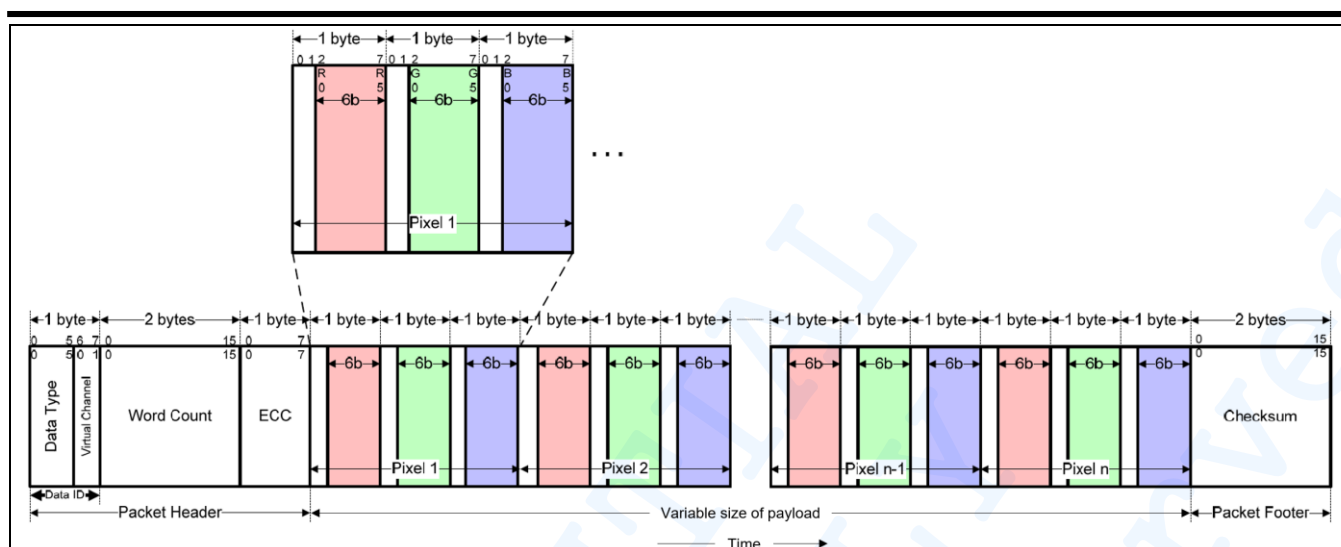


Figure 62 18-bit per Pixel(Loosely Packed) - RGB Color Format, Long Packet

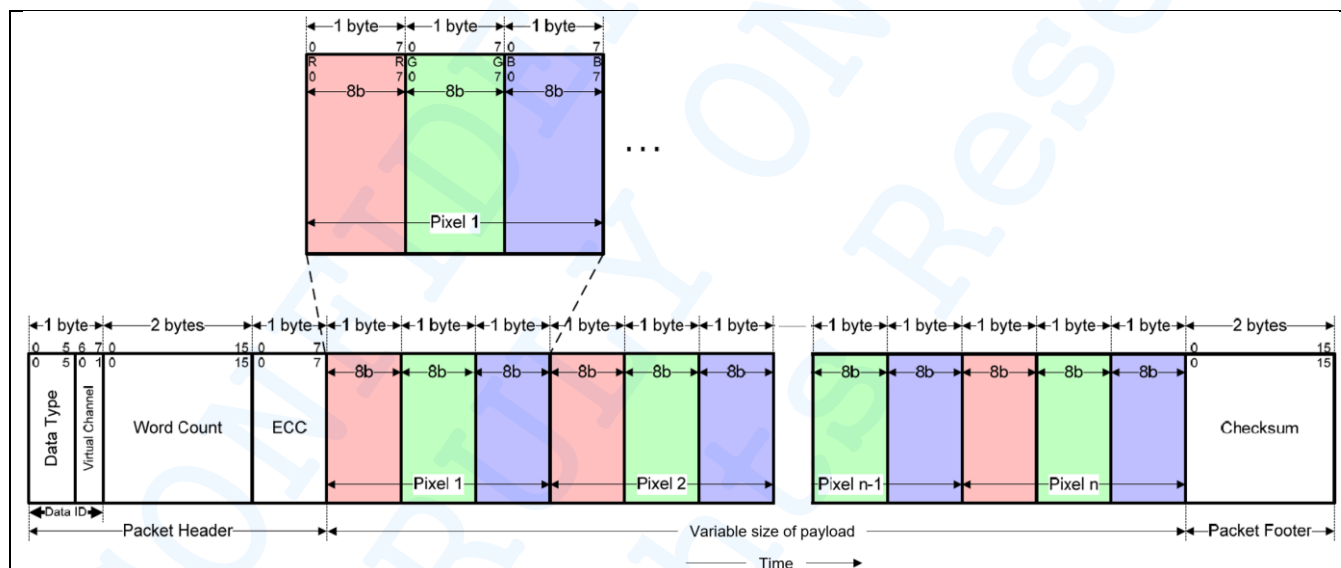


Figure 63 24-bit per Pixel RGB Color Format, Long Packet

4.10.5.8 Error Report Packet

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”.

Table 35 Error Report Bit Definitions

Bit	Description
0	SoT error
1	SoT sync error
2	EoT sync error
3	Escape Mode Entry command error
4	Low-power transmit sync error
5	HS receive timeout error (Timeout error)
6	False control error
7	Contention detection error
8	ECC error, single-bit (Detected and corrected)
9	ECC error, multi-bit (Detected, not corrected)
10	Checksum error (Long packet only)
11	DSI data type not recognized
12	DSI VC ID invalid
13	Invalid transmission length
14	Reserved
15	DSI protocol violation

4.10.5.9 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

4.10.5.9.1 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses.

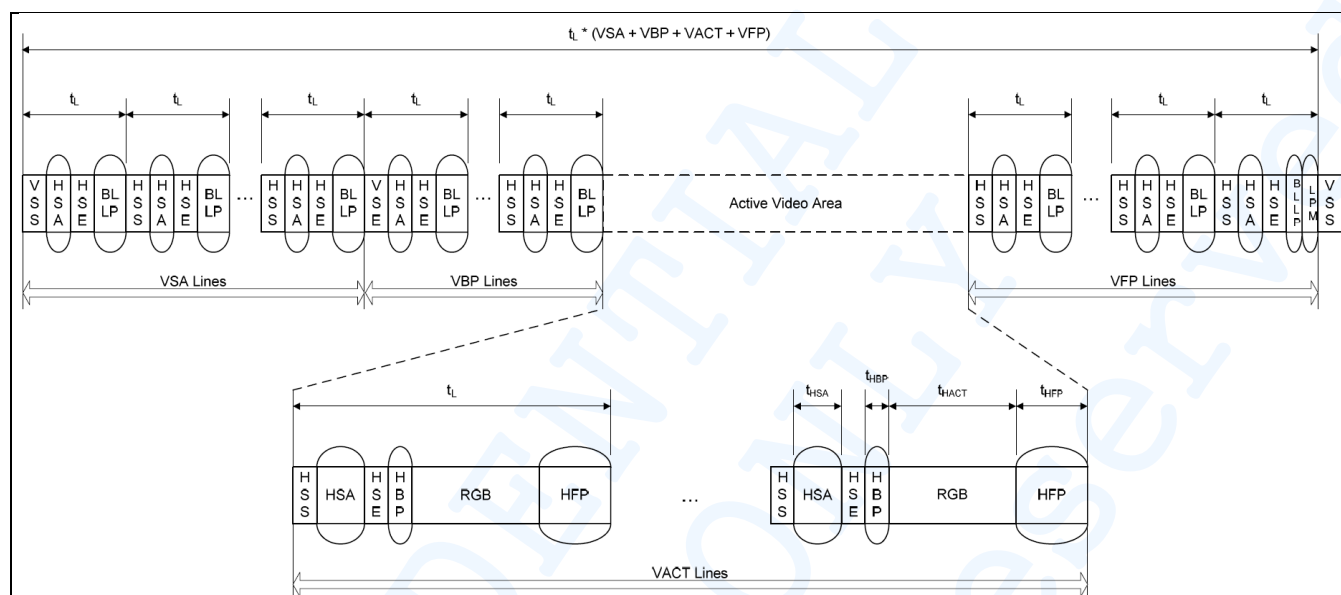


Figure 64 Non-Burst Transmission with Sync Start and End

4.10.5.9.2 Non-Burst Mode with Sync Events

This mode is a simplification of the format described in section 8.11.2. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2.

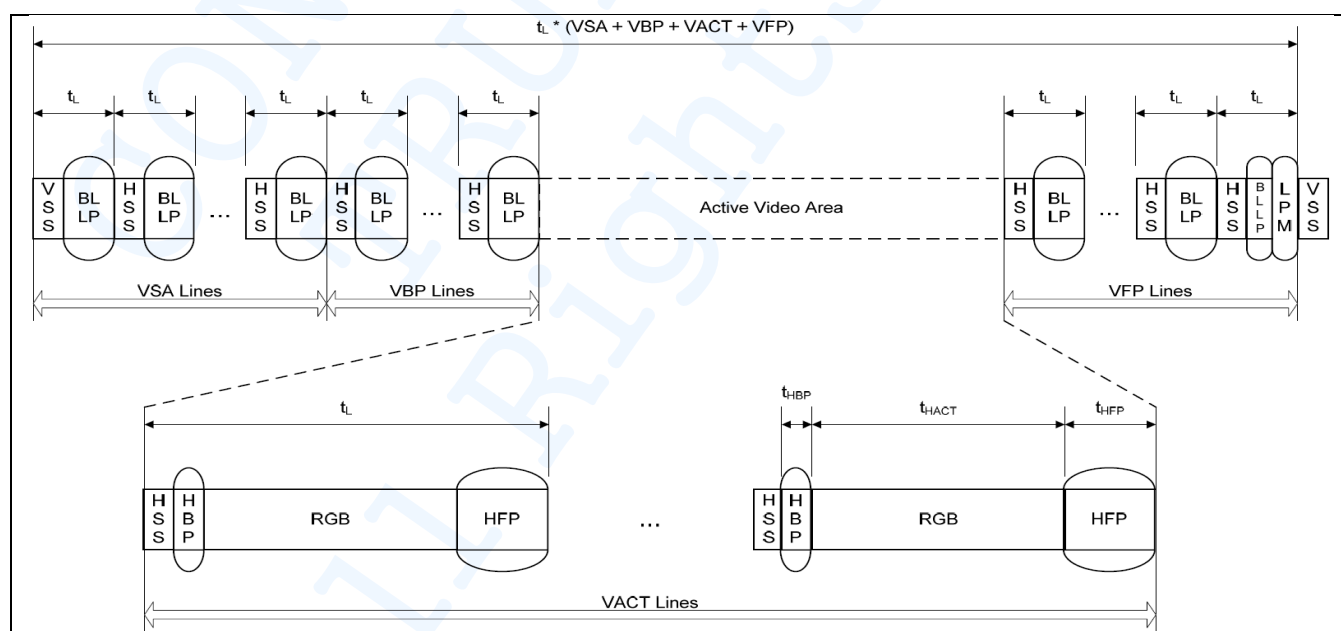


Figure 65 Non-Burst Transmission with Sync Events

4.10.5.9.3 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

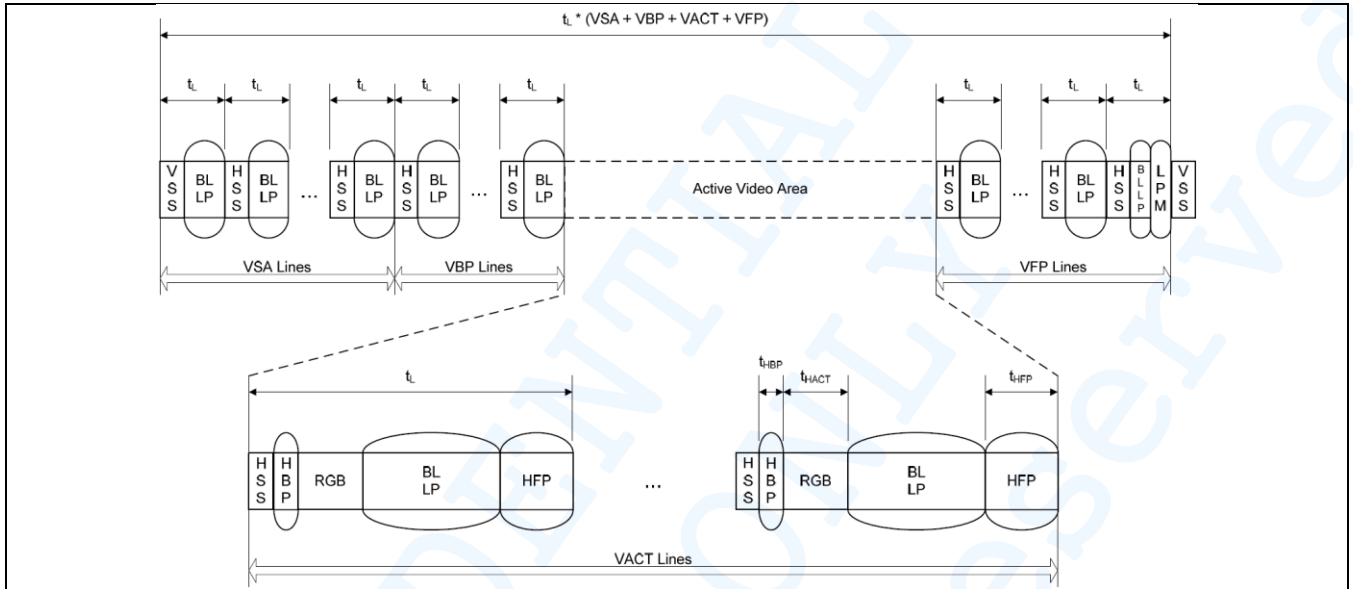


Figure 66 Burst Transmission

4.10.6 MIPI Interface Timing on Video Mode

SH8501A video mode operates as RGB interface.

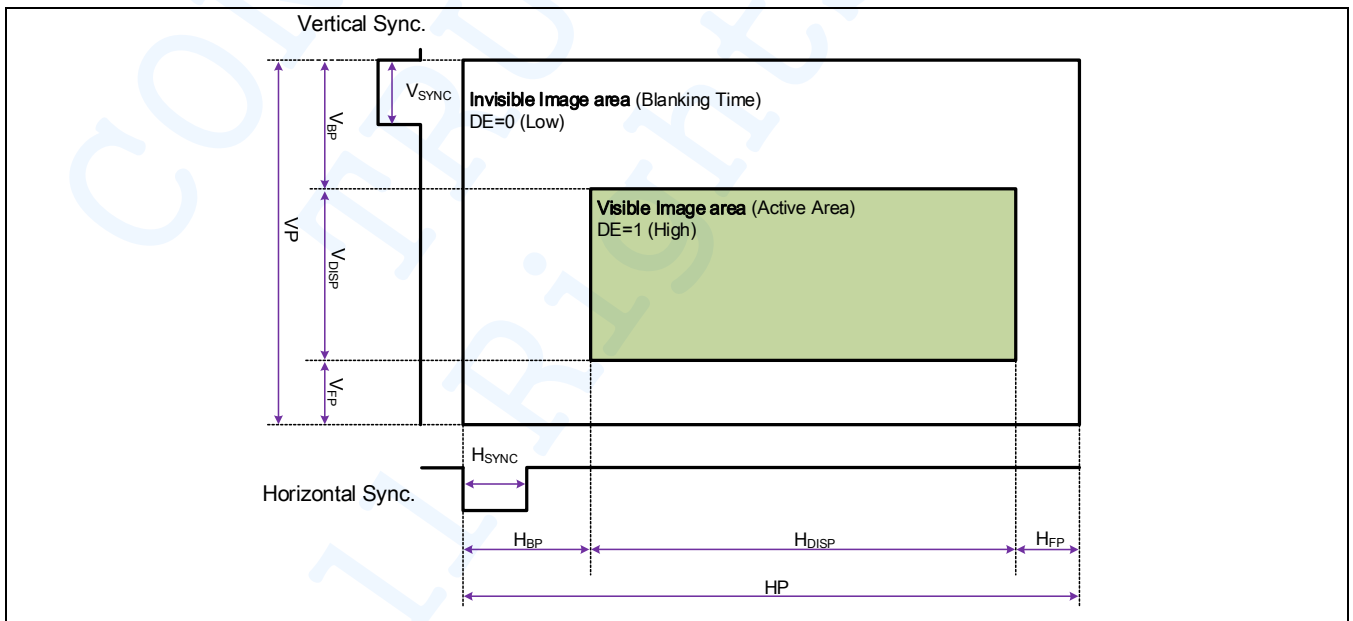


Figure 67 Display Timing (Video Mode)

4.10.6.1 Vertical Display Timing

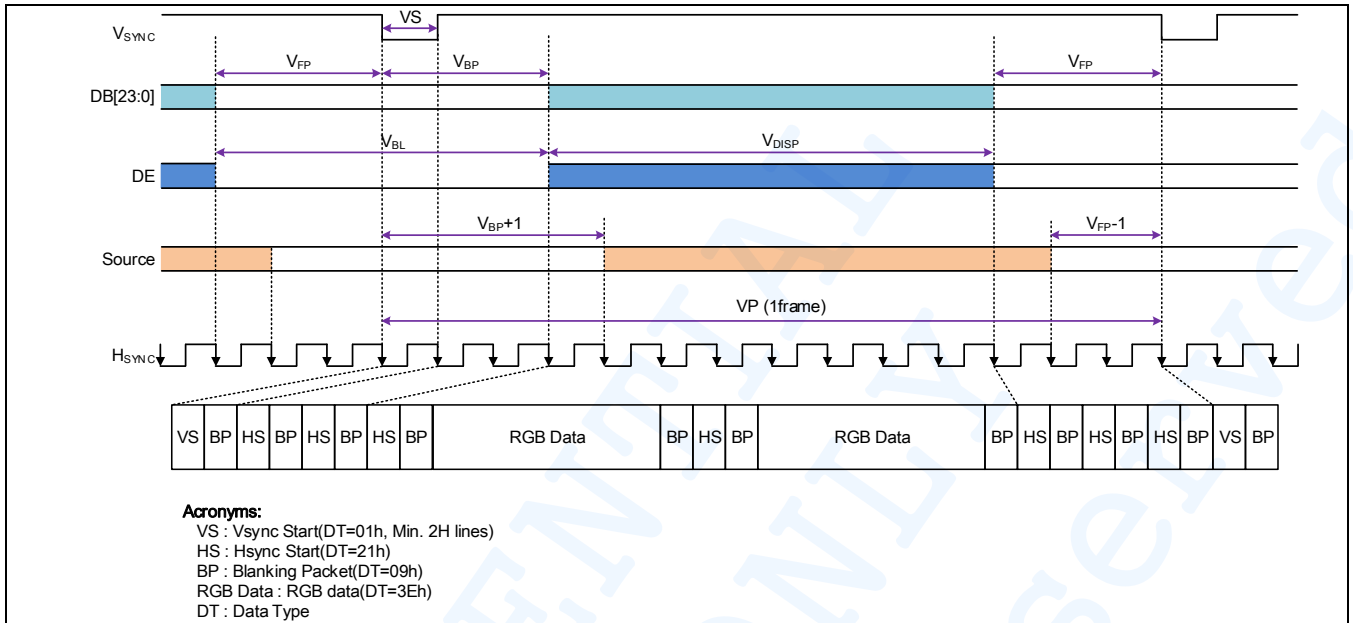


Figure 68 Vertical Display Timing

Table 36 Vertical Timing for Video Mode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Vertical cycle	VP	—	-	256	-	line	(1)
Vertical low pulse width	VS	—	1	2	2		(1) (2) (3)
Vertical front porch	VFP	—	6	8	-		(1) (3)
Vertical back porch	VBP	—	6	8	255		(1) (2) (3)
Vertical blanking period	VBL	VBP + VFP	12	16	-		(1) (3)
Vertical active area	—	VDISP	-	240	-		
(Vertical refresh area)	(VRR)	—	-	60	-	Hz	

NOTE:

1. Typical values are for resolution of 240 x 240 application.
2. VBP are set as back porch by B1h NOR_VBP/VFP[11:0].
3. VS, VBP and VFP values are typical value.

4.10.6.2 Horizontal Display Timings

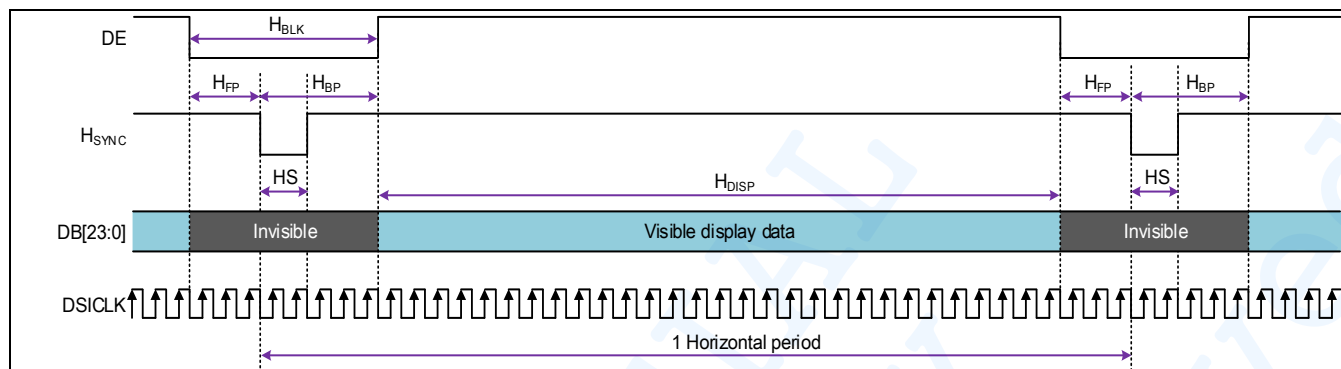


Figure 69 Horizontal Display Timing

Table 37 Horizontal Timings for Video Mode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
HS cycle	HP	—	-	272	-	PCLK	(2)
HS low pulse width	HS	—	1	2	2		(1) (2) (3)
Horizontal back porch	HBP	—	8	16	-		(3)
Horizontal front porch	HFP	—	8	16	-		(3)
Horizontal data start point	—	HBP	8	16	-		
Horizontal blanking period	HBLK	HBP + HFP	16	36	-		
Horizontal active area	HDISP	—	-	240	-		(1)

NOTE:

1. Typical values are for resolution of 240 x 240 application.
2. PCLK is pixel clock and same as byte-clock that is generated by dividing CLK by 4 (ex. 250 Mbps, 32ns).
3. HS, HBP and HFP values are typical value.

5 Command

5.1 List of User Command

Operational Code is abbreviated by Opcode, Read/Write/Command is abbreviated by RWC, and Number of Parameter bytes is abbreviated by Num. of Para.

Table 38 List of Level 1 Command

OpCode (Hex)	Function	R/W/C	Num. of Para.	Parameters
00	No Operation	C	-	NO operation
01	Software Reset	C	-	-
04	Read Display Identification Information	R	3	ID1/2/3
05	Read Number of Errors on DSI	R	1	Number of the error on DSI
0A	Read Display Power Mode	R	1	Display power mode
0B	Read Display MADCTL	R	1	MX, BGR
0C	Read Display Pixel Format	R	1	Display COLMOD
0D	Read Display Image Mode	R	1	Display image mode
0E	Read Display Signal Mode	R	1	Display signal mode
0F	Read Display Self-Diagnostic Result	R	1	Display self-diagnostic result
10	Sleep In	C	-	-
11	Sleep Out	C	-	-
12	Partial Display On	C	-	-
13	Normal Display mode on	C	-	-
20	Inversion Off	C	-	-
21	Inversion On	C	-	-
22	All pixels off	C	-	-
23	All pixels on	C	-	-
28	Display off	C	-	-
29	Display on	C	-	-
2A	Column Address Set	RW	4	Start/End column address in memory write
2B	Page Address Set	RW	4	Start/End page address in memory write
2C	Memory Write Start	W	Variable	Memory write data
30	Partial Area Row Set	RW	4	Start/End row address in partial mode
31	Partial Area Column Set	RW	4	Start/End page address in partial mode

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OpCode (Hex)	Function	R/W/C	Num. of Para.	Parameters
34	Tearing effect off	C	-	-
35	Tearing effect on	WC	1	1 byte for tearing effect line mode selection.
36	Memory data access control	W	1	MX, BGR
38	Idle Mode Off	C	-	-
39	Idle Mode On	C	-	-
3A	Write Display Pixel Format	W	1	1byte for interface color selection
3C	Memory Write Continue	W	Variable	Memory write data
44	Write Tearing Effect Scan Line	W	2	2 byte for TE signal turns on when the display module reaches line N.
45	Read Scan Line Number	R	2	Scan line
46	SPI read Off	C	-	-
47	SPI read On	C	-	-
48	AOD Mode Off	C	-	-
49	AOD Mode On	C	-	-
4A	Write Display Brightness Value in AOD Mode	W	1	1 byte for display brightness value in AOD mode
4B	Read Display Brightness Value in AOD Mode	R	1	1 byte for display brightness value in AOD mode
4F	Deep Standby Mode On	W	1	1 byte for deep standby mode control
51	Write Display Brightness Value in Normal Mode	W	1	1 byte for display brightness value in normal mode
52	Read display brightness value in Normal Mode	R	1	1 byte for display brightness value in normal mode
53	Write CTRL Display1	W	1	1 byte for display control1
54	Read CTRL Display1	R	1	1 byte for display control1
55	Write CTRL Display2	W	1	1 byte for display control2
56	Read CTRL Display2	R	1	1 byte for display control2
58	Write CE	W	1	1 byte for CE control
59	Read CE	R	1	1 byte for CE control
63	Write Display Brightness Value in HBM Mode	W	1	1 byte for display brightness value in HBM mode
64	Read Display Brightness Value in HBM Mode	R	1	1 byte for display brightness value in HBM mode
65	Read HBM Control	R	1	1 byte for HBM control
66	Write HBM Control	W	1	1 byte for HBM control
70	Color Set 0	W	3	SPI 1-1-1 pixel format set0

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OpCode (Hex)	Function	R/W/C	Num. of Para.	Parameters
71	Color Set 1	W	3	SPI 1-1-1 pixel format set1
72	Color Set 3	W	3	SPI 1-1-1 pixel format set2
73	Color Set 3	W	3	SPI 1-1-1 pixel format set3
74	Color Set 4	W	3	SPI 1-1-1 pixel format set4
75	Color Set 5	W	3	SPI 1-1-1 pixel format set5
76	Color Set 6	W	3	SPI 1-1-1 pixel format set6
77	Color Set 7	W	3	SPI 1-1-1 pixel format set7
78	Color Set 8	W	3	SPI 1-1-1 pixel format set8
79	Color Set 9	W	3	SPI 1-1-1 pixel format set9
7A	Color Set 10	W	3	SPI 1-1-1 pixel format set10
7B	Color Set 11	W	3	SPI 1-1-1 pixel format set11
7C	Color Set 12	W	3	SPI 1-1-1 pixel format set12
7D	Color Set 13	W	3	SPI 1-1-1 pixel format set13
7E	Color Set 14	W	3	SPI 1-1-1 pixel format set14
7F	Color Set 15	W	3	SPI 1-1-1 pixel format set15
80	Color Option	W	1	SPI 1-1-1/256 pixel format option
A1	Read DDB start	R	8	8 byte for Read DDB start
A8	Read DDB Continue	R	8	8 byte for Read DDB continue
AA	Read First Checksum	R	1	Read Checksum
AF	Read continue Checksum	R	1	Read Checksum
C4	SPI mode control	W	1	1 byte for SPI mode control
DA	Read ID1	R	1	Read ID1
DB	Read ID2	R	1	Read ID2
DC	Read ID3	R	1	Read ID3

NOTE:

1. Undefined commands are treated as NOP (00H) command.
2. Commands 10H, 28H, 29H, 36H, 51H, 53H, 55H, 61H, 63H, and 66H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately.
Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh), Read Display Self-Diagnostic Result (0Fh), Read Display Brightness Value in normal mode(52h), Read CTRL Display1 (54h), Read CTRL Display2 (56h), Read Display Brightness Value in AOD Mode (4BH), Read Display Brightness Value in HBM Mode (64H) are updated immediately both in Sleep In mode and Sleep Out mode.
3. Parameters of the command are stored onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. This note is valid when a number of the parameters are equal or less than 32.

5.2 Description of User Command

5.2.1 NOP (00h): No Operation

00H	NOP (No Operation)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	0	00
Parameter	No Parameter									
Description	This command is an empty command. It does not have any effect on the display module.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					N/A				
	S/W Reset					N/A				
	H/W Reset					N/A				
Flow Chart	–									

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5.2.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	1	01
Parameter	No Parameter									
Description	When the software reset command is written, it causes a software reset. It resets the User, Manufacturer commands and parameters to their S/W Reset default values (See default tables in each command description.) and OTP is loaded. The display will be blanked. (The display will be blanked after first VSYNC, when Software Reset command is written in sleep out mode. The display remains the blank state in sleep in Mode.)									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5 msec. If software reset is applied during sleep out mode, it will be necessary to wait 60ms before sending sleep out command. Software reset command cannot be sent during sleep out sequence.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					N/A				
	S/W Reset					N/A				
	H/W Reset					N/A				
Flow Chart	SWRESET Display Whole Blank Screen Set Commands to S/W Default Value Sleep in Mode Legend Command Parameter Display Action Mode Sequential Transfer									

5.2.3 RDDIDIF (04h): Read Display Identification Information

04H	RDDIDIF (Read Display Identification Information)									
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	1	0	0	04
1st Para	Read	ID1[7:0]								00
2nd Para	Read	ID2[7:0]								00
3rd Para	Read	ID3[7:0]								00
Description	This command indicates the return value of 24-bit display identification information. ID1[7:0]: AMOLED module maker code (8-bit) ID2[7:0]: Driver IC and module version (8-bit) ID3[7:0]: Project code (8-bit) NOTE: Commands RDID1/2/3 (DAH, DBH, and DCH) reads data corresponding to the parameters 1, 2 and 3 of the command 04H, respectively.									
Restriction	There is one dummy clock before 1st parameter when using Serial interface.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00_00_00H		(OTP value)		
	S/W Reset					00_00_00H		(OTP value)		
	H/W Reset					00_00_00H		(OTP value)		
Flow Chart	RDDIDF(04h) Send 1st parameter Send 2nd parameter Send 3rd parameter Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.4 RDNUMED (05h): Read Number of the Errors on DSI

05H	RDNUMED (Read Number of the Errors on DSI)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	1	0	1	05
1 st Para	Read	NUMED[7:0]								00
Description	This command returns the number of corrupted packets previously received on the DSI link. The NUMED[7:0] bits are set to '0's (as well as RDDSM (0Eh)'s D0 is set to '0' at the same time) after the parameter information is sent, indicating that the read function is completed. NUMED[7] bits is set to '1' if there is overflow with the NUMED[6:0] bits. NUMED[6:0] bits indicates a number of errors.									
Restriction	After the RESX goes high from low, all lanes should be "High". If all lanes are not high, DSI errors may occur and this parameter may not be all zero. The errors only include ECC 1BIT ERROR, ECC MULTIBIT ERROR and CHECKSUM ERROR. If you want specific description of ECC and CHECKSUM ERROR, refer to MIPI DSI document.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	SW Reset					00h				
	H/W Reset					00h				
Flow Chart	Read Number Of the Errors on DSI Host ↓ P[7...0] = 00h RDDSM(0Eh)'s D0=0 Display Legend Command Parameter Display Action Mode Sequential Transfer									

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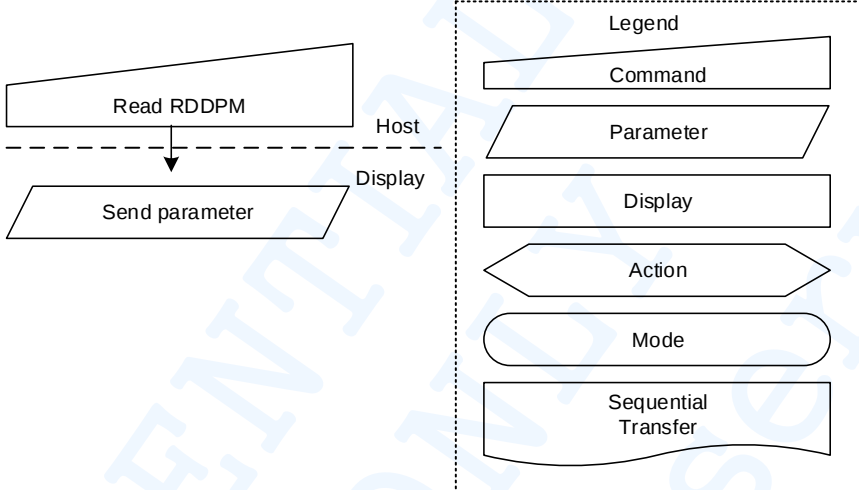
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5.2.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)										
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	0	0	0	0	1	0	1	0	0A	
Parameter	Read	BSTO N	IDMON	PTLON	SLPOU T	NOR ON	DISP ON	0	0	08	
Description	This command indicates the current status of the display as described in the table below:										
	Bit	Description					Remark				
	D7	Booster Voltage Status					-				
	D6	Idle Mode On/Off					-				
	D5	Partial Display Mode On/Off					-				
	D4	Sleep In/Out					-				
	D3	Display Normal Mode On/Off					-				
	D2	Display On/Off					-				
	D1	Reserved					Set to "0"				
	D0	Reserved					Set to "0"				
	• BSTON - Booster Voltage Status 0 = Booster off or has a fault 1 = Booster on and working good • IDMON - Idle Mode On/Off 0 = Idle mode off 1 = Ide mode on • PTLON - Partial Display Mode On/Off 0 = partial display off 1 = partial display on • SLPOUT - This bit is updated immediately after Sleep In (10h) / Sleep Out (11h) command is written. 0 = Sleep in mode 1 = Sleep out mode • NORON - Normal Display Mode On 0 = Normal display off 1 = Normal display on • DISPON - This bit is updated immediately after Display On (29h) / Off (28h) command is written. 0 = Display is off 1 = Display is on • D[1] - Reserved This bit is not applicable for this project, so it is set to "0". • D[0] - Reserved This bit is not applicable for this project, so it is set to "0".										
	Restriction	–									
	Register Availability	Status					Availability				
		Sleep Out					Yes				
		Sleep In					Yes				

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Default	Status	Default Value
	Power On Sequence	08h
	S/W Reset	08h
	H/W Reset	08h
Flow Chart	 Legend - Command - Parameter - Display - Action - Mode - Sequential Transfer	

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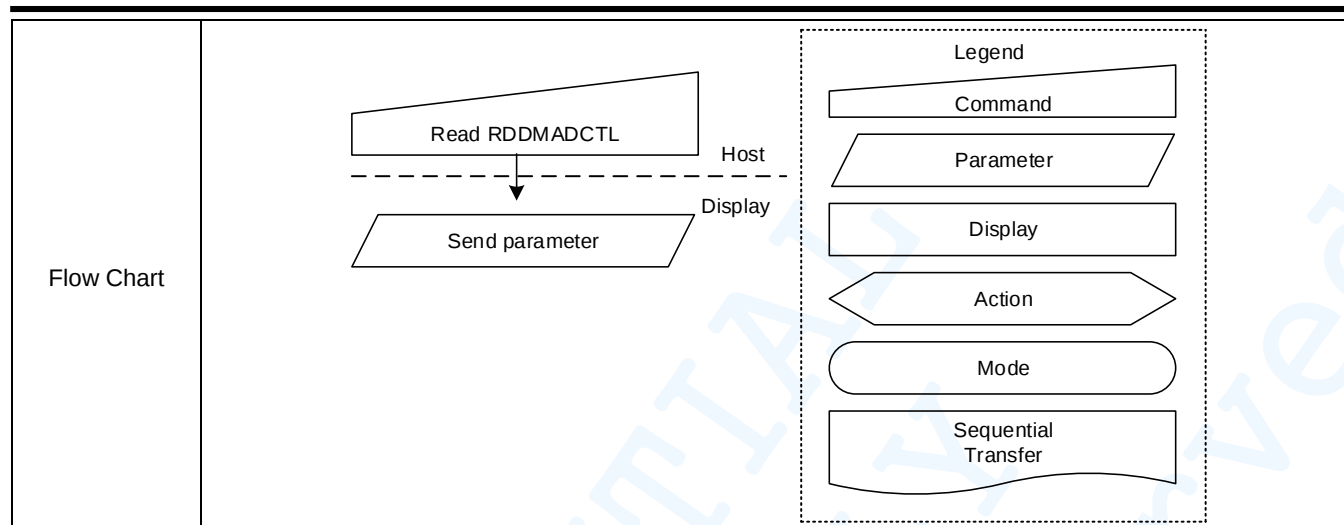
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5.2.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	0	1	1	0B
Parameter	Read	0	MX	0	0	BGR	0	0	0	00
Description	This command indicates the current status of the display as described in the table below:									
	Bit	Description					Remark			
	D7	Reserved					Set to "0"			
	D6	Memory Write Direction Horizontal Flip					-			
	D5	Reserved					Set to "0"			
	D4	Reserved					Set to "0"			
	D3	RGB/BGR Order					–			
	D2	Reserved					Set to "0"			
	D1	Reserved					Set to "0"			
	D0	Reserved					Set to "0"			
	• MX - Memory Write Direction Horizontal Flip 0 = Memory write forward direction 1 = Memory write reverse direction • D[5:4] - Reserved These bits are not applicable for this project, so it is set to "0". • BGR - RGB/BGR Order 0 = RGB (When MADCTL D3 = "0") 1 = BGR (When MADCTL D3 = "1")									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				

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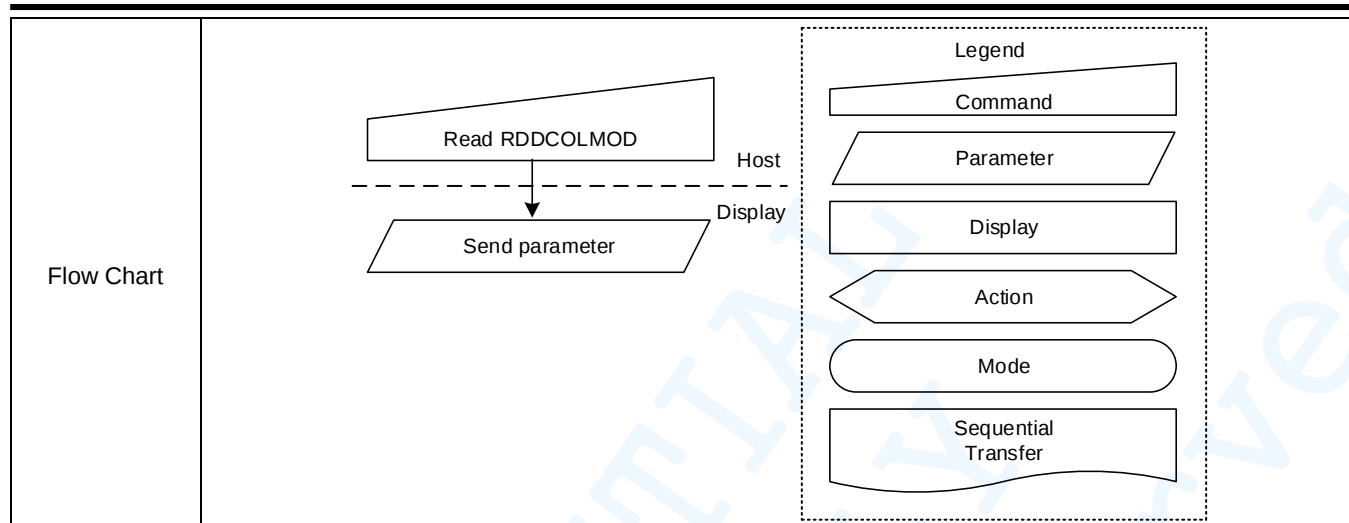
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5.2.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)										
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	0	0	0	0	1	1	0	0	0C	
Parameter	Read	SPI_P F_SEL	VIPF[2:0]			0	IFPF[2:0]			77	
Description	This command indicates the current status of the display as described in the table below: • SPI_PF_SEL – SPI Pixel Format Selection. • VIPF[2:0] – Pixel Format Definition. • D[3] - Reserved This bit is not applicable for this project, so it is set to "0". • IFPF[2:0] - Pixel Format Definition. Refer to section : COLMOD(3Ah) : Control Interface Pixel Format										
	Control Interface Color Format					IFPF[2]		IFPF[1]		IFPF[0]	
	24-bit/pixel(16.7M Color)					1		1		1	
	18-bit/pixel(262K Color)					1		1		0	
	16-bit/pixel(65K Color)					1		0		1	
	Setting Disable					1		0		0	
	3-bit/pixel(8 Color)					0		1		1	
	8-bit/pixel(256 Color, 3-3-2)					0		1		0	
	8-bit/pixel(256 Gray)					0		0		1	
	Setting Disable					0		0		0	
Restriction	–										
Register Availability	Status					Availability					
	Sleep Out					Yes					
	Sleep In					Yes					
Default	Status					Default Value					
	Power On Sequence					77h					
	S/W Reset					77h					
	H/W Reset					77h					

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5.2.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	0	1	0D
Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00
Description	This command indicates the current status of the display as described in the table below: • D[7:6] - Reserved These bits are not applicable for this project, so it is set to "0". • INVON - Display Inversion On/Off 0 = Display inversion Off 1 = Display inversion On • ALLPON - All Pixel On/Off 0 = Normal display 1 = All pixel is on • ALLPOFF - All Pixel Off/On 0 = Normal display 1 = All pixel is off • D[2:0] - Reserved These bits are not applicable for this project, so it is set to "0".									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	Read RDDIM Host Send parameter Display Legend Command Parameter Display Action Mode Sequential Transfer									

5.2.9 RDDSM (0EH): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	1	0	0E
Parameter	Read	TEON	TEM	0	0	0	0	0	DSIE	00
Description	This command indicates the current status of the display as described below: • TEON - This bit is updated immediately after Tearing Effect On (35h) / Off (34h) command is written. 0 = Tearing effect off 1 = Tearing effect on • TEM - This bit is updated immediately after Tearing Effect On (35h) command is written. Refer to section TEON: Tearing Effect On (35H). 0 = Mode 1. 1 = Mode 2. • D[5:1] - Reserved These bits are not applicable for this project, so it is set to "0". • DSIE - Error on DSI, refer to section RDNUMED(05h) : Read Number of the Errors on DSI. If you want specific description of ECC and CHECKSUM ERROR, refer to MIPI DSI document. This bit is only for MIPI interface. In other interface, D0 is set to "0". 0 = No Error 1 = Error									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	Read RDDSM ↓ Send parameter Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	1	1	0F
Parameter	Read	RLDT	FNDT	0	0	0	0	0	CHKS UM_E RR	00
Description	This command indicates the status of the display self-diagnostic results after Sleep Out-command as described in the table below: • RLDT - Register Loading Detection. Refer to section “Register Loading Detection” • FNDT - Functionality Detection Refer to section” Functionality Detection” • D[5:1] - Reserved. These bits are not applicable for this project, so it is set to "0". • CHKSUM_ERR – Checksum Error Detection.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	Read RDDSDR ↓ Send parameter Host ----- Display Legend Command Parameter Display Action Mode Sequential Transfer									

5.2.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	0	10
Parameter	No Parameter									
Description	This command causes the display module to enter the minimum power consumption mode. In this mode, the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.									
Restriction	This command has no effect when module is already in Sleep In mode. Sleep In mode can only be left by the Sleep Out command (11h). It will be necessary to wait 5ms before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 60ms after sending Sleep Out command (when in Sleep In mode) before Sleep In command can be sent.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Sleep In Mode				
	S/W Reset					Sleep In Mode				
	H/W Reset					Sleep In Mode				
Flow Chart	It takes about 60ms before it goes into Sleep-in Mode (Booster off state) after SLPIN command. SLPIN Display whole blank screen (Automatic No effect to DISPON/DISPOFF commands) Drain Charge From Display Panel Stop : DCDC Converter Stop : Internal Oscillator Sleep In Mode Legend Command Parameter Display Action Mode Sequential Transfer									

NOTE: Refer to customer appendix for SLPIN sequence

5.2.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	1	11
Parameter	No Parameter									
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.									
Restriction	This command shall not cause any visible effect on the display module when the module is already in Sleep Out mode. Sleep Out Mode can only be left by the Sleep In command (10h) This host processor must wait 5msec after sending this command before sending other command. The display module loads all display supplier's factory default values from internal OTP to the registers during this 5msec. Also the host processor must wait 60msec after sending a Sleep Out command before sending a Sleep In command to avoid abnormal Sleep In status. This delay time allows the internal power circuits and clock circuits to stabilize.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Sleep In Mode				
	S/W Reset					Sleep In Mode				
	H/W Reset					Sleep In Mode				
Flow Chart	SLPOUT Start Internal Oscillator Start DCDC Converter Charge Offset Voltage for Display Panel Display whole blank screen for 2 frames(Automatic No effect to DISPON/DISPOFF commands) Display Memory Contents in Accordance with the Current Command Table Settings Sleep Out Mode Legend Command Parameter Display Action Mode Sequential Transfer It takes 60ms to become Sleep Out mode after SLPOUT command issued.									

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5.2.13 PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	1	0	12
Parameter	No Parameter									
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the PTLAR(30h)/PTLAC(31h). To leave the Partial Display Mode, NORON(13h) command should be used.									
Restriction	This command has no effect when partial display mode is already active.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Normal Display On				
	SW Reset					Normal Display On				
	H/W Reset					Normal Display On				
Flow Chart	Normal Display Mode ↓ PTLON(12h) ↓ Partial Display Mode Legend Command Parameter Display Action Mode Sequential Transfer									

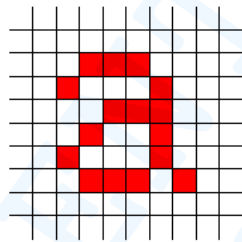
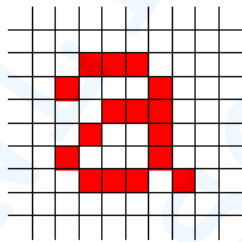
5.2.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	1	1	13
Parameter	No Parameter									
Description	This command returns the display to normal mode. Normal display mode on means All Pixel Off(22h), All Pixel On(23h) and Partial mode(12h) are off.									
Restriction	This command has no effect if Normal Display mode is active.									
Register Availability	Status				Availability					
	Sleep Out				Yes (Reflect in the next V-sync period).					
	Sleep In				Yes					
Default	Status				Default Value					
	Power On Sequence				Normal Display Mode On					
	S/W Reset				Normal Display Mode On					
	H/W Reset				Normal Display Mode On					
Flow Chart	Not Normal Display Mode NORON(13h) Normal Display Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.15 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	0	20
Parameter	No Parameter									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. Example) Memory  → Display Panel 									
Restriction	This command has no effect if Normal Display mode is active.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Display Inversion Off				
	S/W Reset					Display Inversion Off				
	H/W Reset					Display Inversion Off				
Flow Chart	Display Inversion On Mode ↓ INVOFF(20h) ↓ Display Inversion OFF Mode Legend Command Parameter Display Action Mode Sequential Transfer									

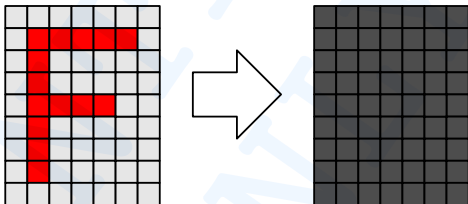
5.2.16 INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	1	21
Parameter	No Parameter									
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. Example) Memory									

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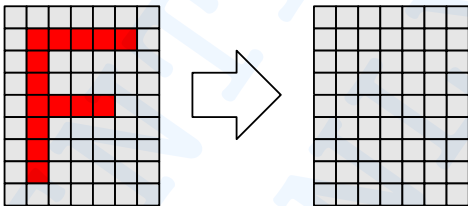
5.2.17 ALLPOFF (22h): All Pixel Off

22H	ALLPOFF (All Pixel Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	0	22
Parameter	No Parameter									
Description	This command turns the display panel black in sleep out mode. It also turns on/off the status of the DISPON/DISPOFF register. This command does not change the content of frame memory or any other status. Memory (Example) Display  'All Pixel On'(23h) or 'Normal Display'(13h) commands are used to leave this mode. The display panel shows the display content from Host after 'Normal Display' command.									
Restriction	This command has no effect if module is already in all pixels off mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Normal Display Mode On				
	S/W Reset					Normal Display Mode On				
	H/W Reset					Normal Display Mode On				
Flow Chart	Normal Display Mode ↓ ALLPOFF(22h) ↓ Black Display Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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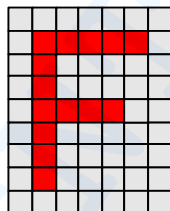
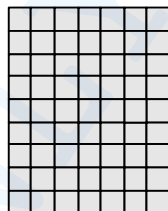
5.2.18 ALLPON (23h): All Pixel On

23H	ALLPON (All Pixel On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	1	23
Parameter	No Parameter									
Description	This command turns the display panel white in sleep out mode. It also turns on/ off the status of the DISPON/DISPOFF register. This command does not change the content of frame memory or any other status. Memory (Example) Display  ‘All Pixel Off’(22h), ‘Normal Display’(13h) commands are used to leave this mode. The display panel shows the display content after ‘Normal Display’ command.									
Restriction	This command has no effect If the module is already in all pixels on mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Normal Display Mode On				
	SW Reset					Normal Display Mode On				
	H/W Reset					Normal Display Mode On				
Flow Chart	Normal Display Mode ↓ ALLPON(23h) ↓ White Display Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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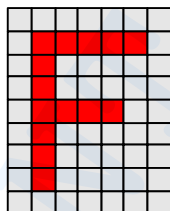
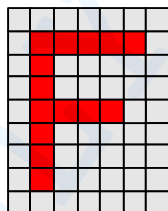
5.2.19 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)									
—	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	0	28
Parameter	No Parameter									
Description	This command is used to enter into Display Off mode. This command does not change any other status except bit D2 of RDDPM command (0Ah). There will be no abnormal visible effect on the display (Example) Host  → Display 									
Restriction	This command has no effect when module is already in display off mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Display Off				
	S/W Reset					Display Off				
	H/W Reset					Display Off				
Flow Chart	Display On Mode ↓ DISPOFF(28h) ↓ Display Off Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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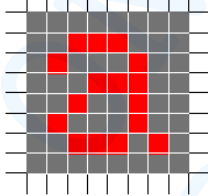
5.2.20 DISPON (29h): Display On

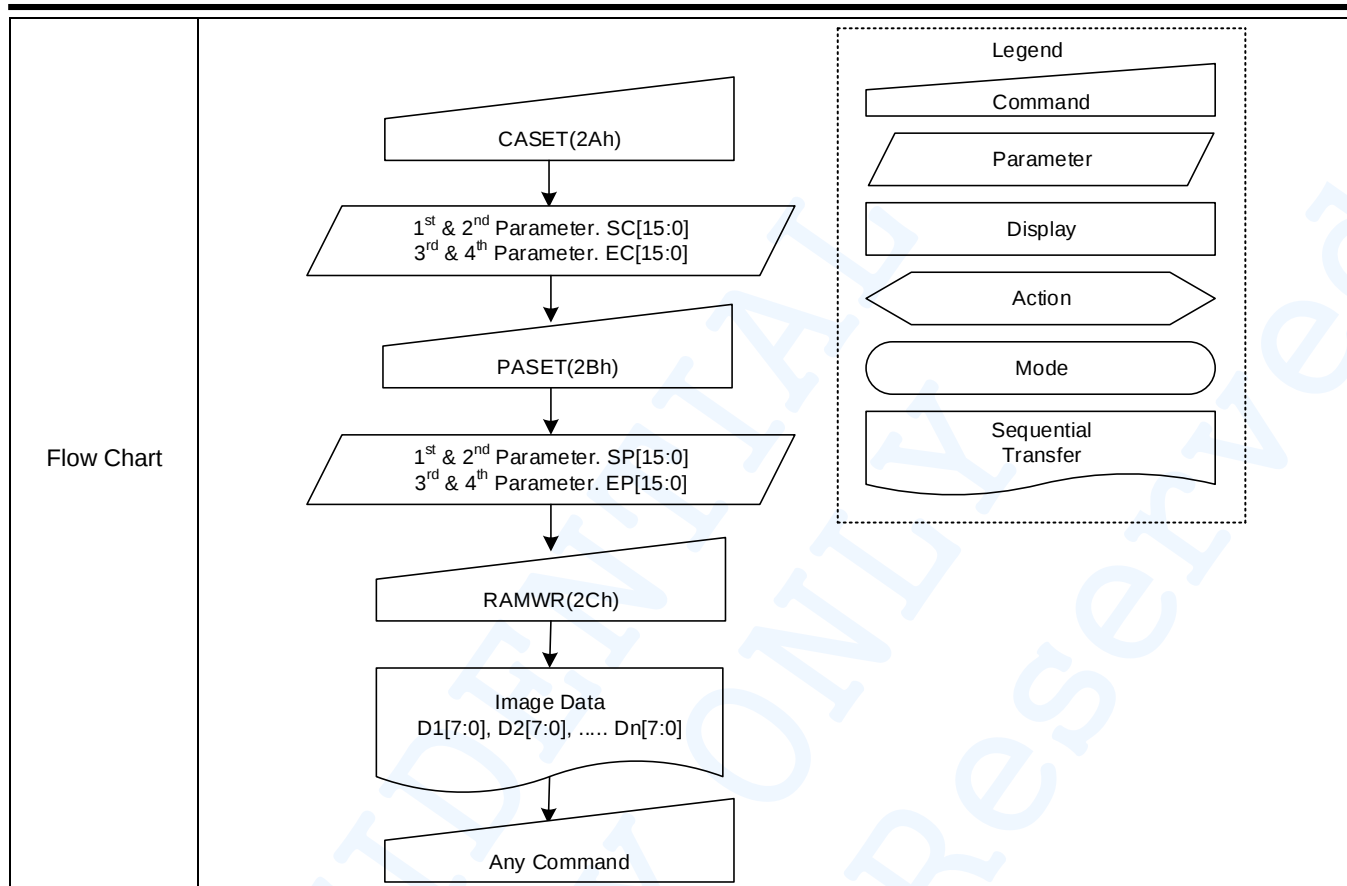
29H	DISPON (Display On)									
—	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	1	29
Parameter	No Parameter									
Description	This command is used to recover from Display Off Mode. This command does not change any other status except bit D2 of RDDPM command (0Ah). (Example) Host  Display 									
Restriction	This command has no effect when module is already in display on mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Display Off				
	S/W Reset					Display Off				
	H/W Reset					Display Off				
Flow Chart	Display Off Mode ↓ DISPON(29h) ↓ Display On Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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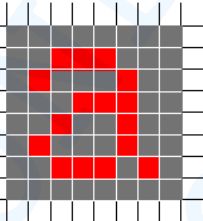
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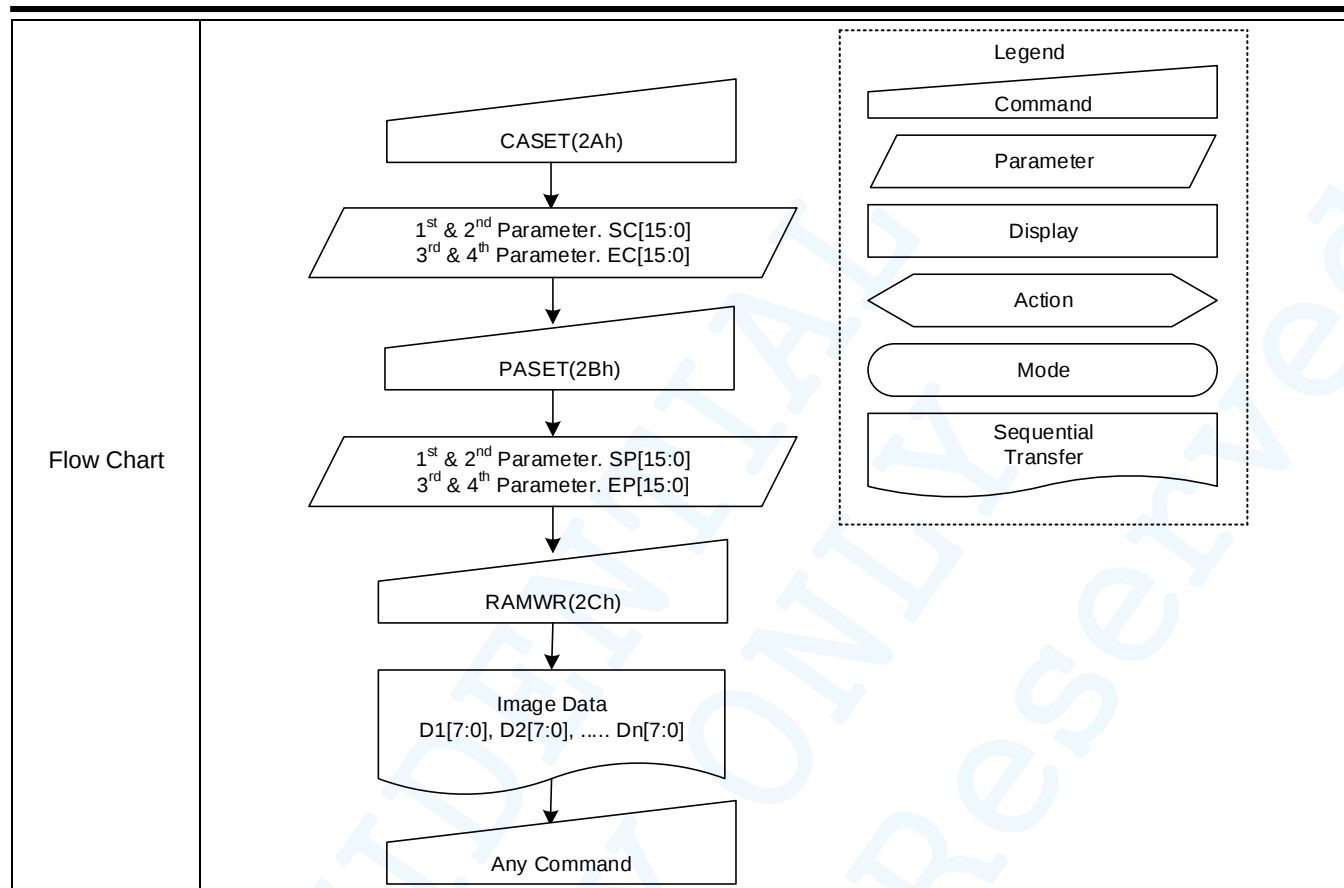
5.2.21 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	1	0	2A
1st Para	RW	SC[15:8]								00
2nd Para	RW	SC[7:0]								00
3rd Para	RW	EC[15:8]								00
4th Para	RW	EC[7:0]								EF
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. Each value represents on column line in the frame memory. Example) SC[15:0] EC[15:0]  ● SC[15:0]: Start of Column ● EC[15:0] : End of Column									
Restriction	SC[15:0] must always be less than EC[15:0] If transferred image size is bigger than setting window size, abnormal display is occurred. So transferred image size should be same as setting window size. The SC[15:0] and EC[15:0]-SC[15:0]+1 must be divisible by 4. In the SPI3W/SPI4W mode, set SPI_RDON(R47h)/SPI_RDOFF(R46h) to read CASET value..									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
						SC[15:0]		EC[15:0]		
	Power On Sequence					00_00h		00_EFh		
	S/W Reset					00_00h		00_EFh		
	H/W Reset					00_00h		00_EFh		



5.2.22 PASET (2Bh): Page Address Set

2BH	PASET (Page Address Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	1	1	2B
1st Para	RW	SP[15:8]								00
2nd Para	RW	SP[7:0]								00
3rd Para	RW	EP[15:8]								01
4th Para	RW	EP[7:0]								3F
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. Each value represents on page line in the frame memory. Example) SP[15:0]  EP[15:0] ● SP[15:0]: Start of Page ● EP[15:0] : End of Page									
Restriction	SP[15:0] must always be less than EP[15:0] If SP[15:0] or EP[15:0] is greater than the available frame memory, then the parameter is not updated. In the SPI3W/SPI4W mode, set SPI_RDON(R47h)/SPI_RDOFF(R46h) to read PASET value..									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
						SP[15:0]		EP[15:0]		
	Power On Sequence					00_00h		01_3Fh		
	S/W Reset					00_00h		01_3Fh		
	H/W Reset					00_00h		01_3Fh		



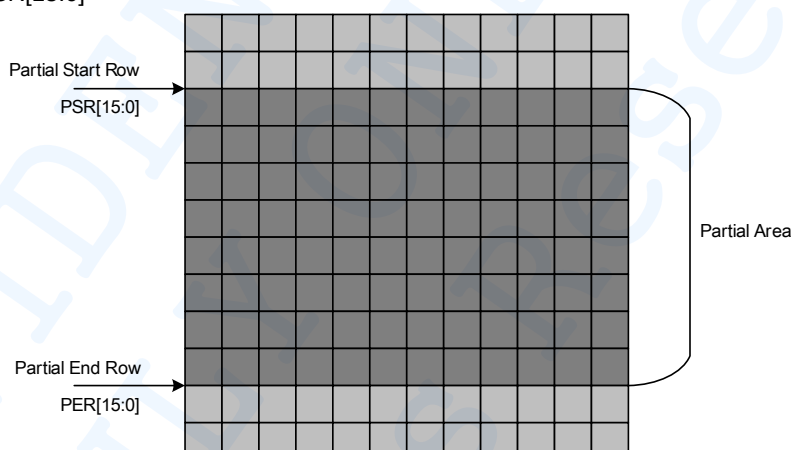
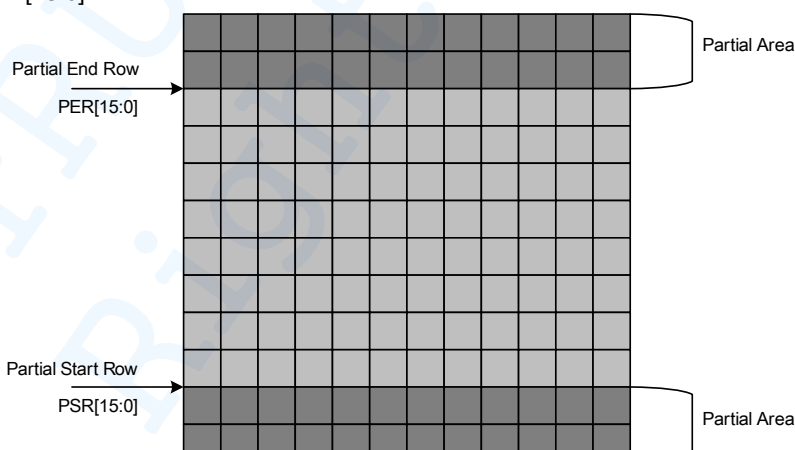
5.2.23 RAMWR (2Ch): Memory Write Start

2CH	RAMWR (Memory Write Start)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	1	0	0	2C
1st Para	Write	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	00
2nd Para	Write	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	00
...										
Nth Para	Write	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to (“0000”/”0000”). Then Dn[7:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame write.									
Restriction	There is no restriction on length of parameters. No access in the frame memory in sleep in mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Contents of memory is set randomly				
	S/W Reset					Contents of memory is set randomly				
	H/W Reset					Contents of memory is set randomly				
Flow Chart	MEMWR(2Ch) Image Data D1[7:0], D2[7:0], Dn[7:0] Next Command Legend Command Parameter Display Action Mode Sequential Transfer									

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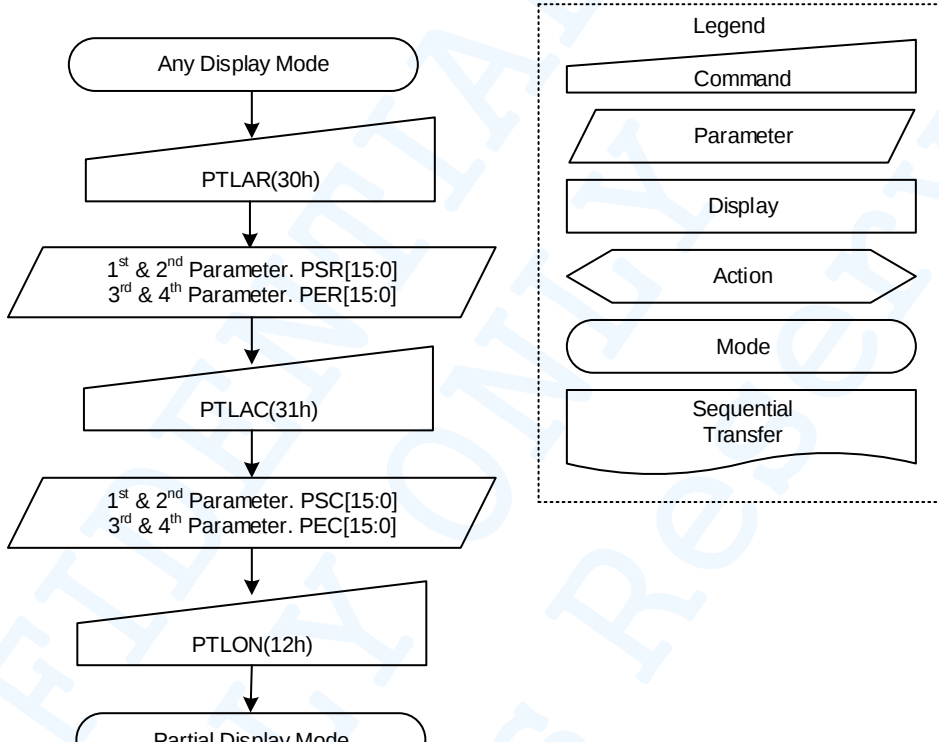
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5.2.24 PTLAR (30h): Partial Area Row Set

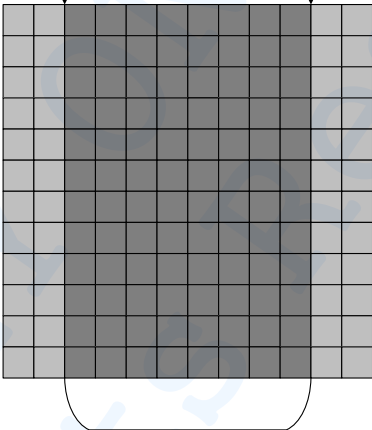
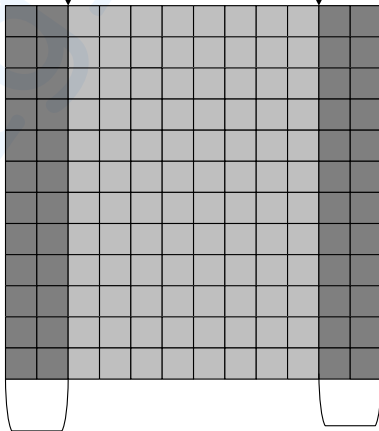
30H	PTLAR (Partial Area Row Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	0	0	0	30
1st Para	RW	PSR[15:8]								00
2nd Para	RW	PSR[7:0]								00
3rd Para	RW	PER[15:8]								01
4th Para	RW	PER[7:0]								3F
Description	This command defines the partial display mode's display area. There are two parameters associated with this command, the first defines the partial start row(PSR) and the second the partial end row(PER). As illustrated in the figures below. PSR[15:0] and PER[15:0] refer to the Frame Memory Line Pointer. Example) If PER[15:0] > PSR[15:0] 									
	If PSR[15:0] > PER[15:0] 									
	Restriction PSR[15:0] and PER[15:0] cannot be 0000h nor exceed the last vertical line number. In the SPI3W/SPI4W mode, set SPI_RDON(R47h)/SPI_RDOFF(R46h) to read PTLAR value..									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in the next V-sync period).				

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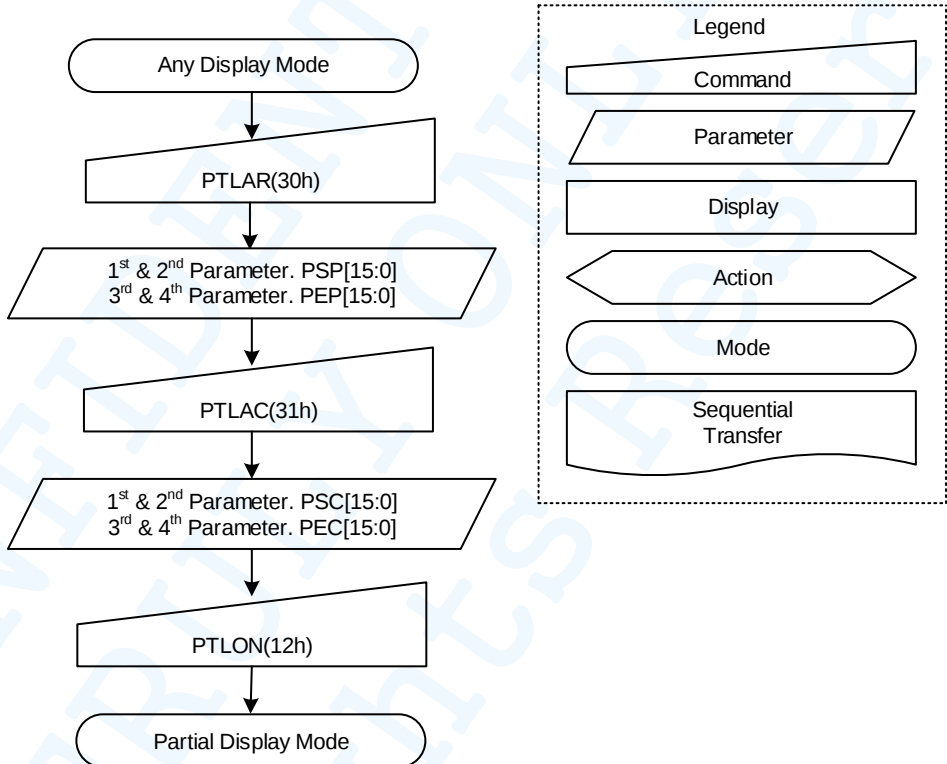
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00_00h / 01_3Fh
	S/W Reset	00_00h / 01_3Fh
	H/W Reset	00_00h / 01_3Fh
Flow Chart		

5.2.25 PTLAC (31h): Partial Area Column Set

31H	PTLAC (Partial Area Column Set)									
—	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	0	0	1	31
1st Para	RW	PSC[15:8]								00
2nd Para	RW	PSC[7:0]								00
3rd Para	RW	PEC[15:8]								00
4th Para	RW	PEC[7:0]								EF
Description	This command defines the partial display mode's display area. There are two parameters associated with this command, the first defines the partial start column(PSC) and the second the partial end column(PEC). As illustrated in the figures below. PSC[15:0] and PEC[15:0] refer to the Frame Memory Line Pointer. Example) If PEC[15:0] > PSC[15:0] Partial Start Column PSC[15:0] Partial End Column PEC[15:0]  If PSC[15:0] > PEC[15:0] Partial End Column PEC[15:0] Partial Start Column PSC[15:0] 									

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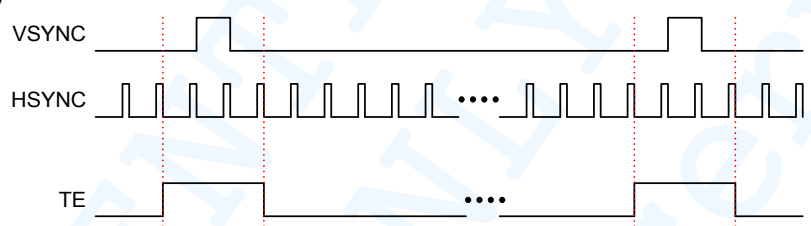
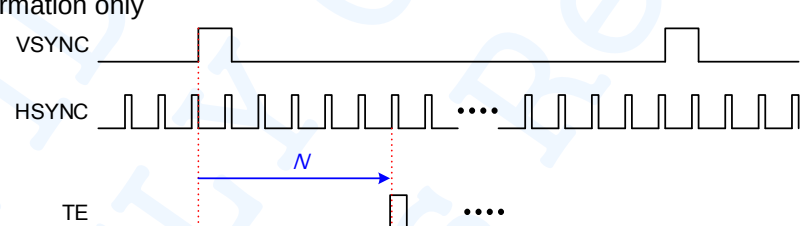
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Restriction	PSC[15:0] and PEC[15:0] cannot be 0000h nor exceed the last pixel number. The setting of PSC[15:0] and PEC[15:0] must be a multiple of 4. In the SPI3W/SPI4W mode, set SPI_RDON(R47h)/SPI_RDOFF(R46h) to read PTLAC value..	
Register Availability	Status	Availability
	Sleep Out	Yes (Reflect in the next V-sync period).
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00_00h / 00_EFh
	SW Reset	00_00h / 00_EFh
	H/W Reset	00_00h / 00_EFh
Flow Chart	 <pre> graph TD A([Any Display Mode]) --> B[/PTLAR(30h)/] B --> C[/1st & 2nd Parameter. PSP[15:0] 3rd & 4th Parameter. PEP[15:0]/] C --> D[/PTLAC(31h)/] D --> E[/1st & 2nd Parameter. PSC[15:0] 3rd & 4th Parameter. PEC[15:0]/] E --> F[/PTLON(12h)/] F --> G([Partial Display Mode]) </pre> Legend - Command: / / - Parameter: / / - Display: [] - Action: > < - Mode: () - Sequential Transfer: []	

5.2.26 TEOFF (34h): Tearing Effect Off

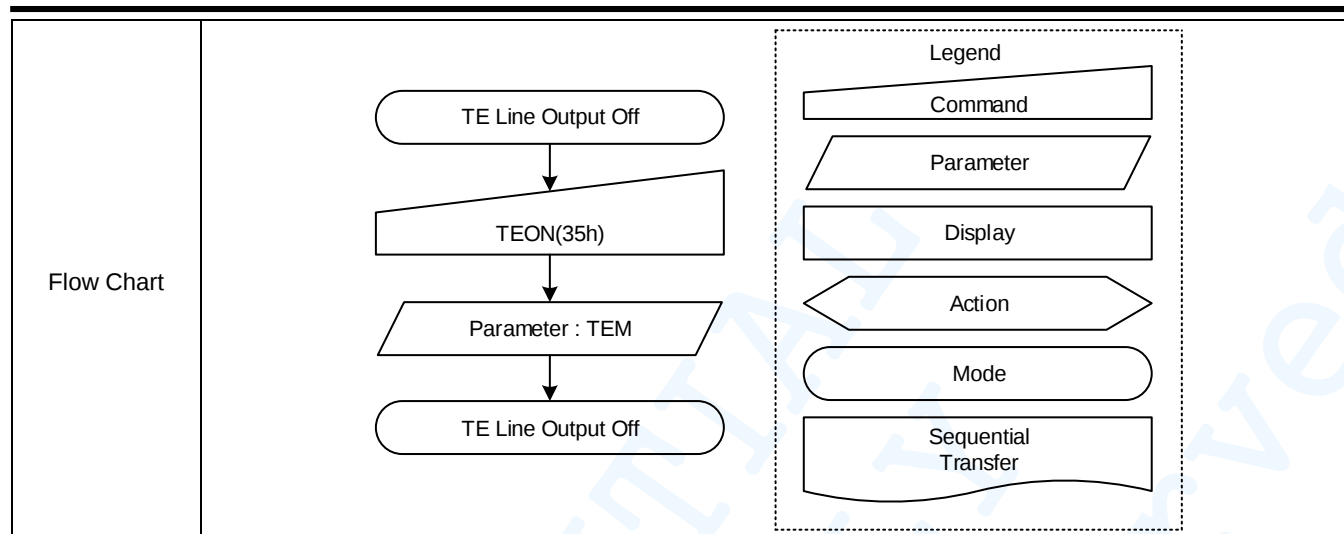
34H	TEOFF (Tearing Effect Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	0	0	34
Parameter	No Parameter									
Description	This command is used to turn off (Active Low) the Tearing Effect output signal from TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart	TE Line Output On ↓ TEOFF(34h) ↓ TE Line Output Off Legend Command Parameter Display Action Mode Sequential Transfer									

5.2.27 TEON (35h): Tearing Effect On

35H	TEON (Tearing Effect On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	0	1	35
1st Para	Write	0	0	0	0	0	0	0	TEM	00
Description	This command is used to turn on the Tearing Effect output signal from the TE signal line. The TEON has one parameter that describes the mode of the Tearing Effect Output Line.									
	When TEM = 0 & TE_SCANLINE (in TESCAN, 44h) = 0: TE Output line consists of V-Blanking information only									
										
	When TEM = 0 & TE_SCANLINE (in TESCAN, 44h) = N (N≠0): TE Output line consists of one H-Blanking information only									
Description										
	When TEM = 1: TE Output line consists of one V-Blanking and H-Blanking information									
										
	NOTE: NOTE: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.									
Restriction	This command has no effect when Tearing Effect output is already On. For enabling Tearing Effect Bus Trigger information, parameter TEM should be "0".									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Tearing effect off & TEM = "0"				
	S/W Reset					Tearing effect off & TEM = "0"				
	H/W Reset					Tearing effect off & TEM = "0"				

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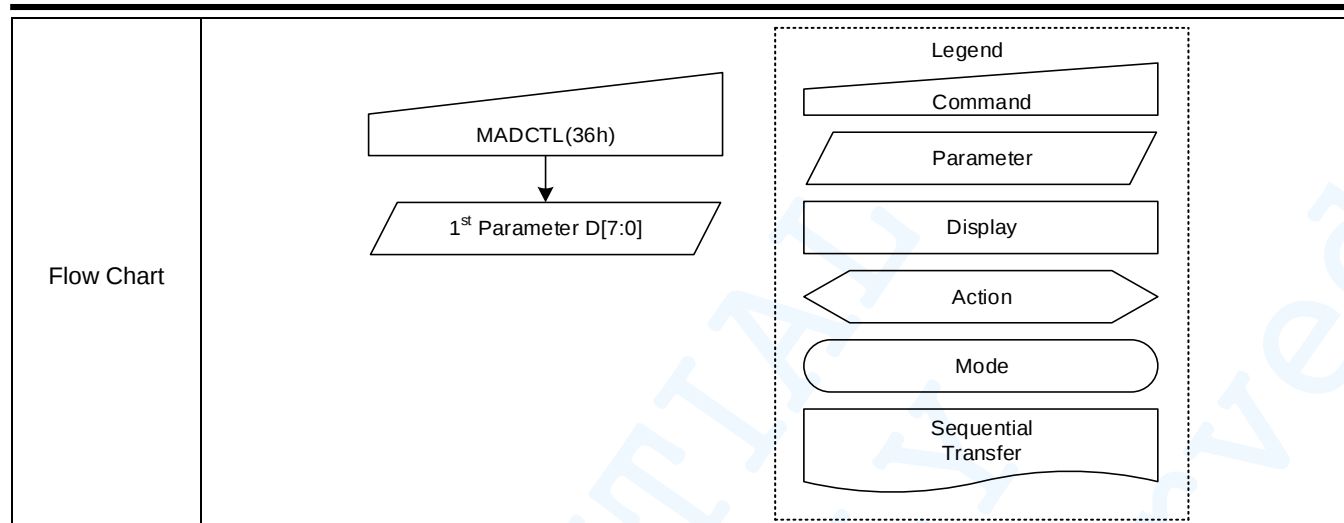


5.2.28 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)										
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	0	0	1	1	0	1	1	0	36	
Parameter	Write	0	MX	0	0	BGR	0	0	0	00	
Description	This command indicates the current status of the display as described in the table below										
	Bit	Description				Remark					
	D7	Reserved				Set to "0"					
	D6	Memory Write Direction Horizontal Flip				-					
	D5	Reserved				Set to "0"					
	D4	Reserved				Set to "0"					
	D3	RGB/BGR Order				–					
	D2	Reserved				Set to "0"					
	D1	Reserved				Set to "0"					
	D0	Reserved				Set to "0"					
	• MX - Memory Write Direction Horizontal Flip 0 = Memory write forward direction 1 = Memory write reverse direction • D[5:4] - Reserved These bits are not applicable for this project, sot it is set to "0". • BGR - RGB/BGR Order 0 = RGB Order 1 = BGR Order • D[7], D[5:4], D[2:0] - Reserved These bits are not applicable for this project, so it is set to "0".										
	Restriction	–									
	Register Availability	Status				Availability					
Sleep Out				D[3] : Yes (Reflect in next V-sync period)							
Sleep In				Yes							
Default	Status				Default Value						
	Power On Sequence				00h						
	S/W Reset				00h						
	H/W Reset				00h						

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5.2.29 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	0	38
Parameter	No Parameter									
Description	This command causes the display module to exit Idle mode.									
Restriction	This command has no effect when the display module is not in Idle mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart	Idle Mode On ↓ IDMOFF(38h) ↓ Idle Mode Off Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.30 IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	1	39
Parameter	No Parameter									
Description	This command causes the display module to enter Idle mode. In idle mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.									
Restriction	This command has no effect when the display module is in Idle mode.									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Off				
	SW Reset					Off				
	H/W Reset					Off				
Flow Chart	Idle Mode Off ↓ IDMON(39h) ↓ Idle Mode On Legend Command Parameter Display Action Mode Sequential Transfer									

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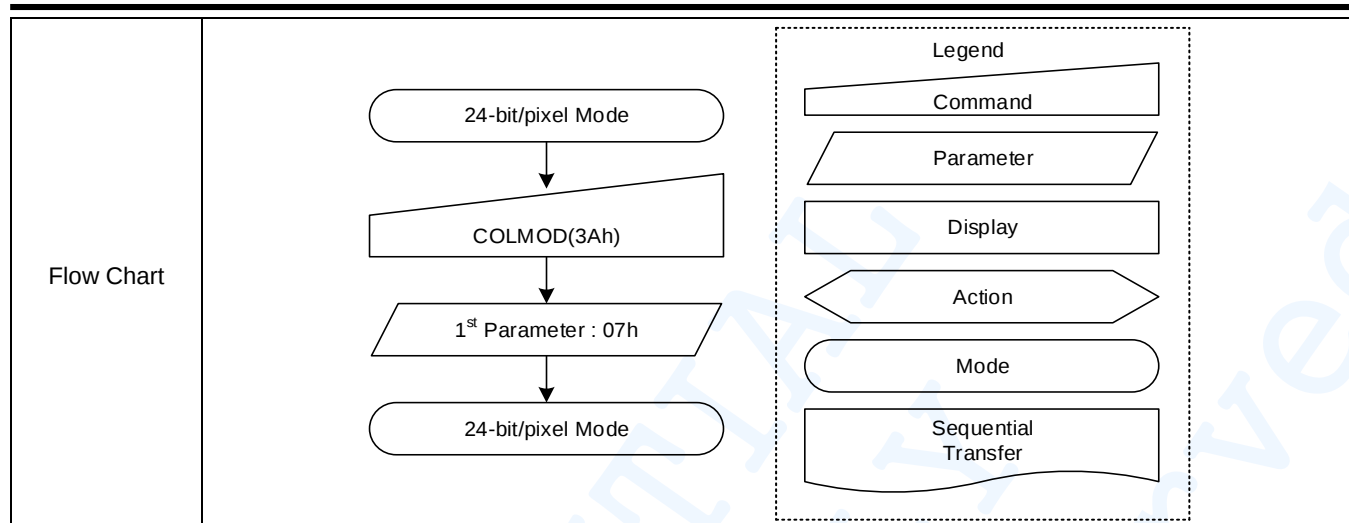
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5.2.31 COLMOD (3Ah): Control Interface Pixel Format

3AH	COLMOD (Control Interface Pixel Format)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	1	0	3A
1st Para	Write	SPI_P F_SEL	VIPF[2:0]			0	IFPF[2:0]			77
Description	This command is used to define the format of RGB picture data. The formats are shown in the table: • SPI_PF_SEL – SPI Pixel Format Selection. 0 = IFPF[2:0] is used by the SPI interface. 1 = VIPF[2:0] is used by the SPI interface. • VIPF[2:0] – This command is used by SPI_PF_SEL=1. • D[3] - Reserved This bit is not applicable for this project, so it is set to "0". • IFPF[2:0] – This command is used by SPI_PF_SEL=0 or MPU or MIPI command mode.									
	Control Interface Pixel Format		IFPF[2]	IFPF[1]	IFPF[0]	Interface Mode				
	24-bit/pixel(16.7M Color)		1	1	1	MIPI, SPI3W, SPI4W, QSPI, MPU				
	18-bit/pixel(262K Color)		1	1	0	MIPI, SPI3W, SPI4W, QSPI, MPU				
	16-bit/pixel(65K Color)		1	0	1	MIPI, SPI3W, SPI4W, QSPI, MPU				
	Setting Disable		1	0	0	-				
	3-bit/pixel(8 Color)		0	1	1	SPI3W, SPI4W, QSPI				
	8-bit/pixel(256 Color, 3-3-2)		0	1	0	SPI3W, SPI4W, QSPI				
	8-bit/pixel(256 Gray)		0	0	1	SPI3W, SPI4W, QSPI				
	Setting Disable		0	0	0	-				
	NOTE: Pixel Format is set by video packet header in video mode.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					77h				
	S/W Reset					77h				
	H/W Reset					77h				

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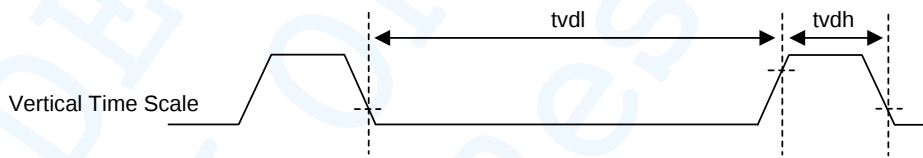
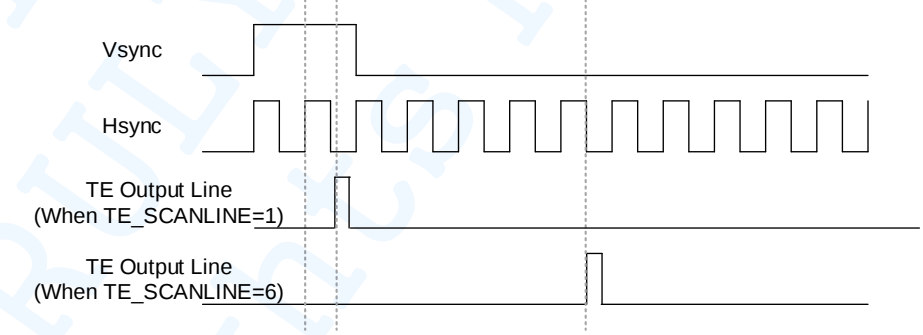
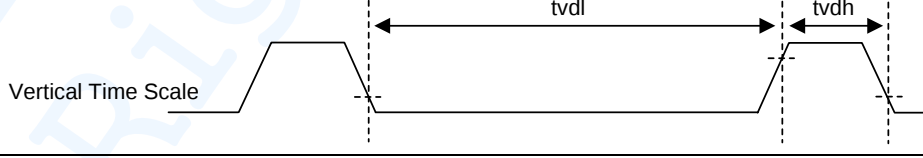
5.2.32 RAMWRC (3Ch): Memory Write Continue

3CH	RAMWRC (Memory Write Continue)									
—	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	1	0	0	3C
1st Para	Write	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	00
2nd Para	Write	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	00
---	---	---	---	---	---	---	---	---	---	00
Nth Para	Write	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00
Description	This command is used to transfer data from MCU to frame memory if user wants to continue memory write after “Memory Write Start(2Ch)” command or “Memory Write Continue(3Ch)”. This command makes no change to the other driver status. When this command is accepted and Dn[7:0] is transferred from MCU, the column register and the page register are incremented from the value which has been arrived by previous memory write operation(2CH or 3Ch).									
Restriction	Host Must send multiple of 4 parameters at once. If host does not, memory write function will not operate properly.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					Contents of memory is set randomly				
	S/W Reset					Contents of memory is set randomly				
	H/W Reset					Contents of memory is set randomly				
Flow Chart	MEMWRC(3Ch) Image Data D1[7:0], D2[7:0], Dn[7:0] Next Command Legend Command Parameter Display Action Mode Sequential Transfer									

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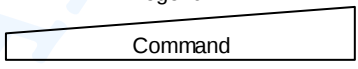
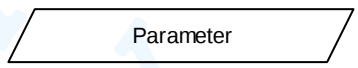
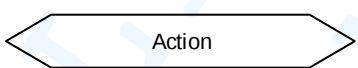
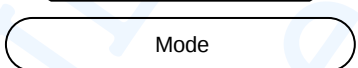
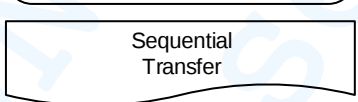
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5.2.33 TESCAN (44h): Set Tear Scan Line

44H	TESCAN (Set Tear Scan line)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	0	0	44
1st Para	Write	TE_SCANLINE[15:8]								00
2nd Para	Write	TE_SCANLINE[7:0]								00
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. When TE_SCANLINE = "1", Tearing Effect Output Line is on at the second line of VSYNC. The Tearing Effect Output line shall be active low when the display module is in Sleep mode. Note that TE_SCANLINE with N = "0" is equivalent to TEON with TEM = "0".									
	35h	44h	TE Output							
	TEM	TE_SC ANLINE								
	0	0	The Tearing Effect Output line consists of V-blanking information only. 							
			The Tearing Effect Output Line consists of Nth line information 							
	1	X	The Tearing Effect Output line consists of V-blanking information only. 							
This command takes effect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous TEON, or TESCAN, command until the end of the frame. TE_SCANLINE[15:0] always must be less than VBP + VFP + VACT.										
Register Availability	Status					Availability				
	Sleep Out					Yes				

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	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00_00h
	S/W Reset	00_00h
	H/W Reset	00_00h
Flow Chart	<pre> graph TD A([TE Output Off]) --> B[/Set Tear On(35h)/] B --> C[/1st & 2nd Parameter : TE_SCANLINE[15:0]/] C --> D([TE Output On]) </pre> Legend  Command  Parameter  Display  Action  Mode  Sequential Transfer	

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5.2.34 RDSCAN (45h): Read Scan Line Number

45H	RDSCAN (Read Scan Line Number)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	0	1	45
1st Para	Read	GET_SCANLINE[15:8]								00
2nd Para	Read	GET_SCANLINE[7:0]								00
Description	The display module returns the current scanline, N, used to update the display device. The first scanline is defined as the first line of Vsync and is denoted as line “0”. When in sleep mode, the value returned by RDSCAN is undefined.									
Restriction										
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00_00h				
	S/W Reset					00_00h				
	H/W Reset					00_00h				
Flow Chart	RDSCAN(45h) ↓ Send 1st & 2nd Parameter GET_SCANLINE[15:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.35 SPI_RDOFF (46h): SPI Read Off

46H	SPI_RDOFF (SPI Read Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	1	0	46
Parameter	No Parameter									
Description	This command disables SPI Read.									
Restriction	-									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					No				
Default	Status					Default Value				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart	SPI Read Enable ↓ SPI_RDOFF(46h) ↓ SPI Read Disable Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.36 SPI_RDON(47h): SPI Read On

47H	SPI_RDON (SPI Read On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	1	1	47
Parameter	No Parameter									
Description	This command enables SPI Read.									
Restriction	-									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					No				
Default	Status					Default Value				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart	SPI Read Disable ↓ SPI_RDON(47h) ↓ SPI Read Enable Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.37 AODOFF (48h): AOD Mode Off

48H	AODOFF (AOD Mode Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	0	0	48
Parameter	No Parameter									
Description	This command turns off AOD mode. (This command is valid when AOD_BY_IDMON=0)									
Restriction	-									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					AOD Off Mode				
	S/W Reset					AOD Off Mode				
	H/W Reset					AOD Off Mode				
Flow Chart	Display AOD Mode ↓ AODOFF(48h) ↓ Display Normal Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.38 AODON (49h): AOD Mode On

49H	AODON (AOD Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	0	1	49
Parameter	No Parameter									
Description	This command turns on AOD mode. (This command is valid when AOD_BY_IDMON=0)									
Restriction	-									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					AOD Off Mode				
	S/W Reset					AOD Off Mode				
	H/W Reset					AOD Off Mode				
Flow Chart	Display Normal Mode ↓ AODON(49h) ↓ Display AOD Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.39 AOD_WRDISBV (4Ah): Write Display Brightness Value in AOD Mode

4AH	AOD_WRDISBV (Write Display Brightness Value in AOD Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	1	0	4A
1st Para	Write	AOD_DBV[7:0]								FF
Description	This command is used to adjust the brightness value of the display in AOD(=Idle) Mode. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					FFh				
	S/W Reset					FFh				
	H/W Reset					FFh				
Flow Chart	AOD_WRDISBV(4Ah) AOD_DBV[7:0] New Display Brightness Value Loaded in AOD Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.40 AOD_RDDISBV (4Bh): Read Display Brightness Value in AOD Mode

4BH	AOD_RDDISBV (Read Display Brightness Value in AOD Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	1	1	4B
1st Para	Read	AOD_DBV[7:0]								FF
Description	This command returns the brightness value of the display in AOD(=Idle) Mode. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principal relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					FFh				
	S/W Reset					FFh				
	H/W Reset					FFh				
Flow Chart	AOD_RDDISBV(4Bh) Host Send 1st Parameter AOD_DBV[7:0] Display Legend Command Parameter Display Action Mode Sequential Transfer									

5.2.41 DSTB (4Fh): Deep Standby Control

4FH	DSTB (Deep Standby Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	1	1	1	4F
1st Para	Write	0	0	0	0	0	0	0	DSTB	00
Parameter	No Parameter									
Description	This command is used to control signal which are related to deep standby mode control ● DSTB : Deep standby mode control. 0 = Deep standby mode disable 1 = Deep standby mode enable To exit deep standby mode, set RESX low pulse more than 3ms to pin RESX. If user wants to enter deep standby mode from normal display directly, it shall enter sleep in mode & display off mode first, and wait 2 frames or more time for completing power off sequence, and then execute this command to enter deep standby mode									
Restriction	-									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	Normal Display Mode ↓ DSTB(4Fh) ↓ Send 1st Parameter DSTB ↓ Deep Standby Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.42 WRDISBV (51h): Write Display Brightness Value

51H	WRDISBV (Write Display Brightness Value)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	0	1	51
1st Para	Write	DBV[7:0]								FF
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					FFh				
	S/W Reset					FFh				
	H/W Reset					FFh				
Flow Chart	WRDISBV(51h) ↓ DBV[7:0] ↓ New Display Brightness Value Loaded Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.43 RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	1	0	52
1st Para	Read	DBV[7:0]								FF
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principal relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					FFh				
	S/W Reset					FFh				
	H/W Reset					FFh				
Flow Chart	RDDISBV(52h) Send 1st Parameter DBV[7:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.44 WRCTRLD1 (53h): Write CTRL Display 1

53H	WRCTRLD1 (Write CTRL Display 1)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	1	1	53
1st Para	Write	0	0	BCTRL	0	DISP_DIM	0	0	0	28
Description	This command control related display brightness. • D[7:6] - Reserved. These bits are not applicable for this project, so it is set to "0". • BCTRL - Brightness Control 0 = Off 1 = On • D[4] - Reserved This bit is not applicable for this project, so it is set to "0". • DISP_DIM – Display Dimming 0 = Display Dimming Off 1 = Display Dimming On • D[2:0] - Reserved These bits are not applicable for this project, so it is set to "0".									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					28h				
	S/W Reset					28h				
	H/W Reset					28h				
Flow Chart	WRCTRLD1(53h) ↓ 1st Parameter BCTRL, DISP_DIM					Legend Command Parameter Display Action Mode Sequential Transfer				

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5.2.45 RDCTRLD1 (54h): Read CTRL Display 1

54H	RDCTRLD1 (Read CTRL Display 1)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	0	0	54
1st Para	Read	0	0	BCTRL	0	DISP_DIM	0	0	0	28
Description	This command returns the brightness value of ‘Write CTRL Display 1’. • D[7:6] - Reserved. These bits are not applicable for this project, so it is set to "0". • BCTRL - Brightness Control 0 = Off 1 = On • D[4] - Reserved This bit is not applicable for this project, so it is set to "0". • DISP_DIM – Display Dimming 0 = Display Dimming Off 1 = Display Dimming On • D[2:0] - Reserved These bits are not applicable for this project, so it is set to "0".									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					28h				
	S/W Reset					28h				
	H/W Reset					28h				
Flow Chart	RDCTRLD1(54h) ↓ Send 1st Parameter BCTRL, DISP_DIM Host ----- Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.46 WRCTRLD2 (55h): Write CTRL Display 2

55H	WRCTRLD2 (Write CTRL Display 2)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	0	1	55
1st Para	Write	0	0	0	0	0	0	ACL_PROF[1:0]		00
Description	This command control related display brightness. • D[7:2] - Reserved These bits are not applicable for this project, so it is set to “0” • ACL_PROF[1:0] – Select ACL Profile 0 = ACL Off 1 = Profile 1 2 = Profile 2 3 = Profile 3									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	WRCTRLD2(55h) ↓ 1st Parameter ACL_PROF[1:0] Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.47 RDCTRLD2 (56h): Read CTRL Display 2

56H	RDCTRLD2 (Read CTRL Display 2)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	1	0	56
1st Para	Read	0	0	0	0	0	0	ACL_PROF[1:0]		00
Description	This command returns the brightness value of ‘Write CTRL Display 2.’ • D[7:2] - Reserved These bits are not applicable for this project. It is “0” • ACL_PROF[1:0] – Select ACL Profile 0 = ACL Off 1 = Profile 1 2 = Profile 2 3 = Profile 3									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	RDCTRLD2(56h) ↓ Send 1st Parameter ACL_PROF[1:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.48 WR_CE (58h): Write CE

58H	WR_CE (Write CE)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	1	0	0	0	58
1st Para	Write	0	0	0	0	0	SRE_EN	SRE_MODE[1:0]		00
Description	This command control related SRE (Sunlight Readability Enhancement) • D[7:3] - Reserved. These bits are not applicable for this project, so it is set to "0". • SRE_EN – SRE Control 0 = Off 1 = On • SRE_MODE[1:0] – Sunlight Readability Mode 0 = Low 1 = Low 2 = Medium 3 = High									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	WR_CE(58h) ↓ 1st Parameter SRE_EN, SRE_MODE[1:0] Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.49 RD_CE (59h): Read CE

59H	RD_CE (Read CE)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	1	0	0	1	59
1st Para	Read	0	0	0	0	0	SRE_EN	SRE_MODE[1:0]		00
Description	This command control related SRE (Sunlight Readability Enhancement) • D[7:3] - Reserved. These bits are not applicable for this project, so it is set to "0". • SRE_EN – SRE Control 0 = Off 1 = On • SRE_MODE[1:0] – Sunlight Readability Mode 0 = Low 1 = Low 2 = Medium 3 = High									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	RD_CE(59h) Host Send 1st Parameter SRE_EN, SRE_MODE[1:0] Display Legend Command Parameter Display Action Mode Sequential Transfer									

5.2.50 HBM_WRDISBV (63h): Write Display Brightness Value in HBM Mode

63H	HBM_WRDISBV (Write Display Brightness Value in HBM Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	0	1	1	63
1st Para	Write	HBM_DBV[7:0]								FF
Description	This command is used to adjust the brightness value of the display in HBM Mode. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					FFh				
	S/W Reset					FFh				
	H/W Reset					FFh				
Flow Chart	HBM_WRDISBV(63h) ↓ HBM_DBV[7:0] ↓ New Display Brightness Value Loaded in HBM Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.51 HBM_RDDISBV (64h): Read Display Brightness Value in HBM Mode

64H	HBM_RDDISBV (Read Display Brightness Value in HBM Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	1	0	0	64
1st Para	Read	HBM_DBV[7:0]								FF
Description	This command returns the brightness value of the display in HBM Mode. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principal relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					FFh				
	S/W Reset					FFh				
	H/W Reset					FFh				
Flow Chart	HBM_RDDISBV(64h) ↓ Send 1st Parameter HBM_DBV[7:0] Host ----- Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.52 RDHBMCTL (65h): Read HBM Control

66H	RDHBMCTL (Read HBM Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	1	0	1	65
1st Para	Read	0	0	0	0	0	0	HBM_EN	0	00
Description	This command control related high brightness mode. • D[7:2] - Reserved. These bits are not applicable for this project, so it is set to "0". • HBM_EN – HBM Control 0 = Off 1 = On • D[0] - Reserved. This bit is not applicable for this project, so it is set to "0".									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	RDHBMCTL(65h) ↓ Send 1st Parameter HBM_EN Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.53 HBMCTL (66h): HBM Control

66H	HBMCTL (HBM Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	1	1	0	66
1st Para	Write	0	0	0	0	0	0	HBM_EN	0	00
Description	This command control related high brightness mode. • D[7:2] - Reserved. These bits are not applicable for this project, so it is set to "0". • HBM_EN – HBM Control 0 = Off 1 = On • D[0] - Reserved. This bit is not applicable for this project, so it is set to "0".									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	HBMCTL(66h) HBM_EN, HBM_MODE[1:0] New Display Brightness Value Loaded in HBM Mode Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.54 COLSET0 to COLSET15 (70h to 7Fh): SPI 1-1-1 Pixel Format Set

70H to 7FH	COLSETn (SPI Pixel Format Set)									
–	Write	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	1	0	0	0	0	70
1st Para	Write	COLSET0_R[7:0]								00
2nd Para	Write	COLSET0_G[7:0]								00
3rd Para	Write	COLSET0_B[7:0]								00
Command	Write	0	1	1	1	0	0	0	1	71
1st Para	Write	COLSET1_R[7:0]								00
2nd Para	Write	COLSET1_G[7:0]								00
3rd Para	Write	COLSET1_B[7:0]								FF
Command	Write	0	1	1	1	0	0	1	0	72
1st Para	Write	COLSET2_R[7:0]								00
2nd Para	Write	COLSET2_G[7:0]								FF
3rd Para	Write	COLSET2_B[7:0]								00
Command	Write	0	1	1	1	0	0	1	1	73
1st Para	Write	COLSET3_R[7:0]								00
2nd Para	Write	COLSET3_G[7:0]								FF
3rd Para	Write	COLSET3_B[7:0]								FF
Command	Write	0	1	1	1	0	1	0	0	74
1st Para	Write	COLSET4_R[7:0]								FF
2nd Para	Write	COLSET4_G[7:0]								00
3rd Para	Write	COLSET4_B[7:0]								00
Command	Write	0	1	1	1	0	1	0	1	75
1st Para	Write	COLSET5_R[7:0]								FF
2nd Para	Write	COLSET5_G[7:0]								00
3rd Para	Write	COLSET5_B[7:0]								FF
Command	Write	0	1	1	1	0	1	1	0	76
1st Para	Write	COLSET6_R[7:0]								FF
2nd Para	Write	COLSET6_G[7:0]								FF
3rd Para	Write	COLSET6_B[7:0]								00
Command	Write	0	1	1	1	0	1	1	1	77
1st Para	Write	COLSET7_R[7:0]								FF
2nd Para	Write	COLSET7_G[7:0]								FF
3rd Para	Write	COLSET7_B[7:0]								FF
Command	Write	0	1	1	1	1	0	0	0	78
1st Para	Write	COLSET8_R[7:0]								00
2nd Para	Write	COLSET8_G[7:0]								00

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3td Para	Write	COLSET8_B[7:0]								00
Command	Write	0	1	1	1	1	0	0	1	79
1st Para	Write	COLSET9_R[7:0]								00
2nd Para	Write	COLSET9_G[7:0]								00
3td Para	Write	COLSET9_B[7:0]								FF
Command	Write	0	1	1	1	1	0	1	0	7A
1st Para	Write	COLSETA_R[7:0]								00
2nd Para	Write	COLSETA_G[7:0]								FF
3td Para	Write	COLSETA_B[7:0]								00
Command	Write	0	1	1	1	1	0	1	1	7B
1st Para	Write	COLSETB_R[7:0]								00
2nd Para	Write	COLSETB_G[7:0]								FF
3td Para	Write	COLSETB_B[7:0]								FF
Command	Write	0	1	1	1	1	1	0	0	7C
1st Para	Write	COLSETC_R[7:0]								FF
2nd Para	Write	COLSETC_G[7:0]								00
3td Para	Write	COLSETC_B[7:0]								00
Command	Write	0	1	1	1	1	1	0	1	7D
1st Para	Write	COLSETD_R[7:0]								FF
2nd Para	Write	COLSETD_G[7:0]								00
3td Para	Write	COLSETD_B[7:0]								FF
Command	Write	0	1	1	1	1	1	1	0	7E
1st Para	Write	COLSETE_R[7:0]								FF
2nd Para	Write	COLSETE_G[7:0]								FF
3td Para	Write	COLSETE_B[7:0]								00
Command	Write	0	1	1	1	1	1	1	1	7F
1st Para	Write	COLSETF_R[7:0]								FF
2nd Para	Write	COLSETF_G[7:0]								FF
3td Para	Write	COLSETF_B[7:0]								FF
Description	This command set the SPI 1-1-1 color format map directly to 24bits by command 70h to 7Fh.									
	SPI 1-1-1 color mapping				R[7:0]		G[7:0]		B[7:0]	
	0000 (70h)				COLSET0_R[7:0]		COLSET0_G[7:0]		COLSET0_B[7:0]	
	0001 (71h)				COLSET1_R[7:0]		COLSET1_G[7:0]		COLSET1_B[7:0]	
	0010 (72h)				COLSET2_R[7:0]		COLSET2_G[7:0]		COLSET2_B[7:0]	
	0011 (73h)				COLSET3_R[7:0]		COLSET3_G[7:0]		COLSET3_B[7:0]	
	0100 (74h)				COLSET4_R[7:0]		COLSET4_G[7:0]		COLSET4_B[7:0]	
	0101 (75h)				COLSET5_R[7:0]		COLSET5_G[7:0]		COLSET5_B[7:0]	

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	0110 (76h)	COLSET6_R[7:0]	COLSET6_G[7:0]	COLSET6_B[7:0]
	0111 (77h)	COLSET7_R[7:0]	COLSET7_G[7:0]	COLSET7_B[7:0]
	1000 (78h)	COLSET8_R[7:0]	COLSET8_G[7:0]	COLSET8_B[7:0]
	1001 (79h)	COLSET9_R[7:0]	COLSET9_G[7:0]	COLSET9_B[7:0]
	1010 (7Ah)	COLSETA_R[7:0]	COLSETA_G[7:0]	COLSETA_B[7:0]
	1011 (7Bh)	COLSETB_R[7:0]	COLSETB_G[7:0]	COLSETB_B[7:0]
	1100 (7Ch)	COLSETC_R[7:0]	COLSETC_G[7:0]	COLSETC_B[7:0]
	1101 (7Dh)	COLSETD_R[7:0]	COLSETD_G[7:0]	COLSETD_B[7:0]
	1110 (7Eh)	COLSETE_R[7:0]	COLSETE_G[7:0]	COLSETE_B[7:0]
	1111 (7Fh)	COLSETF_R[7:0]	COLSETF_G[7:0]	COLSETF_B[7:0]
	Restriction	-		
Register Availability	Status		Availability	
	Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value	
	Power On Sequence		000000h (70h) to FFFFFFFh (7Fh)	
	SW Reset		000000h (70h) to FFFFFFFh (7Fh)	
	H/W Reset		000000h (70h) to FFFFFFFh (7Fh)	
Flow Chart	16 colors set ↓ COLSETn(70h to 80h) ↓ 3 Parameters ↓ New 16 colors set Legend Command Parameter Display Action Mode Sequential Transfer			

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5.2.55 COLOPT (80h): SPI 1-1-1/256 Pixel Format Option

80H	COLOPT (SPI Pixel Format Option)										
–	Write	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	1	0	0	0	0	0	0	0	80	
1st Para	Write	0	111_OPT	0	0	4BIT_EN	GRAY256_COLOR[2:0]			07	
Description	This command set the SPI 1-1-1/256 gray color format options.										
	111_OPT = 0 Supporting in IFPF[2:0]=011 case setting by 3Ah (Interface pixel format is SPI 1-1-1)										
	1-1-1 Bit	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Note
	CMDWR	0	0	0	0	0	0	0	0	0	2Ch for GRAM Write
	1 st RAM Data	1	x	x	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	1,2 pixel data
	2 nd RAM Data	1	x	x	R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]	3,4 pixel data
	3 rd RAM Data	1	x	x	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]	5,6 pixel data
	...										...
	111_OPT = 1 Supporting in IFPF[2:0]=011 case setting by 3Ah (Interface pixel format is SPI 1-1-1)										
	1-1-1 Bit	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Note
	CMDWR	0	0	0	0	0	0	0	0	0	2Ch for GRAM Write
	1 st RAM Data	1	x	R1[0]	G1[0]	B1[0]	x	R2[0]	G2[0]	B2[0]	1,2 pixel data
	2 nd RAM Data	1	x	R3[0]	G3[0]	B3[0]	x	R4[0]	G4[0]	B4[0]	3,4 pixel data
	3 rd RAM Data	1	x	R5[0]	G5[0]	B5[0]	x	R6[0]	G6[0]	B6[0]	5,6 pixel data
	...										...
	4BIT_EN = 0 Supporting in IFPF[2:0]=011 case setting by 3Ah (Interface pixel format is SPI 1-1-1) Three bits per pixel formats map directly to 24bits by command 70h to 77h										
	1-1-1 Bit	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Note
	CMDWR	0	0	0	0	0	0	0	0	0	2Ch for GRAM Write
	1 st RAM Data	1	x	x	P1[2]	P1[1]	P1[0]	P2[2]	P2[1]	P2[0]	1,2 pixel data
	2 nd RAM Data	1	x	x	P3[2]	P3[1]	P3[0]	P4[2]	P4[1]	P4[0]	3,4 pixel data
	3 rd RAM Data	1	x	x	P5[2]	P5[1]	P5[0]	P6[2]	P6[1]	P6[0]	5,6 pixel data
	...										...
	Example :										
P1[2:0] = 3'b101 = {COLSET5_R[7:0], COLSET5_G[7:0], COLSET5_B[7:0]} by command 75h											

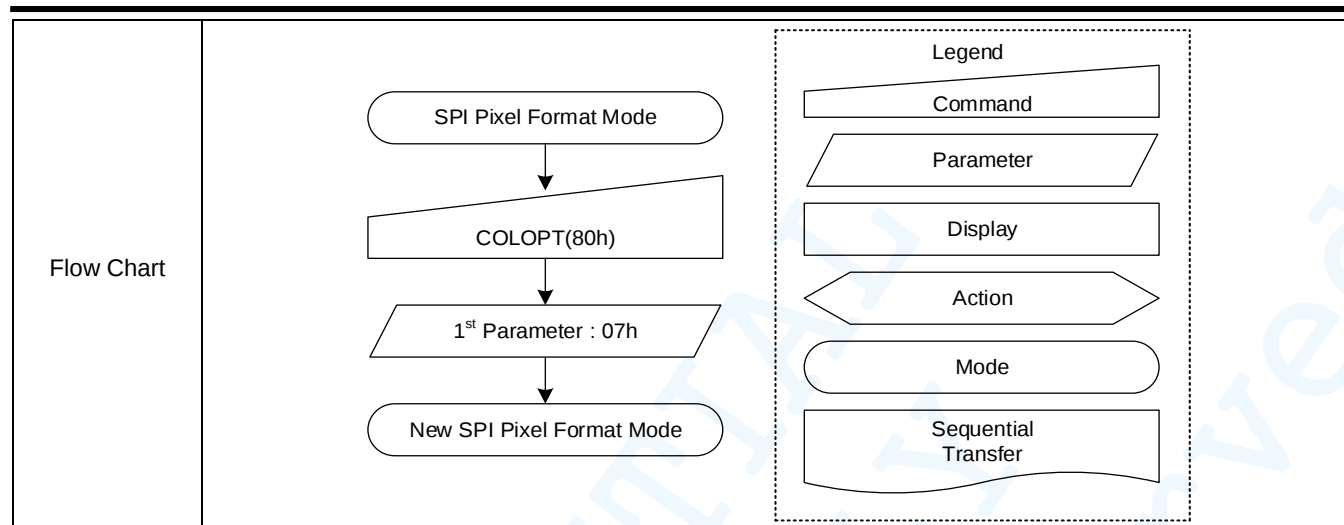
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	• 4BIT_EN = 1 Supporting in IFPF[2:0]=011 case setting by 3Ah (Interface fpixel format is SPI 1-1-1) Four bits per pixel formats map directly to 24bits by command 70h to 7Fh										
	1-1-1 Bit	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Note
	CMDWR	0	0	0	0	0	0	0	0	0	2Ch for GRAM Write
	1 st RAM Data	1	P1[3]	P1[2]	P1[1]	P1[0]	P2[3]	P2[2]	P2[1]	P2[0]	1,2 pixel data
	2 nd RAM Data	1	P3[3]	P3[2]	P3[1]	P3[0]	P4[3]	P4[2]	P4[1]	P4[0]	3,4 pixel data
	3 rd RAM Data	1	P5[3]	P5[2]	P5[1]	P5[0]	P6[3]	P6[2]	P6[1]	P6[0]	5,6 pixel data
	...										...
	Example : P1[3:0] = 4'b1101 = {COLSETD_R[7:0], COLSETD_G[7:0], COLSETD_B[7:0]} by command 7Dh										
	• GRAY256_COLOR Supporting in IFPF[2:0]=001 case setting by 3Ah (Interface fpixel format is SPI 256 Gray) This command sets the valid red, green and blue 256 grayscale.										
	GRAY256_COLOR[2:0]		Read Grayscale			Green Grayscale			Blue Grayscale		
	000		00000000			00000000			00000000		
	001		00000000			00000000			P[7:0]		
	010		00000000			P[7:0]			00000000		
	011		00000000			P[7:0]			P[7:0]		
	100		P[7:0]			00000000			00000000		
	101		P[7:0]			00000000			P[7:0]		
	110		P[7:0]			P[7:0]			00000000		
	111		P[7:0]			P[7:0]			P[7:0]		
Restriction	-										
Register Availability	Status					Availability					
	Sleep Out					Yes					
	Sleep In					Yes					
Default	Status					Default Value					
	Power On Sequence					07h					
	S/W Reset					07h					
	H/W Reset					07h					

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5.2.56 RDDDBS (A1h): Read DDB Start

A1H	RDDDBS (Read DDB Start)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	0	0	0	1	A1
1st Para	Read	DDB1[7:0]								00
2nd Para	Read	DDB2[7:0]								00
3rd Para	Read	DDB3[7:0]								00
4th Para	Read	DDB4[7:0]								00
5th Para	Read	DDB5[7:0]								00
6th Para	Read	DDB6[7:0]								00
7th Para	Read	DDB7[7:0]								00
8th Para	Read	DDB8[7:0]								00
9th Para	Read	1	1	1	1	1	1	1	1	FF
Description	This command returns supplier identification and display module model/revision information of DDh. NOTE: This information is not the same <u>RDID1(DAh) : Read ID1</u> , <u>RDID2(DBh) : Read ID2</u> , and <u>RDID3(DCh) : Read ID3</u> commands are returning.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					(OTP value)				
	S/W Reset					(OTP value)				
	H/W Reset					(OTP value)				
Flow Chart	RDDDBS(A1h) Send 1st & 2nd Parameter Send 3rd & 4th Parameter Send 5th & 6th Parameter Send 7th & 8th Parameter Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.57 RDDDBC (A8h): Read DDB Continue

A8H	RDDDBC (Read DDB Continue)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	1	0	0	0	A8
1st Para	Read	DDBn+1[7:0]								00
2nd Para	Read	DDBn+2[7:0]								00
3rd Para	Read	DDBn+3[7:0]								00
4th Para	Read	DDBn+4[7:0]								00
5th Para	Read	DDBn+5[7:0]								00
6th Para	Read	DDBn+6[7:0]								00
7th Para	Read	DDBn+7[7:0]								00
8th Para	Read	DDBn+8[7:0]								00
9th Para	Read	1	1	1	1	1	1	1	1	FF
Description	This command returns supplier identification and display module model/revision information of DDh. NOTE: This information is not the same <u>RDID1(DAh) : Read ID1</u> , <u>RDID2(DBh) : Read ID2</u> and <u>RDID3(DCh) : Read ID3</u> commands are returning. Use when want to read DDh continuously after used A1h.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					(OTP value)				
	S/W Reset					(OTP value)				
	H/W Reset					(OTP value)				
Flow Chart	RDDDBC(A8h) Send 1st & 2nd Parameter Send 3rd & 4th Parameter Send 5th & 6th Parameter Send 7th & 8th Parameter Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.58 RDFCS (AAh): Read First Checksum

AAH	RDFCS (Read First Checksum)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	1	0	1	0	AA
1st Para	Read	FCS[7:0]								00
Description	This command returns the first checksum what has been calculated from “User Command Set” area registers(not include “Manufacture Command Set”) and the frame memory after write access to those registers and/or frame memory has been done.									
Restriction	It will be necessary to wait 150ms after there is the last access on “User Command Set” area registers before there can read this checksum value.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	RDFCS(AAh) Send 1st Parameter FCS[7:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.59 RDCCS (AFh): Read Continue Checksum

AFH	RDCCS (Read Continue Checksum)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	1	1	1	1	AF
1st Para	Read	CCS[7:0]								00
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.									
Restriction	It will be necessary to wait 300ms after there is the last access on “User Command Set” area registers before there can read this checksum value in the first time.									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart	RDCCS(AFh) Send 1st Parameter CCS[7:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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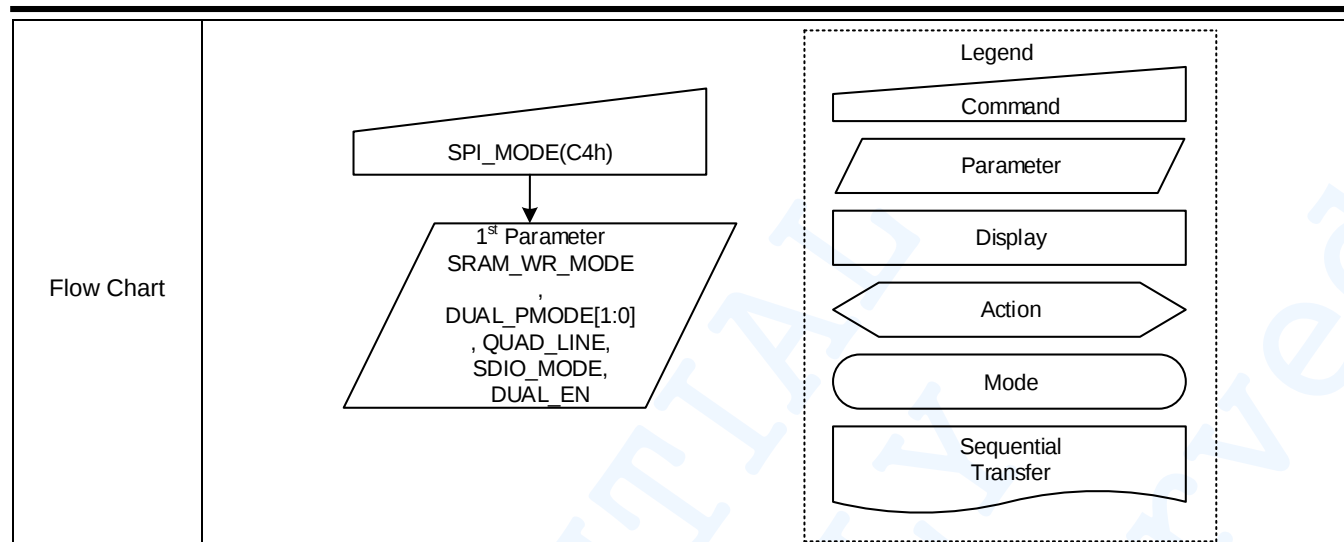
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5.2.60 SPI_MODE (C4h): SPI Mode Control

C4H	SPI_MODE (SPI Mode Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	0	0	1	0	0	C4
1st Para	Write	0	0	DUAL_PMODE[1:0]		0	QUAD_LINE	SDIO_MODE	DUAL_EN	00
Description	This command control interface mode. • D[6] - Reserved This bit is not applicable for this project, so it is set to “0”. • DUAL_PMODE[1:0] – RGB image data transfer format in SPI3,4W interface mode 0 = 1P / 1T 1 line 1 = 1P / 1T for 2 line 2 = 2P / 3T for 2 line • D[3] - Reserved This bit is not applicable for this project, so it is set to “0”. • QUAD_LINE – Quad line 0 = SDIO, SDI1, SDI2, SDI3 (4 line) 1 = SDIO (1 line) • SDIO_MODE – Read protocol in SPI3,4W interface mode 0 = SDI 1 = SDI + SDO • DUAL_EN – Dual mode enable in SPI3,4W interface mode 0 = Disable 1 = Enable									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				

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5.2.61 RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	1	1	0	1	0	DA
1st Para	Read	ID1[7:0]								00
Description	This read byte is an identifier. It is specified by Module maker code.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					(OTP value)				
	S/W Reset					(OTP value)				
	H/W Reset					(OTP value)				
Flow Chart	RDID1(DAh) ↓ Send 1st Parameter ID1[7:0] Host ----- Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.62 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	1	1	0	1	1	DB
1st Para	Read	ID2[7:0]								00
Description	This read byte is an identifier. It is specified by Module/Driver version.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					(OTP value)				
	SW Reset					(OTP value)				
	H/W Reset					(OTP value)				
Flow Chart	RDID2(DBh) ↓ Send 1st Parameter ID2[7:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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5.2.63 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	1	1	1	0	0	DC
1st Para	Read	ID3[7:0]								00
Description	This read byte is an identifier. It is specified by Module/Driver project code.									
Restriction	–									
Register Availability	Status					Availability				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	Status					Default Value				
	Power On Sequence					(OTP value)				
	S/W Reset					(OTP value)				
	H/W Reset					(OTP value)				
Flow Chart	RDID3(DCh) ↓ Send 1st Parameter ID3[7:0] Host Display Legend Command Parameter Display Action Mode Sequential Transfer									

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