P47001

20x2 Character Yellow OLED Application Notes (For 4-SPI Interface)

Revision History

Version	Content
X01	First release

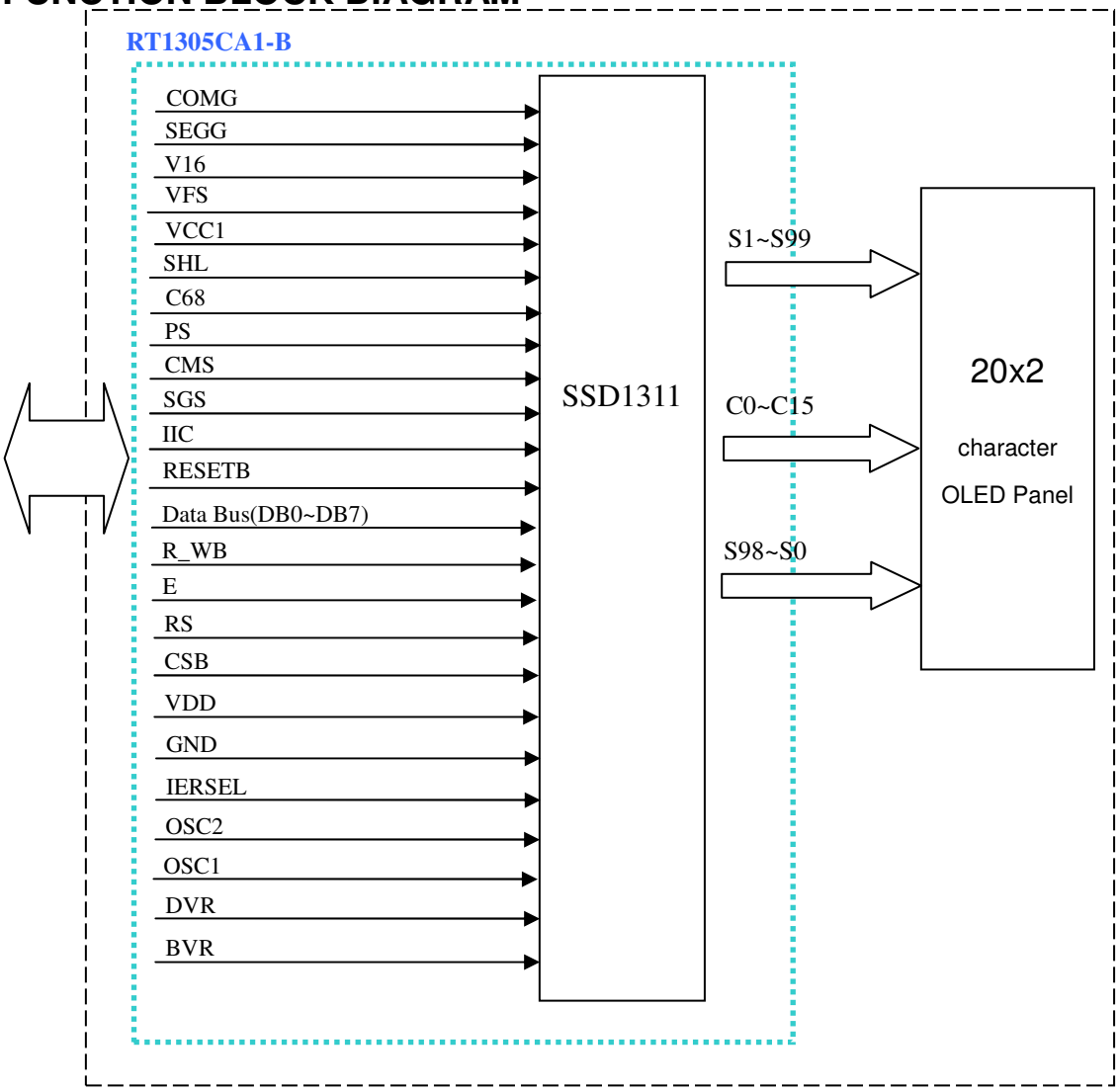
DESCRIPTION

P47001 is a 20x2 character Yellow passive OLED module with controller for many compact portable applications.

FEATURE

- Panel matrix: 20x2 character.
- Driver IC：RT1305CA1-B.
- V16=12V.
- VCC1=2.7V~ 5.5V.
- 8080/6800-series 4bit/8bit parallel bi-directional interface, SPI3/SPI4 interface, IIC interface.
- 128 x 8-bit Display RAM.
- Build-in 64x8-bits character generator RAM.

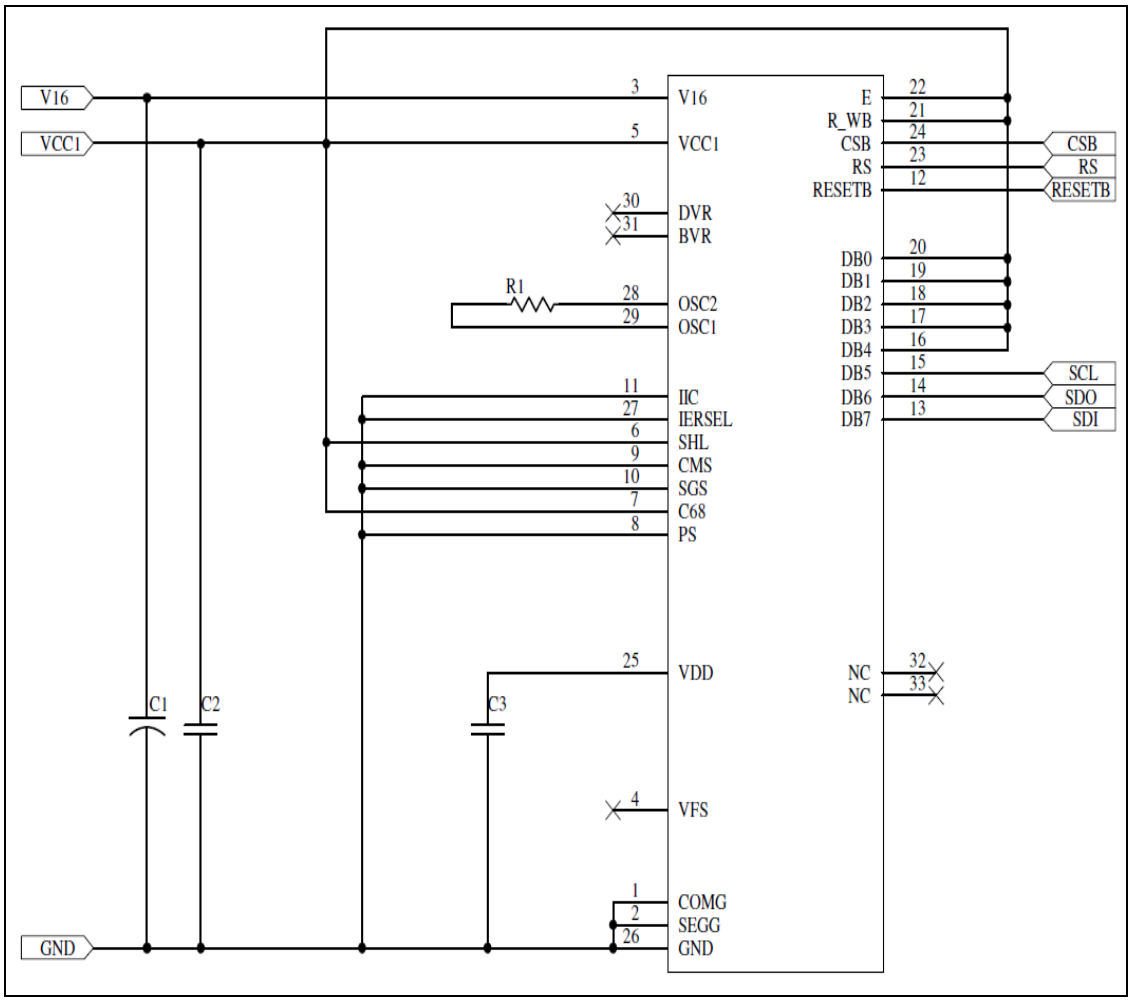
FUNCTION BLOCK DIAGRAM



RiTdisplay 20X2 character OLED Module

Application circuit

(ExternalDC/DC)



Recommend components:

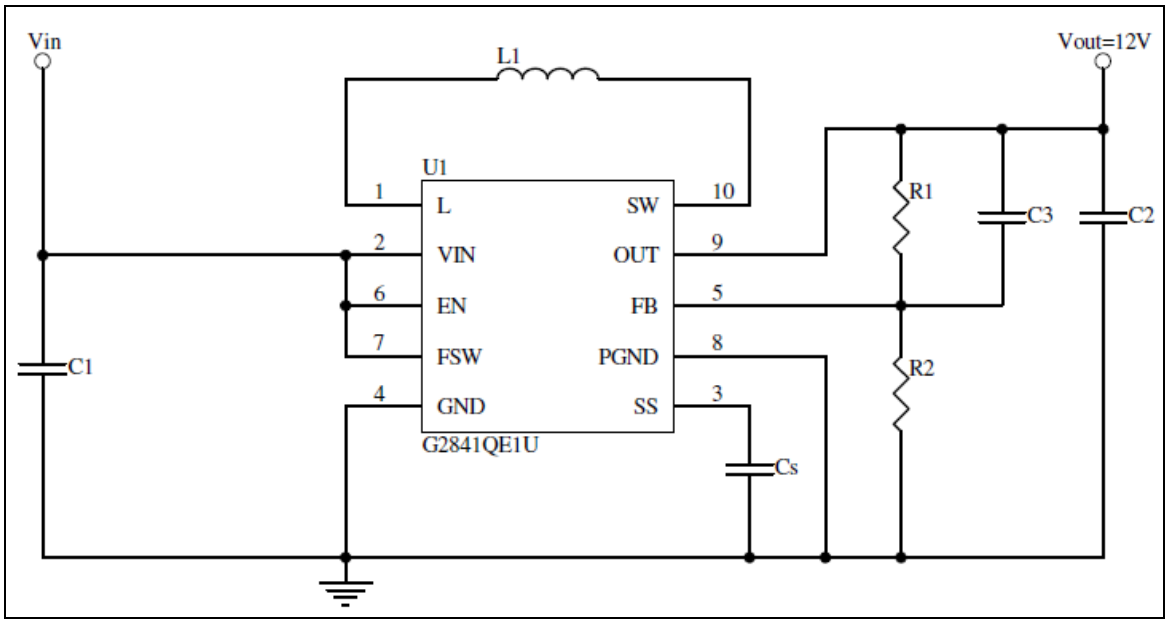
C1: 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)

C2, C3: 1uF/16V(0603)

R1: 43K ohm 1%(0603)

This circuit is for SPI4 interface.

DC-DC application circuit for OLED module(For External DC/DC)



Recommend components:

The C1: 4.7uF/6.3V.

The C2: 4.7 uF/25V Tantalum type capacitor.

The C3: 50pF/16V.

The CS: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 137K ohm/ 1%.

The L1: 4.7uH.

The U1: G2841AQE1U(Global Mixed-mode Technology)

The R1, R2 and C3 value should be fine tune by customer.

Pin Assignments

PIN No.	PIN Name.	DESCRIPTION	Setting at each interface		
			6800 parallel	SPI4	IIC
1	COMG	OLED COM drive power supply (0V).			
2	SEGG	OLED SEG drive power supply (0V).			
3	V16	Power supply for panel driving voltage.			
4	VFS	For Test , Please keep floating or VSS.			
5	VCC1	Logic power pin.			
6	SHL	Data shift direction pin. User can this pin to decide display direction.			
7	C68	I/O interface configuration pins.	High	High	High/ Low
8	PS	I/O interface configuration pins.	High	Low	High/ Low
9	CMS	COM output mapping selection.			
10	SGS	SEG output mapping selection.			
11	IIC	I/O interface configuration pins.	Low	Low	High
12	RESETB	Reset pin. When RESETB is “L”, the chip will be initialized to it’s default state.			
13	DB7	I/O interface data pins These pins are used for data transfer and reception between the MPU and RT1305. DB0~DB3 are not used during a 4-bit operation. DB7 can be used as a Busy Flag.	DB7	SDI	SDI
14	DB6		DB6	SDO	SDO
15	DB5		DB5	SCL	SCL
16	DB4		DB4	High	High
17	DB3		DB3	High	High
18	DB2		DB2	High	High
19	DB1		DB1	High	High
20	DB0		DB0	High	High
21	R_WB	Read/Write Control Input Pin.	R_WB	High	High
22	E	Read/Write Control Input Pin.	E	High	High
23	RS	Register Select Input Pin When this pin is set to "0", it is used as an Instruction Register. When this pin is set to "1", it is used for as the Data Register.	RS	RS	High
24	CSB	Chip select input pins Data / instruction I/O is enabled only when CSB is “L”.	CSB	CSB	High
25	VDD	Internal core power pin (connect to a stabilization capacitor).			
26	GND	Logic ground pin (0V).			
27	IERSEL	IERSEL=H : internal res oscillator IERSEL=L : external res oscillator			

28	OSC2	Oscillator Output Pin.			
29	OSC1	Oscillator Input Pin.			
30	DVR	Pre charge time control.			
31	BVR	Brightness control pin.			
32	NC	This is dummy pin.			
33	NC	This is dummy pin.			

Note

(1) Low is connected to GND

(2) High is connected to VCC1.

Application Initial Setting

/*20x2 character OLED driver program*/

/*The more detail of SPI4 sequence please refer the RT1305CA1-B datasheet */

```
void initial(void)
{
comm_out(0x06);//Entry Mode Set
comm_out(0x13);//DISABLE INTERNAL POWER
comm_out(0x38);//Function Set
delay_mSec(10);//Delay 10m sec
cleanDDR();
//-----------------------------------------------------------------------------------------
comm_out(0x03);//test on
comm_out(0x73);//select internal DVR,BVR
comm_out(0xfa);//BVR current
comm_out(0x32);
comm_out(0xfb);//DVR control
comm_out(0x3e);
comm_out(0x00);//test off
//-----------------------------------------------------------------------------------------
comm_out(0x0c);//Display ON Control
}
```

```
void cleanDDR(void)
{
int i;
      comm_out(0x80+0x00);//Set RAM address
      for(i=0;i<40;i++)
      {
      data_out(0x20); //Line1 display blank
      }
      comm_out(0x80+0x40);//Set RAM address
      for(i=0;i<40;i++)
      {
      data_out(0x20); //Line2 display blank
      }
}
```

After initial the driver IC, user can display character directly.

```
void show_data(void)
{
int i,j;
      comm_out(0x80+0x00);//Set RAM address
      for(i=0;i<16;i++)
      {
      data_out(0x30+i);//Line1 display character ’0’~’?’
      }
      for(j=0;j<4;j++)
      {
      data_out(0x20);
      }
      comm_out(0x80+0x40);//Set RAM address
      for(i=0;i<16;i++)
      {
      data_out(0x30+i); //Line2 display character ’0’~’?’
      }
      for(j=0;j<4;j++)
      {
      data_out(0x20);
      }

}
```

Graphic Display Data RAM (GDDRAM)

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR5 X 8DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
High						Low		High				Low		High						Low		
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	1	1	1	0	Character pattern 1
											0	0	1	*	*	*	1	0	0	0	1	
											0	1	0	*	*	*	1	0	0	0	1	
											0	1	1	*	*	*	1	1	1	1	0	
											1	0	0	*	*	*	1	0	1	0	0	
											1	0	1	*	*	*	1	0	0	1	0	
											1	1	0	*	*	*	1	0	0	0	1	
											1	1	1	*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	0	0	1	0	0	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern 2
											0	0	1	*	*	*	0	1	0	1	0	
											0	1	0	*	*	*	1	1	1	1	1	
											0	1	1	*	*	*	0	0	1	0	0	
											1	0	0	*	*	*	1	1	1	1	1	
											1	0	1	*	*	*	0	0	1	0	0	
											1	1	0	*	*	*	0	0	1	0	0	
											1	1	1	*	*	*	0	0	0	0	0	Cursor position
0	0	0	0	*	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	*	*	*	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	Character pattern 3~7
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	0	0	0	0	0	Character pattern 8
											0	0	1	*	*	*	0	1	0	1	0	
											0	1	0	*	*	*	0	0	0	0	0	
											0	1	1	*	*	*	0	0	0	0	0	
											1	0	0	*	*	*	1	0	0	0	1	
											1	0	1	*	*	*	0	1	1	1	0	
											1	1	0	*	*	*	0	0	1	0	0	
											1	1	1	*	*	*	0	0	0	0	0	Cursor position

INTERNAL RESET CIRCUIT INITIALIZATION

When power is turned ON, RT1305CA1-B is initialized automatically by an internal reset circuit. The following items are set (default) during the initialization.

1.Displayclear

2.Functionset:
DL="1":8-bit interface data,"0":4-bit data length
N="0": 1-line display
F="0":5x8 dot character font

3.Power turn off
PWR="0"

4.Display on/off control:
D="0":Display off
C="0":Cursor off
B="0":Blinking off

5.Entry mode set
I/D="0":Decrement by1
S="0":No shift

6.Cursor/Display shift/Mode / Pwr
S/C="0", R/L="1": Shifts cursor position to the right
G/C="0": Character mode
Pwr="1": Internal DCDC power on, "0": Internal DCDC power off

The Busy Flag(BF) is in a busy state until the initialization is completed (BF="1").The busy state will be In effect 10 ms after VDD stabilization.

Thank You