P44803

128x128 White OLED
Application Notes

(for SPI Interface)

Design Dept.

RiTdisplay Corporation

Revision History

| Version	REVISION DESCRIPTION
X01	First release

DESCRIPTION

P44803 is a 128x128 dot matrix White passive OLED module with controller for many compact portable applications.

FEATURE

- Panel matrix 128x128
- Driver IC: SH1107
- VPP=13.5V
- VDD = 1.65V ~ 3.5V
- 4-wire serial peripheral interface.
- Row re-mapping and column re-mapping.
- Vertical scrolling.

FUNCTION BLOCK DIAGRAM

SH1107

VSS

Data Bus(SCL & SI)

A0

RES

CS

IREF

VDD

VCOMH

VPP

SH1107

S0 ~ S126

C0 ~ C127

S127 ~ S1
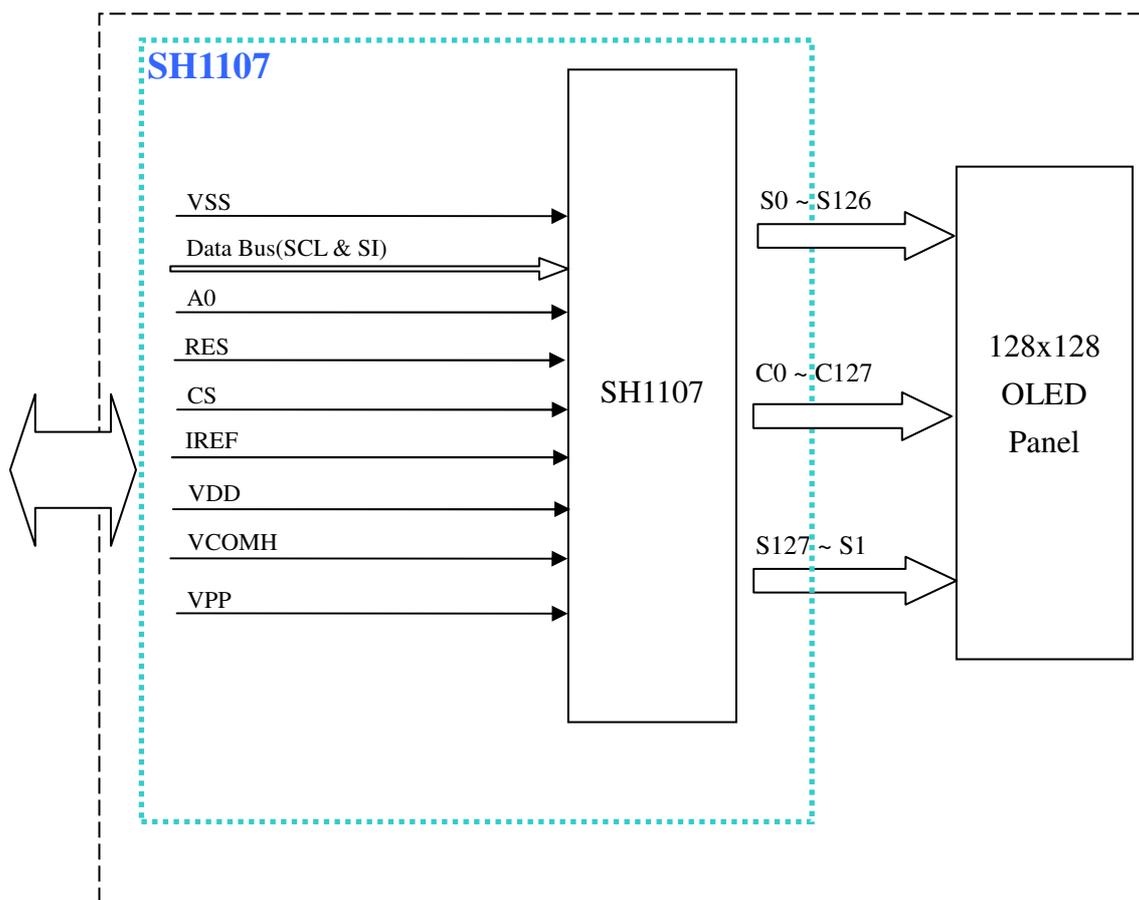
128x128 OLED Panel

RiTdisplay 128X128 OLED Module

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APPLICATION CIRCUIT
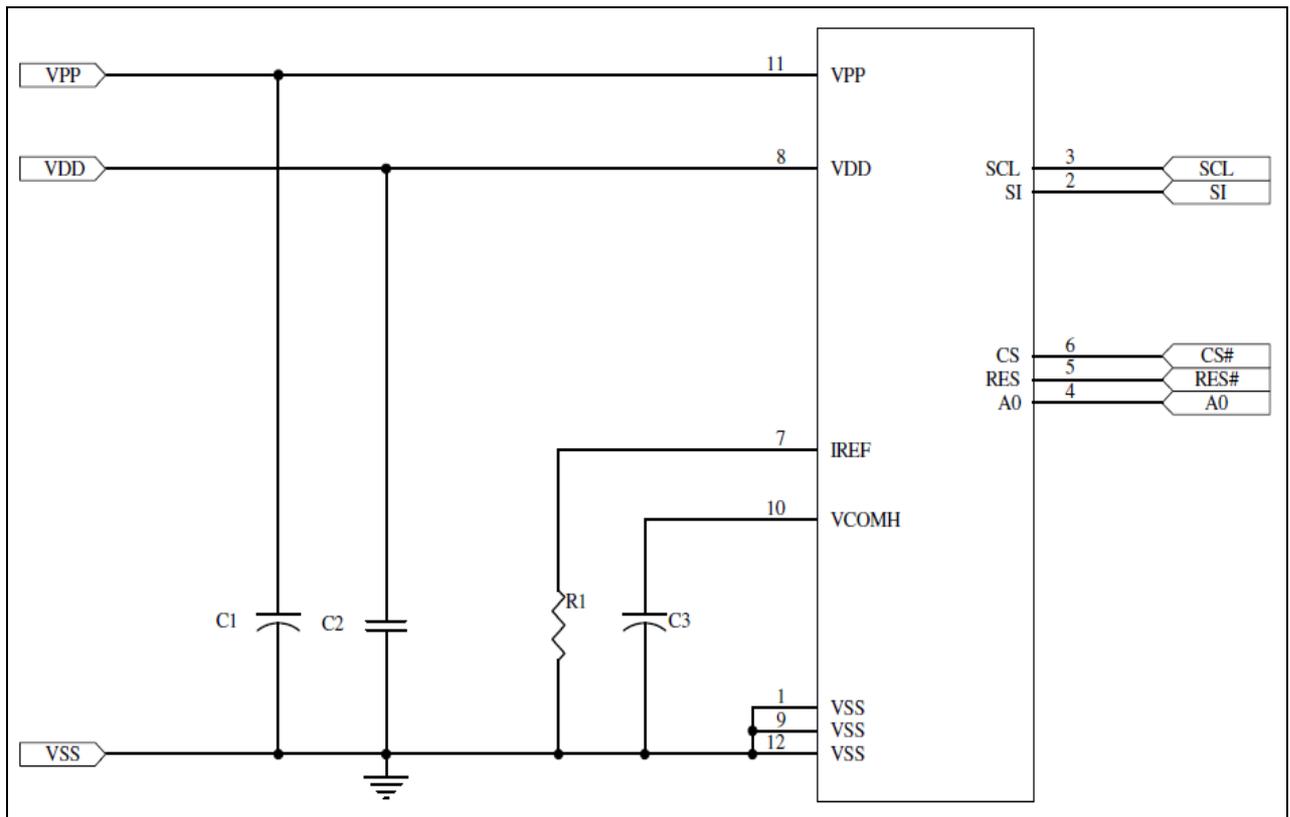
Recommended components：

C1：4.7uF/16V(0805)

C2：1uF/6.3V(0603)

C3：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

R1：1M ohm 1%(0603)

This circuit is for 4-wire SPI interface.

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DC-DC application circuit for OLED module(For External DC/DC)
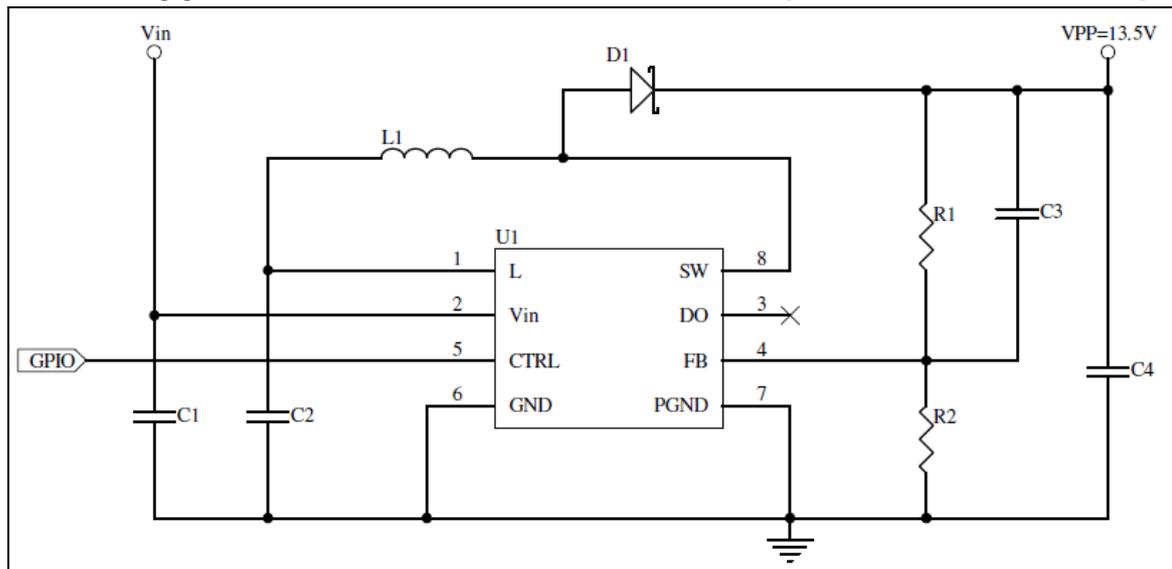
Recommend components:

The C1: 0.1uF/6.3V.

The C2: 4.7 uF/6.3V.

The C3: 22pF/16V.

The C4: 4.7uF/25V Tantalum type capacitor.

The R1: 1.2M ohm1%.

The R2: 120K ohm1%.

The D1: SCHOTTY DIODE.

The L1: 10uH.

The U1: TPS61045

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

PIN NO.	PIN NAME	DESCRIPTION	Setting at each interface		
			8080 parallel	SPI	IIC
1	VSS	Ground pin.			
2	SI	When the serial interface is selected, then D0 serves as the serial clock input pin (SCL) and D1 serves as the serial data input pin (SI).	NA	SI	NA
3	SCL		NA	SCL	NA
4	A0	This is the Data/Command control pin that determines whether the data bits are data or a command. In I^{2}C interface, this pin serves as SA0 to distinguish the different address of OLED driver.	NA	A0	NA
5	RES	This is a reset signal input pin. When RES is set to "L", the settings are initialized.	NA	RES#	NA
6	CS	This pin is the chip select input. When CS = "L", then the chip select becomes active, and data/command I/O is enabled.	NA	CS#	NA
7	IREF	This is a segment current reference pin. A resistor should be connected between this pin and VSS.			
8	VDD	Power supply for logic and input/output.			
9	VSS	Ground pin.			
10	VCOMH	This is voltage output high level for common signals. A capacitor should be connected between this pin and VSS.			
11	VPP	Power supply for panel driving voltage.			
12	VSS	Ground pin.			

Note

(1) Low is connected to VSS

(2) High is connected to VDD

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Application Initial Setting

/*128x128 OLED driver program*/

/* The more detail of SPI sequence please refer to the SH1107 datasheet */

```
void initial(void)
{
comm_out(0xae);//Display OFF

comm_out(0x20);//Page addressing mode

comm_out(0x81);//Set Contrast Control
comm_out(0x7f);//For VPP:13.5V

comm_out(0xa0);//Set Segment Re-map

comm_out(0xa4);//Set Entire Display OFF/ON

comm_out(0xa6);//Set Normal/Reverse Display

comm_out(0xc0);//Set Common Output Scan Direction

comm_out(0xd5);//Set Display Clock Divide Ratio/Oscillator Frequency
comm_out(0x50);

comm_out(0xd9);//Set Dis-charge/Pre-charge Period
comm_out(0x22);

comm_out(0xdb);//Set VCOMH Deselect Level
comm_out(0x3f);

comm_out(0xa8);//Multiplex Ration Mode Set
comm_out(0x7f);

comm_out(0xad);// Set DC-DC Setting
comm_out(0x80);
```

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```
comm_out(0xd3);//Set Display Offset
comm_out(0x00);


comm_out(0xdc);//Set Display Start Line
comm_out(0x00);


cleanDDR (); //Clear the whole DDRAM


comm_out(0xaf);//Set Display ON


}
```

```c
void cleanDDR(void)
{
int i,j;
for(i=0;i<16;i++)
    {
       comm_out(0xb0+i);
       comm_out(0x00);
       comm_out(0x10)
       for(j=0;j<128;j++)
       {
       data_out(0x00);
       }
    }
}
```

After initial the driver IC, user can display all pixels on.

```c
void show_data(void)
{
int i,j;
for(i=0;i<16;i++)
    {
       comm_out(0xb0+i);
       comm_out(0x00);
       comm_out(0x10);
       for(j=0;j<128;j++)
       {
       data_out(0xff);
       }
    }
}
```

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Graphic Display Data RAM (GDDRAM)

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 X 128 bits.

For mechanical flexibility, re-mapping on segment and the direction of common outputs can be selected by software.

Figure 10 （a） RAM map example: ADC=0(POR)

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Figure 10 (b) RAM map example: ADC=1 (Seg remap)

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POWER ON / OFF SEQUENCE

External power is being used immediately after turning on the power:

Power On

```
┌─────────────────────────────────┐
│ VDD is off                      │
│ External power VPP is off       │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Turn on the VDD1 and VPP power, │
│ keep the  RES pin="L"(>10us)    │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Release the reset state (RES pin="H" ) │
│ Reset timing depends on SH1107 data sheet │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Initialized state(Default)      │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Set up initial code (user setup)│
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Clear internal RAM to "00H"     │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ Set display on: AFH             │
└─────────────────────────────────┘
              │  Wait 100ms
              ▼
┌─────────────────────────────────┐
│ Send display data               │
└─────────────────────────────────┘
```

Power On sequence：

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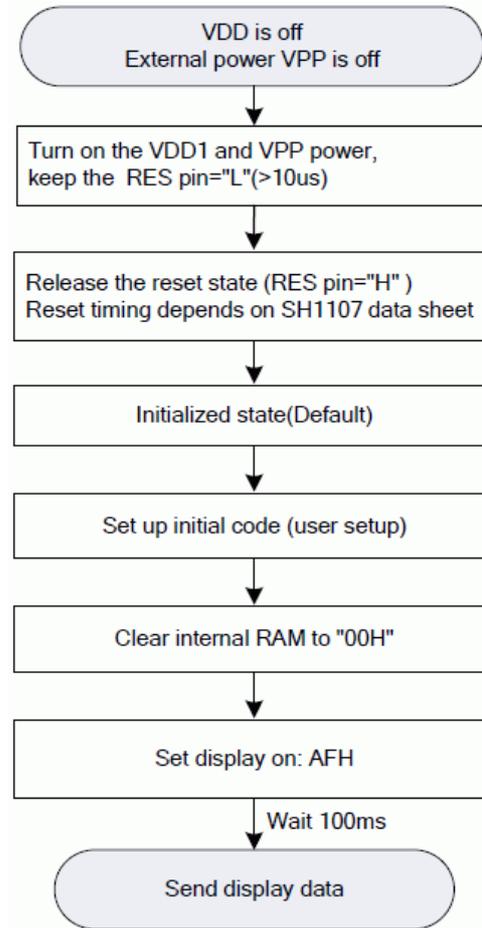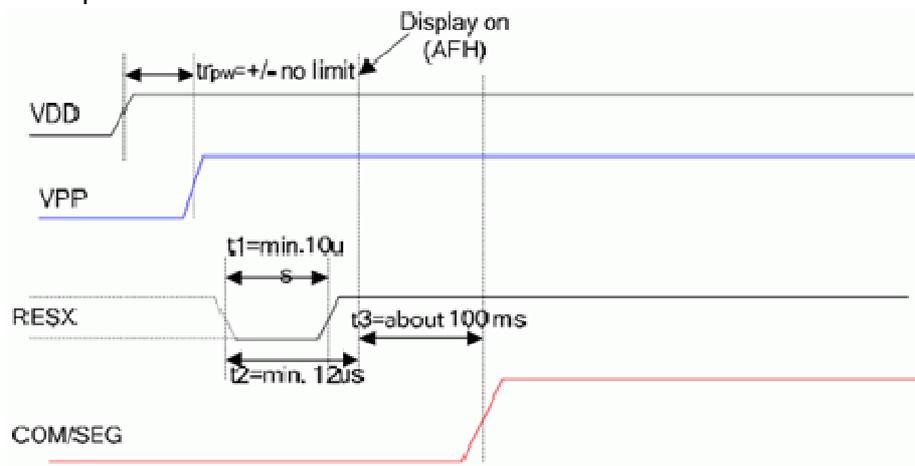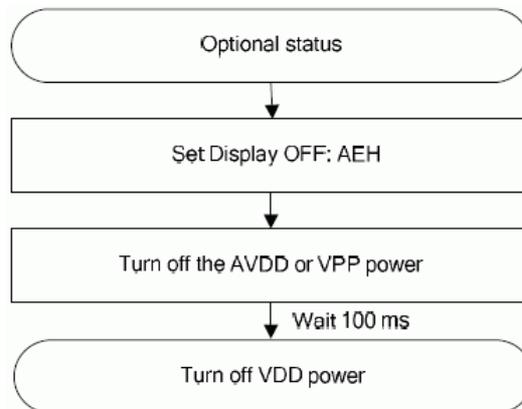
Power Off

Power Off sequence：
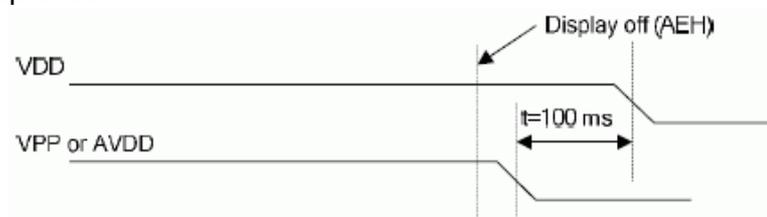
Note：There will be no damages to the display module if the power sequences are not met.

Thank You

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