P43901

64x128 White OLED
Application Notes

(for IIC Interface)

Revision History

Version	REVISION DESCRIPTION
X01	First release
X02	Modify Power ON and OFF sequence(Page 9)

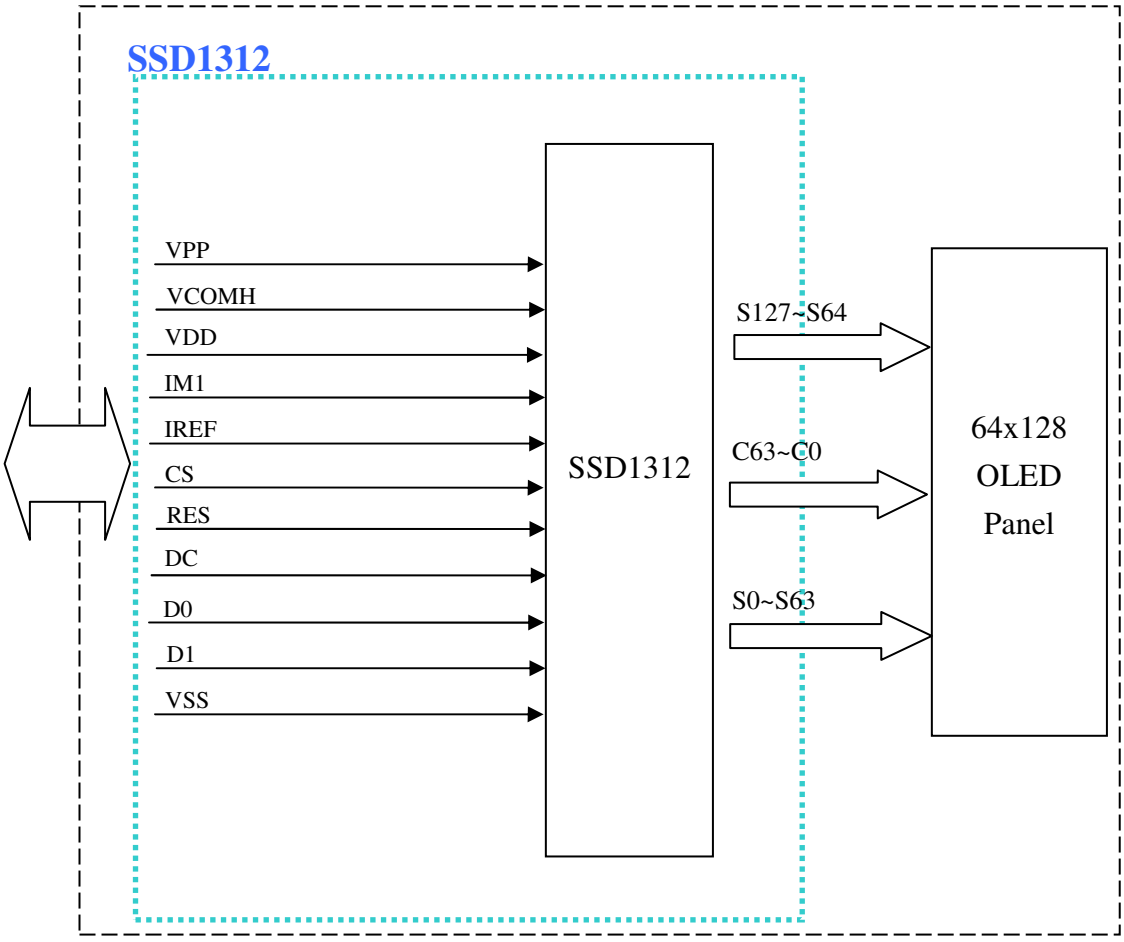
DESCRIPTION

P43901 is a 64x128 dot matrix White passive OLED module with controller for many compact portable applications.

FEATURE

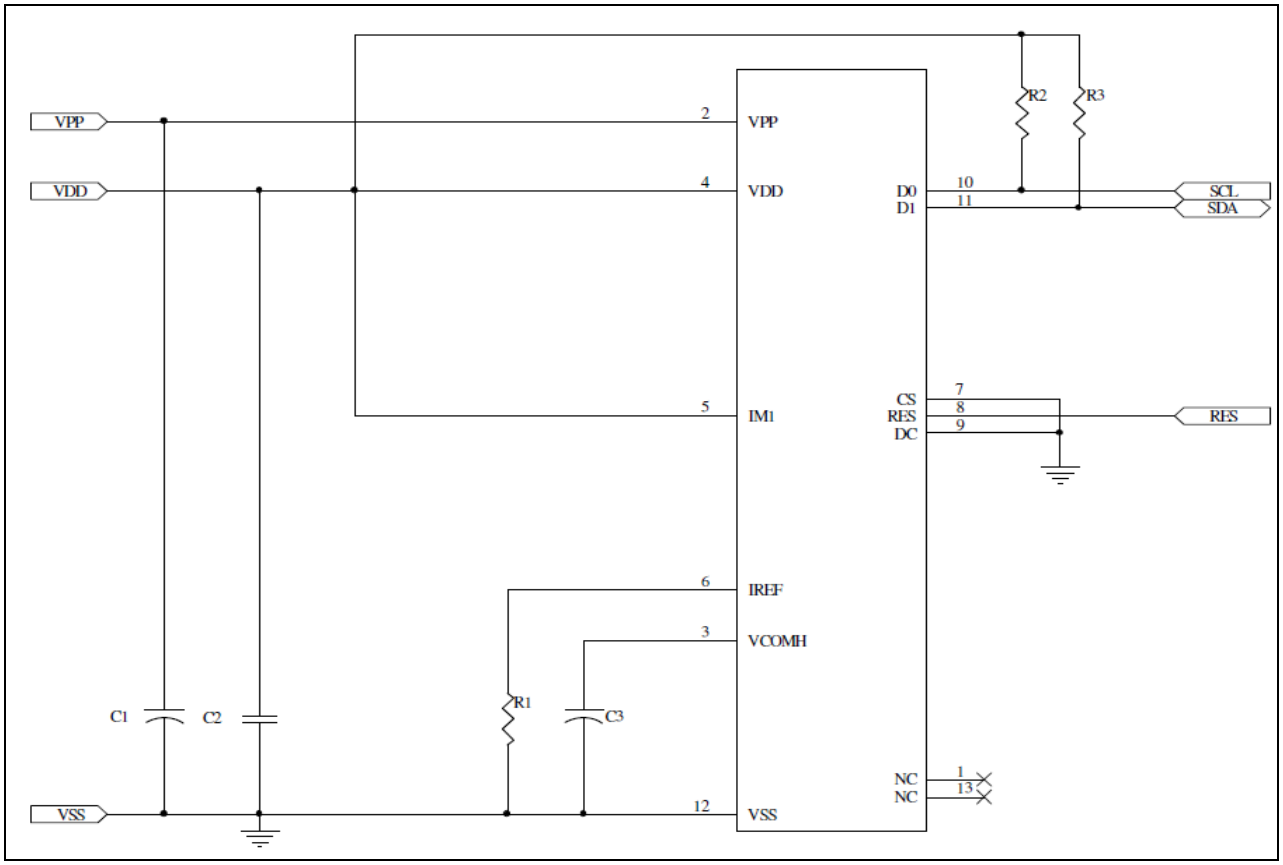
- Panel matrix 64x128.
- Driver IC: SSD1312.
- VPP=9V.
- VDD = 1.65V ~ 3.5V.
- Embedded 128 x 64 bit SRAM display buffer.
- 4 wire Serial Peripheral Interface, I^2C Interface.
- Screen saving continuous scrolling function in both horizontal and vertical
- direction.

FUNCTION BLOCK DIAGRAM



RiTdisplay 64X128 OLED Module

APPLICATION CIRCUIT



Recommend components:

C1: 4.7uF/16V(0805)

C2: 1uF/16V(0603)

C3：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

R1: 560K ohm (0603) 1%

R2, R3: 10K ohm(0603)

This circuit is for I^2C interface.

Note:

1.The R1 and R2 value should be fine tune by customer.

PIN ASSIGNMENTS

PIN No.	PIN Name.	DESCRIPTION	Setting at each interface		
			8080 parallel	SPI	IIC
1	NC	No connection.			
2	VPP	Power supply for panel driving voltage.			
3	VCOMH	This is voltage output high level for common signals. A capacitor should be connected between this pin and VSS.			
4	VDD	Power supply for logic and input/output.			
5	IM1	Interface mode select pin.	NA	Low	High
6	IREF	This is a segment current reference pin. A resistor should be connected between this pin and VSS.			
7	CS	This pin is the chip select input connecting to the MCU.	NA	CS#	Low
8	RES	This pin is reset signal input. When the pin is pulled Low, initialization of the chip is executed.	NA	RES#	RES#
9	DC	This pin is Data/Command control pin connecting to the MCU.	NA	D/C#	SA0
10	D0	When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN. When I^2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.	NA	SCLK	SCL
11	D1		NA	SDIN	SDA
12	VSS	Ground pin.			
13	NC	No connection.			

Note

(1) Low is connected to VSS

(2) High is connected to VDD

Application Initial Setting

```
/*64x128 OLED driver program*/
/* The more detail of I2C sequence please refer the SSD1312 datasheet */
//Slave Address:0x78

void initial(void)
{
comm_out(0xae);//Set Display OFF

comm_out(0xa8);//Set Multiplex Ratio
comm_out(0x3f);//

comm_out(0xad);//External or Internal IREF Selection
comm_out(0x40);

comm_out(0xd3);//Set Display Offset
comm_out(0x00);

comm_out(0xc8);//Set COM Output Scan Direction

comm_out(0xa0);//Set Segment Remap

comm_out(0xa6);//Set Normal Display

comm_out(0x40);//Set Display Start Line

comm_out(0xa4);//Entire Display ON/Off

comm_out(0x81);//Set Contrast Control
comm_out(0x57);//For VPP:9V

comm_out(0xd9);//Set Pre-charge Period
comm_out(0x42);

comm_out(0xd5);//Set Display Clock Divide Ratio/Oscillator Frequency
comm_out(0x90);
```

```
comm_out(0xda);//Set SEG Pins Hardware Configuration
comm_out(0x10);

comm_out(0x20);//Set Memory Addressing Mode
comm_out(0x02);//Page Addressing Mode

comm_out(0xdb);//Set VCOMH Deselect Level
comm_out(0x30);//

comm_out(0x8d);//Charge Pump Setting
comm_out(0x10);//Charge Pump Disable

cleanDDR(); //Clear the whole DDRAM

comm_out(0xaf); //set display ON

}
```

```
void cleanDDR(void)
{
int i,j;
      for(i=0;i<8;i++)
      {
            comm_out (0xb0+i) ; //Set Page
            comm_out (0x00) ; //Lower Column Address
            comm_out (0x10) ; //Higher Column Address
            for (j=0;j<128;j++)
            {
            data_out(0x00);
            }
      }
}
```

After initial the driver IC, user can display all pixels on.

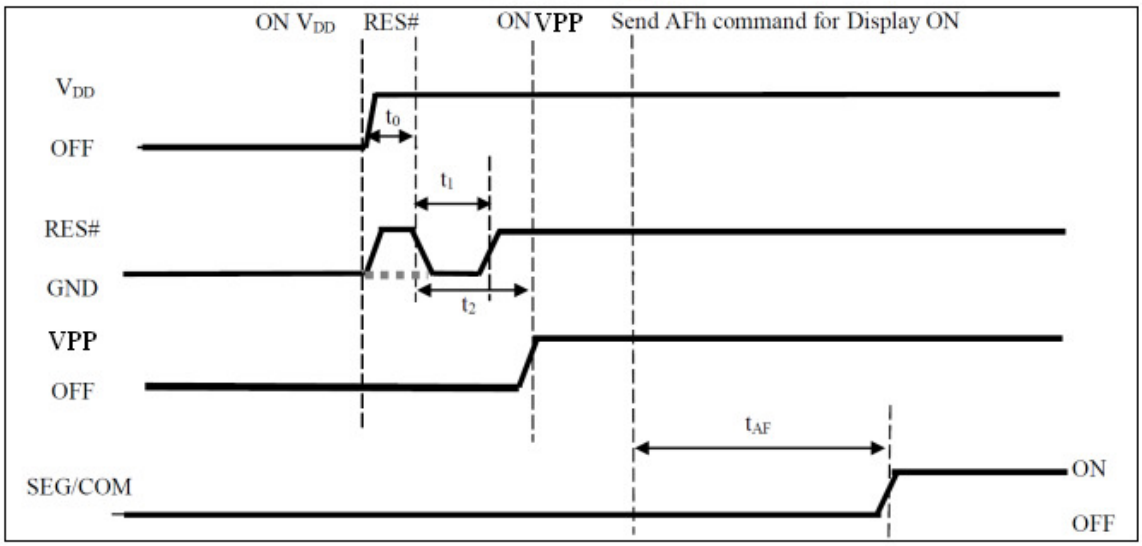
```
void show_data(void)
{
      int i,j;
      for(i=0;i<8;i++)
      {
            comm_out (0xb0+i) ; //Set Page
            comm_out (0x00) ; //Lower Column Address
            comm_out (0x10) ; //Higher Column Address
            for (j=0;j<128;j++)
            {
            data_out(0xff);
            }
      }
}
```

POWER ON AND OFF SEQUENCE

Power ON sequence(External V_{PP}):

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{PP}.[1]
4. After V_{PP} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).

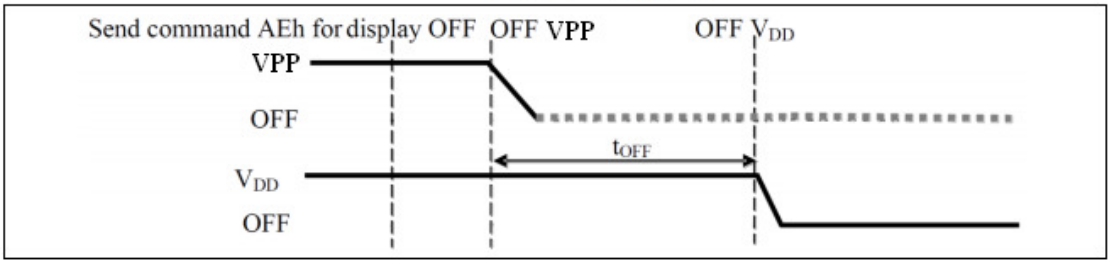
The Power ON Sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{PP}.[1], [2]
3. Power OFF V_{DD} after t_{OFF}. [4] (where Minimum t_{OFF}=80ms, typical t_{OFF}=100ms).

The Power OFF Sequence



Note:

(1)VPP should be kept float (i.e. disable) when it is OFF.

(2) Power Pins (VDD, VPP) can never be pulled to ground under any circumstance.

(3) The register values are reset after t1.

(4) VDD should not be Power OFF before VPP Power OFF.

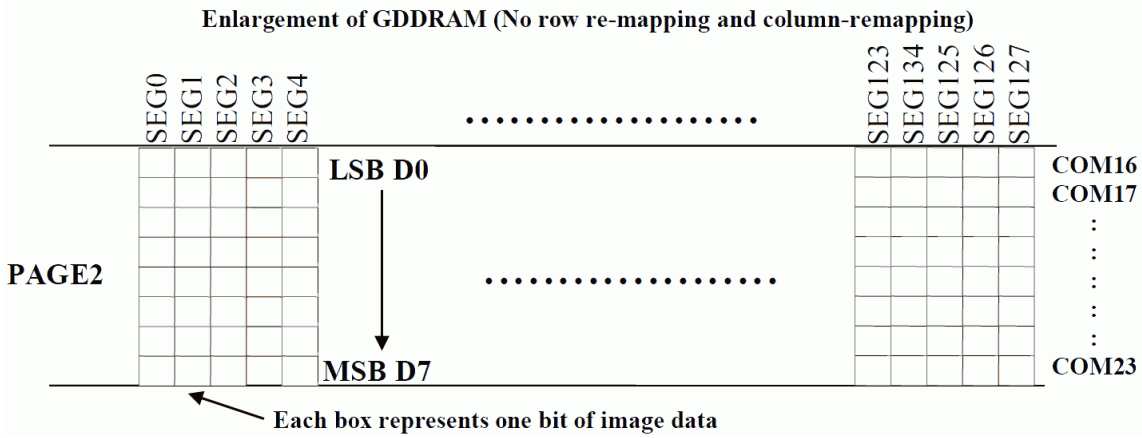
GRAPHIC DISPLAY DATA RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.

GDDRAM pages structure

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

Thank You