

P43601

96x3x64 Full Color Application Notes (for SPI Interface)

Revision History

Version	REVISION DESCRIPTION
X01	First release
X02	Add luminance setting(page 15)

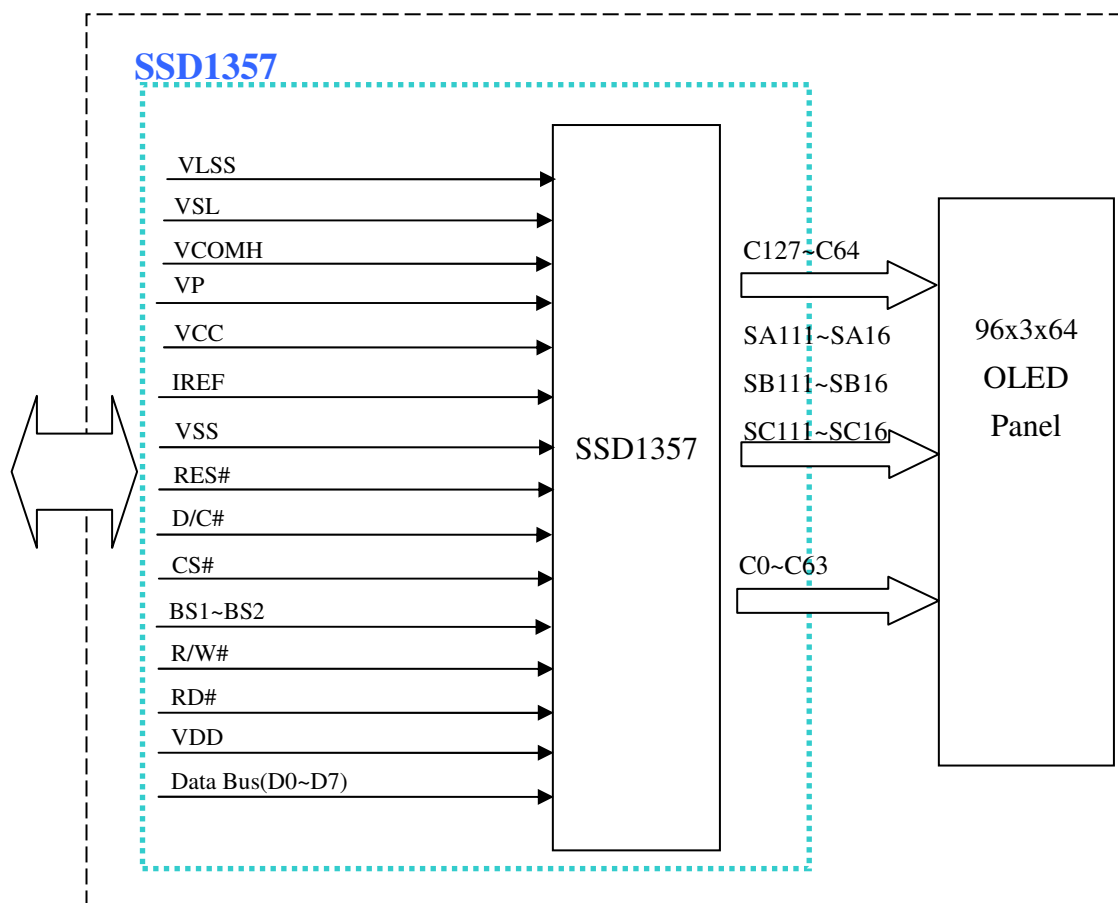
DESCRIPTION

P43601 is a 96x3x64 dot matrix full color passive OLED module with controller for many compact portable applications.

FEATURE

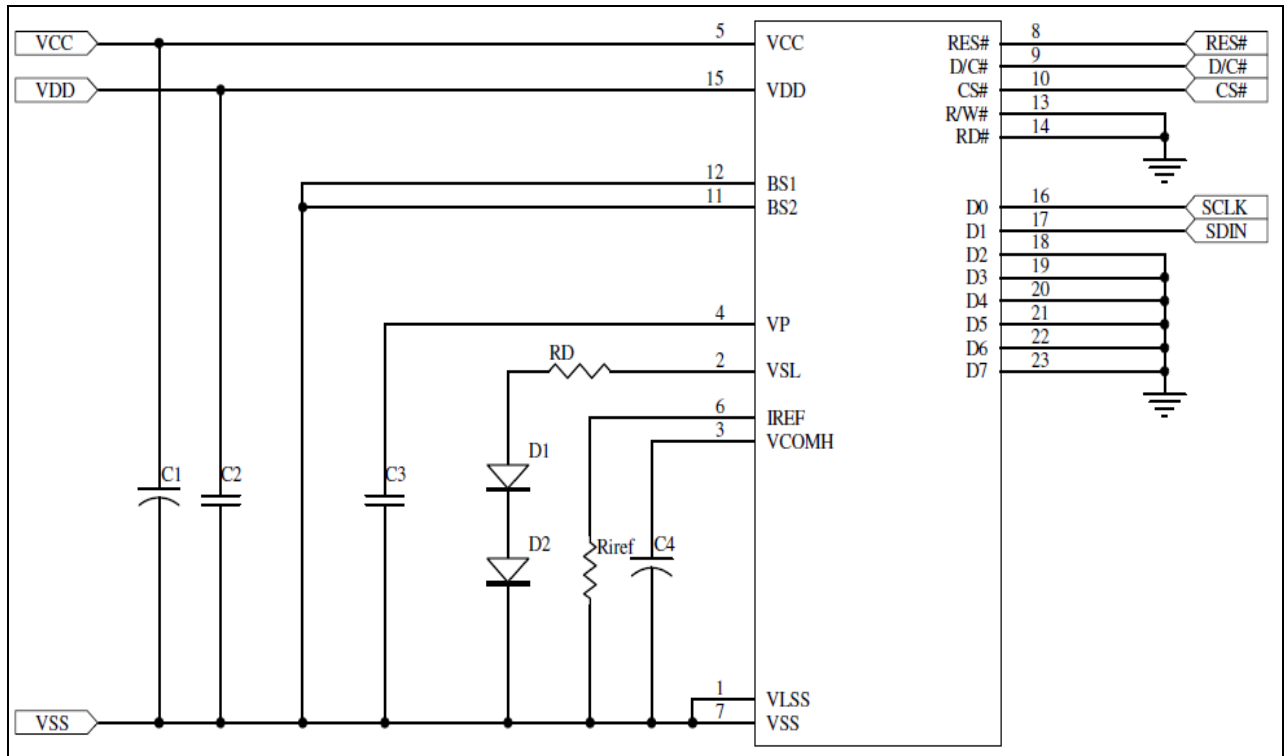
- 96x3x64 dot matrix full color OLED panel.
- Driver IC: SSD1357.
- VCC=13.5V.
- VDD = 1.65V ~ 3.5V.
- 8-bit 6800/8080-series parallel interface,4-wire serial peripheral interface, I²C Interface.
- Screen saving continuous scrolling function in both horizontal and vertical direction.

FUNCTION BLOCK DIAGRAM



RiTdisplay 96X3X64 OLED Module

APPLICATION CIRCUIT



Recommended components :

C1 、 C4 : 4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C2 、 C3 : 1uF/16V(0805)

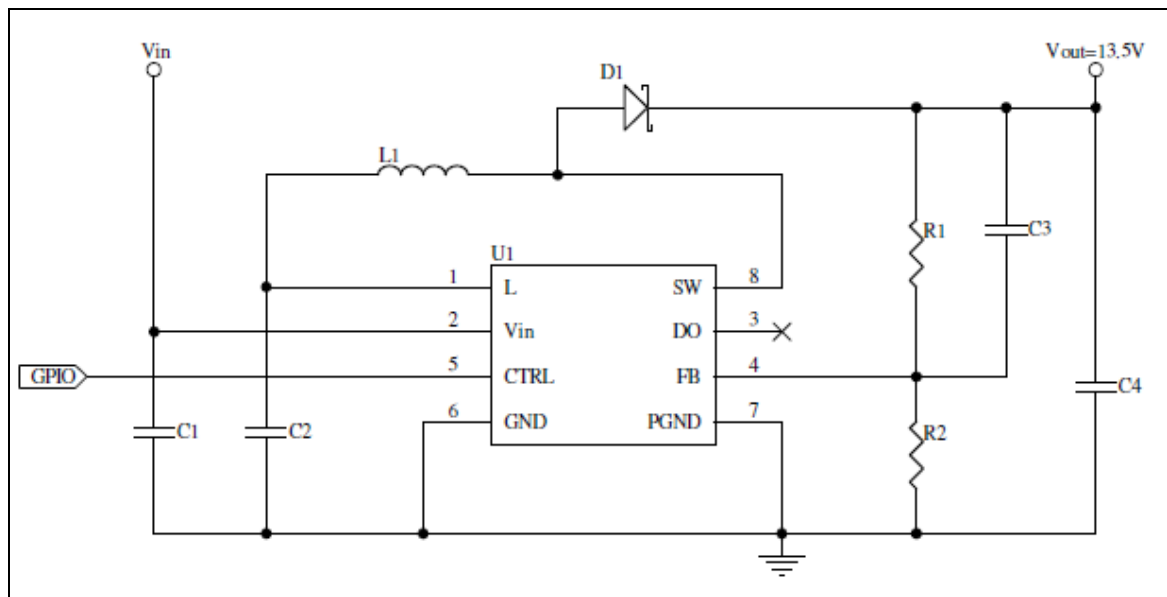
Riref : 1M ohm 1%(0603)

RD : 49.9 ohm 1/4W

D1 、 D2 : RB480K (ROHM)

This circuit is for SPI interface.

DC-DC application circuit for OLED module(For External DC/DC)



Recommend components:

The C1: 0.1uF/25V.

The C2: 4.7uF/25V.

The C3: 22pF/16V.

The C4: 4.7uF/25V Tantalum type capacitor.

The R1: 1.2M ohm1%.

The R2: 120K ohm1%.

The D1: SCHOTTY DIODE.

The L1: 10uH.

The U1: TPS61045.

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION	Setting at each interface		
			16-8080 parallel	SPI	IIC
1	VLSS	Analog system ground pin. It must be connected to external ground.			
2	VSL	This is segment voltage reference pin.			
3	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
4	VP	This pin is the segment pre-charge voltage reference pin.			
5	VCC	Power supply for panel driving voltage.			
6	IREF	This is an internal voltage reference pin. A capacitor should be connected to this pin and VSS.			
7	VSS	Ground pin.			
8	RES#	This is a reset signal input. Low active.	RES#	RES#	RES#
9	D/C#	This pin is Data/Command control pin.	D/C#	D/C#	SA0
10	CS#	This pin is the chip select input. Low active.	CS#	CS#	Low
11	BS2	MCU bus interface selection pins.	High	Low	Low
12	BS1		High	Low	High
13	R/W#	This pin is read / write control input pin connecting to the MCU interface.	WR#	Low	Low
14	RD#	This pin is MCU interface input.	RD#	Low	Low
15	VDD	Power supply pin for core logic operation. A capacitor should be connected between this pin and VSS.			
16	D0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie Low. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN. When I ² C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.	D0	SCLK	SCL
17	D1		D1	SDIN	SDA _{IN}
18	D2		D2	Low	SDA _{OUT}
19	D3		D3	Low	Low
20	D4		D4	Low	Low
21	D5		D5	Low	Low
22	D6		D6	Low	Low
23	D7		D7	Low	Low

Note

(1) Low is connected to VSS

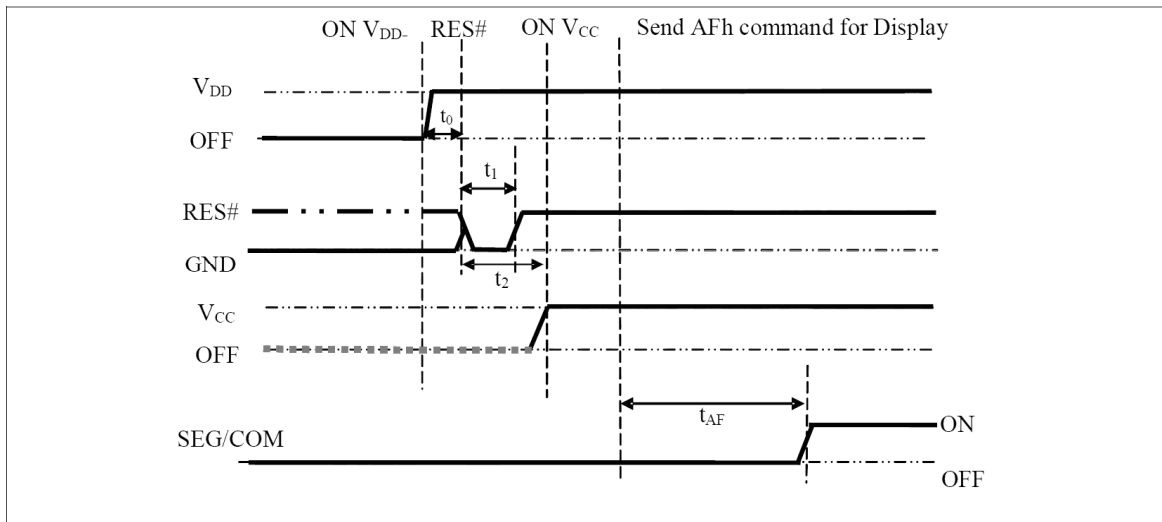
(2) High is connected to VDD

Power ON / OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1357.

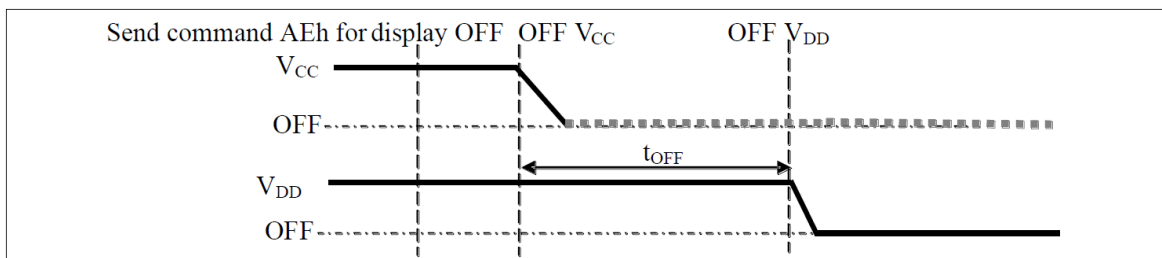
Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).
5. After V_{DD} become stable, wait for at least 300ms to send command.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Power OFF V_{DD} after t_{OFF} .⁽⁴⁾ (where Minimum t_{OFF} =80ms, typical t_{OFF} =100ms)



Note:

- (1) V_{CC} should be kept float (i.e. disable) when it is OFF.
- (2) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.
- (3) The register values are reset after t_1 .
- (4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x16bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 16-bit data. Sub-pixels for color A, C have 5 bits and B have 6 bits. The arrangement of data pixel in graphic display data RAM is shown figures.

65k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	Remapped	0			1			2	126	127		
Color	A	B	C	A	B	C	A	C	A	B	C		
Common Address	Data format	B5	C4	A4	B5	C4	A4	C4	A4	B5	C4		
	A4	B4	C4	A4	B4	C4	A4	C4	A4	B4	C4		
	A3	B3	C3	A3	B3	C3	A3	C3	A3	B3	C3		
	A2	B2	C2	A2	B2	C2	A2	C2	A2	B2	C2		
	A1	B1	C1	A1	B1	C1	A1	C1	A1	B1	C1		
Normal	Remapped	A0	B0	C0	A0	B0	C0	A0	C0	A0	B0	C0	
0	127	5	6	5	5	6	5	5	5	5	6	5	
1	126	5	6	5	5	6	5	5	5	5	6	5	
2	125	5	6	5	5	6	5	5	5	5	6	5	
3	124	5	6	5	5	6	5	5	5	5	6	5	
4	123	5	6	5	5	6	5	5	5	5	6	5	
5	122	5	6	5	5	6	5	5	5	5	6	5	
6	121	5	6	5	5	6	5	5	5	5	6	5	
7	120	5	6	no. of bits in this cell			5	5	5	5	6	5	
:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	
123	4	5	6	5	5	6	5	5	5	5	6	5	
124	3	5	6	5	5	6	5	5	5	5	6	5	
125	2	5	6	5	5	6	5	5	5	5	6	5	
126	1	5	6	5	5	6	5	5	5	5	6	5	
127	0	5	6	5	5	6	5	5	5	5	6	5	

Common output
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
:
:
:
:
:
COM124
COM125
COM126
COM127

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	SC126	SA127	SB127	SC127
------------	-----	-----	-----	-----	-----	-----	-----	-------	-------	-------	-------	-------	-------

Application Initial Setting

```
/*96x3x64 OLED driver program */
/* The more detail of SPI sequence please refer the SSD1357 datasheet */
void initial(void)
{
comm_out(0xfd);//Set Command Lock
data_out(0x12);

comm_out(0xae);//Display off

comm_out(0xa0);//Set Re-map/Color Depth(Display RAM to Panel)
data_out(0x42);
data_out(0x10);

comm_out(0xa1);//Set Display Start Line
data_out(0x00);

comm_out(0xa2);//Set Display Offset
data_out(0x00);

comm_out(0xa6);//Reset to normal display

comm_out(0xb1);//Set Reset(Phase 1)/Pre-charge(Phase 2)period
data_out(0x84);

comm_out(0xb3);//Front Clock Divider(DivSet)/Oscillator Frequency
data_out(0x81);

comm_out(0xb6);//Set Second Precharge Period
data_out(0x08);

comm_out(0xbb);//Set Pre-charge voltage
data_out(0x1e);

comm_out(0xbe);//Set VCOMH Voltage
data_out(0x07);//
```

```
comm_out(0xc1); //Set Contrast Current for Color A,B,C  
data_out(0x20);  
data_out(0x17);  
data_out(0x22);
```

```
comm_out(0xc7); //Master Contrast Current Control  
data_out(0x0f); The value is for VCC=13.5V
```

```
comm_out(0xca); //Set MUX Ratio  
data_out(0x7f); //
```

```
clearDDR(); //Clear the whole DDRAM
```

```
comm_out(0xaf); //Display on  
}
```

```
void clearDDR(void)
{
    int i,j;
    comm_out(0x15);
    data_out(0x00);
    data_out(0x7f);
    comm_out(0x75);
    data_out(0x00);
    data_out(0x7f);
    comm_out(0x5c);
    for(i=0;i<128;i++)
    {
        for(j=0;j<128;j++)
        {
            data_out(0x00);
            data_out(0x00);
        }
    }
}

write_red_data(void) // display all red pixels on
{
    int i,j;
    comm_out(0x15); //Set SEG Address.
    data_out(0x10);
    data_out(0x6f);
    comm_out(0x75); // Set COM Address.
    data_out(0x00);
    data_out(0x3f);
    comm_out(0x5c);
    for(i=0;i<64;i++)
    {
        for(j=0;j<96;j++)
        {
            data_out(0xf8);
            data_out(0x00);
        }
    }
}
```

```
}  
  
write_green_data(void) // display all green pixels on  
{  
    int i,j;  
    comm_out(0x15); //Set SEG Address.  
    data_out(0x10);  
    data_out(0x6f);  
    comm_out(0x75); // Set COM Address.  
    data_out(0x00);  
    data_out(0x3f);  
    comm_out(0x5c);  
    for(i=0;i<64;i++)  
        {  
            for(j=0;j<96;j++)  
                {  
                    data_out(0x07);  
                    data_out(0xe0);  
                }  
        }  
}  
  
write_blue_data(void) // display all blue pixels on  
{  
    int i,j;  
    comm_out(0x15); //Set SEG Address.  
    data_out(0x10);  
    data_out(0x6f);  
    comm_out(0x75); // Set COM Address.  
    data_out(0x00);  
    data_out(0x3f);  
    comm_out(0x5c);  
    for(i=0;i<64;i++)  
        {  
            for(j=0;j<96;j++)  
                {  
                    data_out(0x00);  
                    data_out(0x1f);  
                }  
        }  
}
```

```
    }  
  }  
}
```

`write_white_data(void)` // **display all pixels on(Red, Green and Blue)**

```
{  
  int i,j;  
  comm_out(0x15); //Set SEG Address.  
  data_out(0x10);  
  data_out(0x6f);  
  comm_out(0x75); // Set COM Address.  
  data_out(0x00);  
  data_out(0x3f);  
  comm_out(0x5c);  
  for(i=0;i<64;i++)  
  {  
    for(j=0;j<96;j++)  
    {  
      data_out(0xff);  
      data_out(0xff);  
    }  
  }  
}
```

For 20 cd/m² setting, user could follow the below setting.

```
Brightness_mode1 (void);  
{  
comm_out(0xc7); //Master Contrast Current  
data_out(0x01);  
comm_out(0xc1); //Set contrast level for R,G,B  
data_out(0x26); //Blue contrast set  
data_out(0x15); //Green contrast set  
data_out(0x21); //Red contrast set  
}
```

For 50 cd/m² setting, user could follow the below setting.

```
Brightness_mode2 (void);  
{  
comm_out(0xc7); //Master Contrast Current  
data_out(0x04);  
comm_out(0xc1); //Contrast Current  
data_out(0x27); //B  
data_out(0x18); //G  
data_out(0x22); //R  
}
```

For 80 cd/m² setting, user could follow the below setting.

```
Brightness_mode3 (void);  
{  
comm_out(0xc7); //Master Contrast Current  
data_out(0x06);  
comm_out(0xc1); //Contrast Current  
data_out(0x2d); //B  
data_out(0x20); //G  
data_out(0x2a); //R  
}
```

For 100 cd/m²

setting, user could follow the below setting.

```
Brightness_mode4 (void);  
{  
comm_out(0xc7);//Master Contrast Current  
data_out(0x0c);  
comm_out(0xc1);//Contrast Current  
data_out(0x20);//B  
data_out(0x17);//G  
data_out(0x20);//R  
}
```

For 120 cd/m² setting, user could follow the below setting.

```
Brightness_mode5 (void);  
{  
comm_out(0xc7);//Master Contrast Current  
data_out(0x0f);  
comm_out(0xc1);//Contrast Current  
data_out(0x20);//B  
data_out(0x17);//G  
data_out(0x22);//R  
}
```

For 160 cd/m² setting, user could follow the below setting.

```
Brightness_mode5 (void);  
{  
comm_out(0xc7);//Master Contrast Current  
data_out(0x0f);  
comm_out(0xc1);//Contrast Current  
data_out(0x2c);//B  
data_out(0x20);//G  
data_out(0x3a);//R  
}
```

Thank You

