P43401

176x3x176 Full Color
Application Notes
(For 4 wire SPI Interface)

Revision History

Version	Content
X01	First release(For 4 wire SPI Interface)
X02	Modify brightness Setting(Page 11 / Page 17~18)

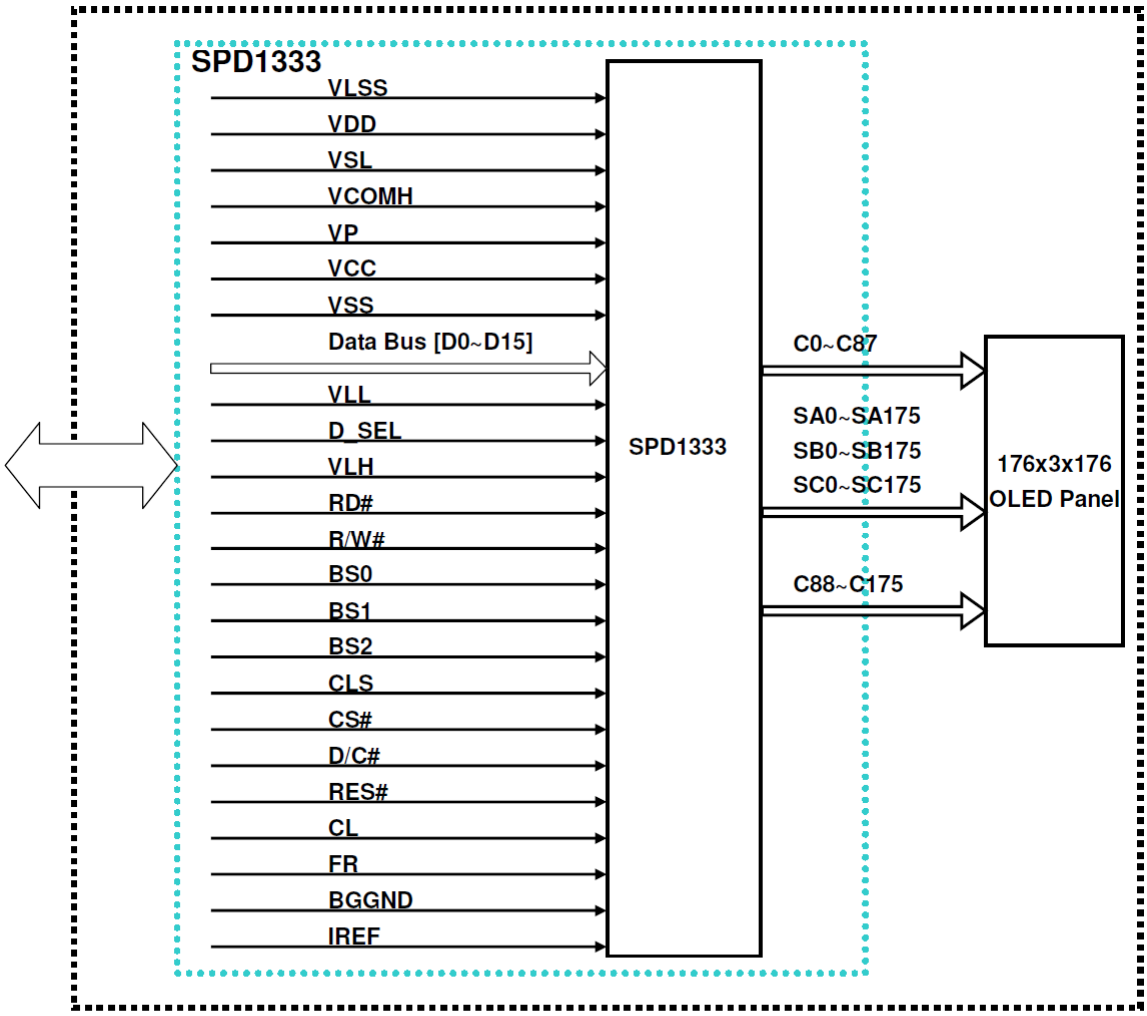
DESCRIPTION

P43401 is a 176x3x176 full color passive OLED module with controller for many compact portable applications.

FEATURE

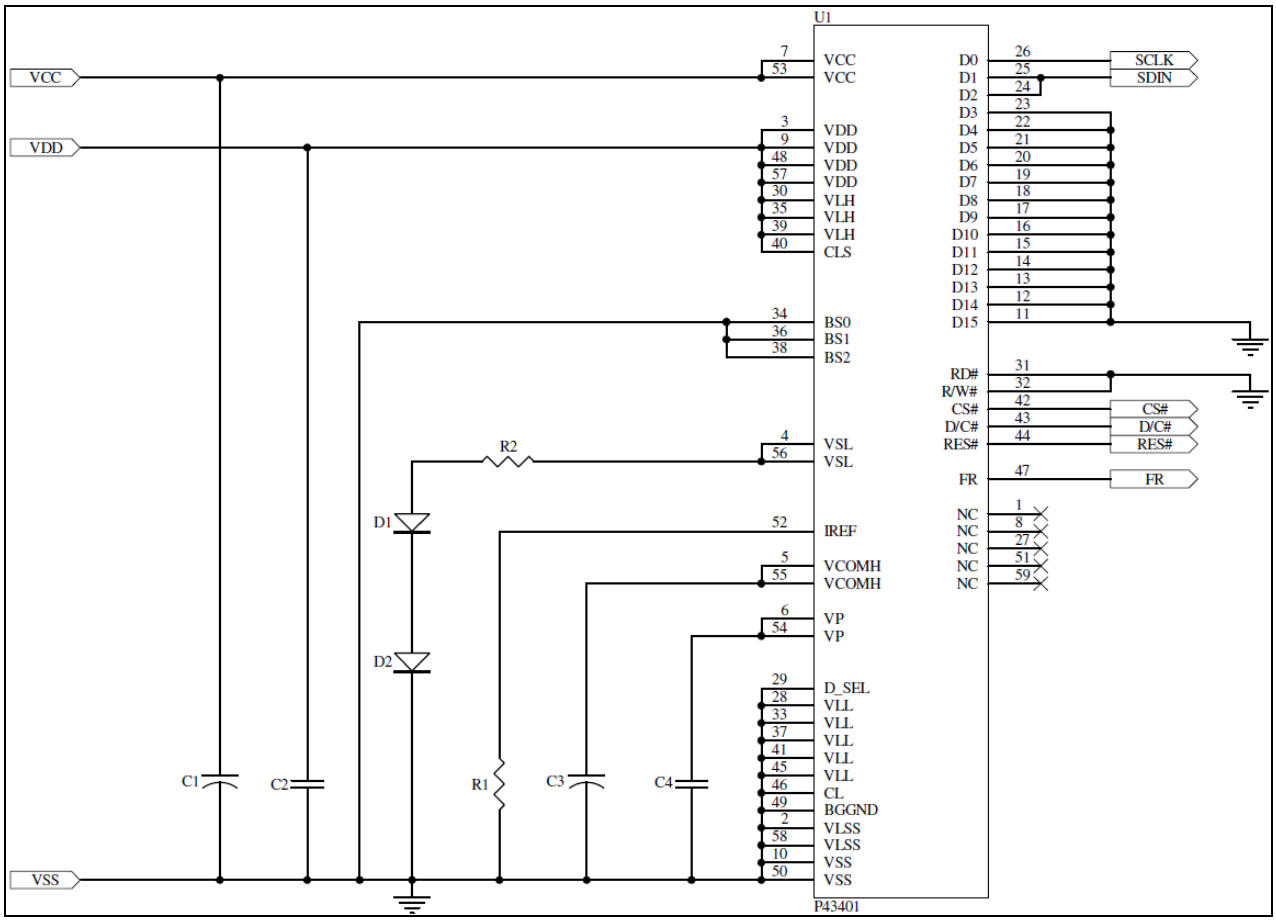
- 176x3x176 dot matrix full color OLED panel.
- Driver IC SPD1333.
- VCC = 17V
- VDD = 1.65V~3.5V
- 8/16 bits 6800/8080-series parallel Interface, 3/4 wire serial peripheral interface.
- Scrolling function.
- Row re-mapping and Column re-mapping.

FUNCTION BLOCK DIAGRAM



RiTdisplay 176X3x176 OLED Module

APPLICATION CIRCUIT



Recommend components:

C1 : 4.7uF/25V(0805)

C3 : 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)

C2, C4 : 1uF/16V(0603)

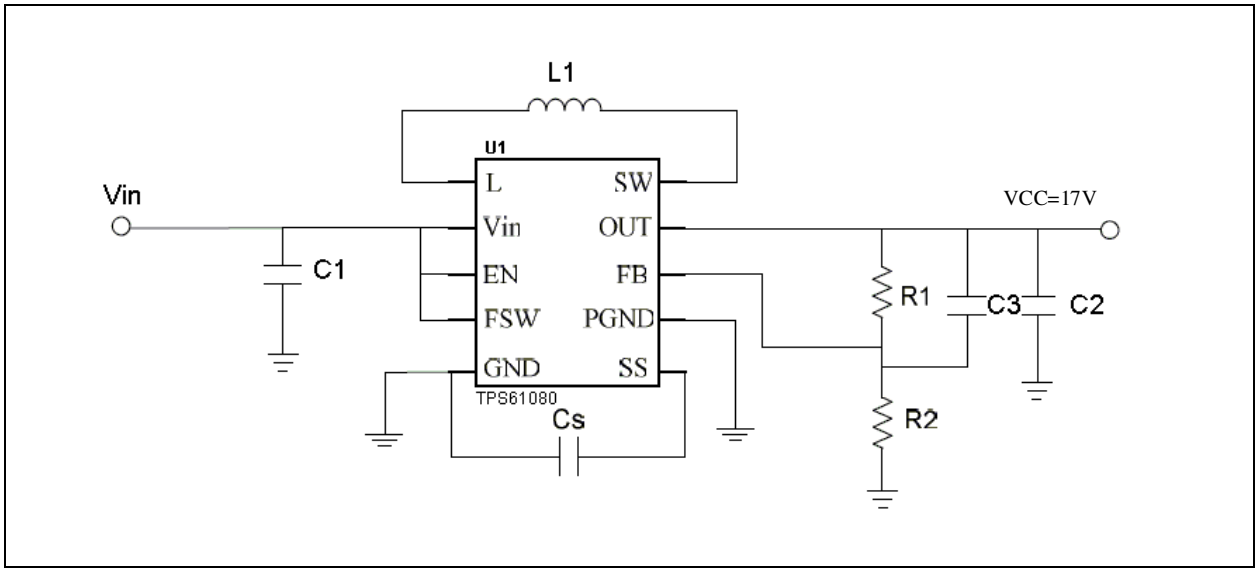
R1: 1M ohm (0603) 1%

R2: 49.9 ohm 1/4W

D1,D2: RB480K (ROHM)

This circuit is for 4 wire SPI interface.

DC-DC application circuit for OLED module



Recommend components:

The C1: 4.7uF/6.3V.

The C2: 4.7 uF/25V Tantalum type capacitor.

The C3: 50pF/16V.

The Cs: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 92K ohm/ 1%.

The L1: 4.7uH.

The U1: TPS61080

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

Pin No.	Pin Name	Description	Setting at each interface		
			8080 16bit parallel	8080 8bit parallel	4 wire SPI
1	NC	No connection.			
2	VLSS	Analog system ground pin.			
3	VDD	Power supply pin for core logic operation.			
4	VSL	This is segment voltage reference pin.			
5	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
6	VP	This pin is the segment pre-charge voltage reference pin.			
7	VCC	Power supply for panel driving voltage.			
8	NC	No connection.			
9	VDD	Power supply pin for core logic operation.			
10	VSS	Ground pin.			
11	D15	These pins are bi-directional data bus connecting to the MCU data bus. When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK.	D15	Tie LOW	Tie LOW
12	D14		D14	Tie LOW	Tie LOW
13	D13		D13	Tie LOW	Tie LOW
14	D12		D12	Tie LOW	Tie LOW
15	D11		D11	Tie LOW	Tie LOW
16	D10		D10	Tie LOW	Tie LOW
17	D9		D9	Tie LOW	Tie LOW
18	D8		D8	Tie LOW	Tie LOW
19	D7		D7	D7	Tie LOW
20	D6		D6	D6	Tie LOW
21	D5		D5	D5	Tie LOW
22	D4		D4	D4	Tie LOW
23	D3		D3	D3	Tie LOW
24	D2		D2	D2	SDIN
25	D1		D1	D1	SDIN

26	D0		D0	D0	SCLK
27	NC	No connection.			
28	VLL	Logic low.			
29	D_SEL	Should be connected to VLL.			
30	VLH	Logic high.			
31	RD#	8080: data read enable pin; 6800:Read/Write enable pin.When serial interface is selected, this pin must be connected to VSS.	RD#	RD#	Tie LOW
32	R/W#	This pin is read / write control input pin connecting to the MCU interface. 8080: data write enable pin; 6800:Read/Write select pin.	R/W#	R/W#	Tie LOW
33	VLL	Logic low.			
34	BS0	MCU bus interface selection pins.	High	Low	Low
35	VLH	Logic high.			
36	BS1	MCU bus interface selection pins.	High	High	Low
37	VLL	Logic low.			
38	BS2	MCU bus interface selection pins.	High	High	Low
39	VLH	Logic high.			
40	CLS	This is internal clock enable pin.			
41	VLL	Logic low.			
42	CS#	This pin is the chip select input. Low active.	CS#	CS#	CS#
43	D/C#	This pin is Data/Command control pin	D/C#	D/C#	D/C#
44	RES#	This is a reset signal input. Low active.			
45	VLL	Logic low.			
46	CL	This is external clock input pin.			
47	FR	This pin outputs RAM write synchronization signal.			
48	VDD	Power supply pin for core logic operation.			
49	BGGND	It must be connected to VSS.			
50	VSS	Ground pin.			
51	NC	No connection.			
52	IREF	This is an internal voltage reference pin. A capacitor should be connected to this pin and VSS.			

53	VCC	Power supply for panel driving voltage.			
54	VP	This pin is the segment pre-charge voltage reference pin.			
55	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
56	VSL	This is segment voltage reference pin.			
57	VDD	Power supply pin for core logic operation.			
58	VLSS	Analog system ground pin.			
59	NC	No connection.			

Note

(1) Low is connected to VSS

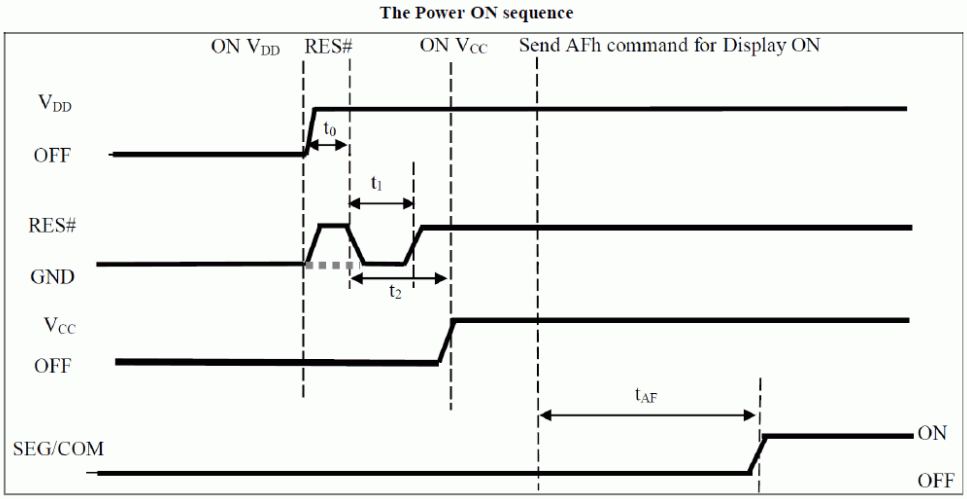
(2) High is connected to VDD

Power ON / OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1333.

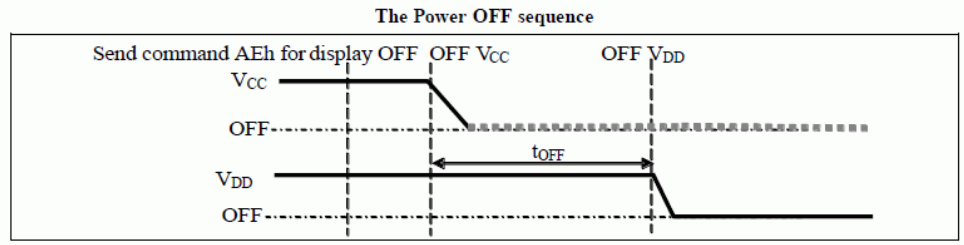
Power ON sequence:

1. Power ON VDD
2. After VDD become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1)[4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON VCC.[1]
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC.[1], [2]
3. Power OFF VDD after t_{OFF}.[4] (where Minimum t_{OFF}=80ms, typical t_{OFF}=100ms)



Note:

(1)V_{CC} should be kept float (i.e. disable) when it is OFF.

(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

(3) The register values are reset after t_1.

(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 176 x 176 x16bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 16-bit data. Sub-pixels for color A, C have 5 bits and B have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below figures.

65k Color Depth Graphic Display Data RAM Structure

Segment	Normal	0			1			2	.....	.....	174	175		
Address	Remapped	175			174			173	.....	.....	1	0		
Color		A	B	C	A	B	C	A			C	A	B	C
Data format			B5			B5			.....	.....			B5	
Common Address		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0
Normal	Remapped													
0	175	5	6	5	5	6	5	5	.....	.....	5	5	6	5
1	174	5	6	5	5	6	5	5	.....	.....	5	5	6	5
2	173	5	6	5	5	6	5	5	.....	.....	5	5	6	5
3	172	5	6	5	5	6	5	5	.....	.....	5	5	6	5
4	171	5	6	5	5	6	5	5	.....	.....	5	5	6	5
5	170	5	6	5	5	6	5	5	.....	.....	5	5	6	5
6	169	5	6	5	5	6	5	5	.....	.....	5	5	6	5
7	168	5	6	no. of bits in this cell			5	5	.....	.....	5	5	6	5
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
171	4	5	6	5	5	6	5	5	.....	.....	5	5	6	5
172	3	5	6	5	5	6	5	5	.....	.....	5	5	6	5
173	2	5	6	5	5	6	5	5	.....	.....	5	5	6	5
174	1	5	6	5	5	6	5	5	.....	.....	5	5	6	5
175	0	5	6	5	5	6	5	5	.....	.....	5	5	6	5

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC174	SA175	SB175	SC175

Common output
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
:
:
:
:
COM172
COM173
COM174
COM175

Application Initial Setting

```
/* 176x3x176 OLED driver program */
/* The more detail of SPI sequence please refer the SSD1333 datasheet */

void initial(void)
{
comm_out(0xfd);//Set Command Lock
data_out(0x12);

comm_out(0xae);//Display off

comm_out(0xa0);//Set Re-map/Color Depth
data_out(0x64);

comm_out(0xa1);//Set Display Start Line
data_out(0x00);

comm_out(0xa2);//Set Display Offset
data_out(0x00);

comm_out(0xa6);//Reset to normal display

comm_out(0xb1);//Set Reset(Phase 1)/Pre-charge(Phase 2)period
data_out(0x24);

comm_out(0xb3);//Front Clock Divider(DivSet)/Oscillator Frequency
data_out(0x80);

comm_out(0xb6);//Set Second Precharge Period
data_out(0x0f);

comm_out(0xbb);//Set Pre-charge voltage
data_out(0x1f);

comm_out(0xbe);//Set VCOMH Voltage
data_out(0x05);
```

```
comm_out(0xc1);//Set Contrast Current for Color A,B,C
data_out(0x003c); // Luminance 80 nits
data_out(0x0039);
data_out(0x0043);

comm_out(0xc7);//Master Contrast Current Control
data_out(0x0f);//VCC=17V

comm_out(0xca);//Set MUX Ratio
data_out(0xaf);

comm_out(0xb8);//gamma LUT
data_out(0x00);//1
data_out(0x02);//2
data_out(0x04);//3
data_out(0x06);//4
data_out(0x07);//5
data_out(0x08);//6
data_out(0x09);//7
data_out(0x0a);//8
data_out(0x0b);//9
data_out(0x0c);//10
data_out(0x0d);//11
data_out(0x0e);//12
data_out(0x10);//13
data_out(0x11);//14
data_out(0x12);//15
data_out(0x14);//16
data_out(0x15);//17
data_out(0x16);//18
data_out(0x18);//19
data_out(0x1a);//20
data_out(0x1b);//21
data_out(0x1d);//22
data_out(0x1f);//23
data_out(0x20);//24
data_out(0x22);//25
data_out(0x24);//26
```

```
data_out(0x26);//27
data_out(0x27);//28
data_out(0x29);//29
data_out(0x2b);//30
data_out(0x2d);//31
data_out(0x2f);//32
data_out(0x31);//33
data_out(0x33);//34
data_out(0x35);//35
data_out(0x37);//36
data_out(0x39);//37
data_out(0x3b);//38
data_out(0x3d);//39
data_out(0x3f);//40
data_out(0x42);//41
data_out(0x44);//42
data_out(0x46);//43
data_out(0x48);//44
data_out(0x4b);//45
data_out(0x4d);//46
data_out(0x50);//47
data_out(0x52);//48
data_out(0x55);//49
data_out(0x57);//50
data_out(0x5a);//51
data_out(0x5b);//52
data_out(0x5f);//53
data_out(0x62);//54
data_out(0x65);//55
data_out(0x67);//56
data_out(0x6a);//57
data_out(0x6d);//58
data_out(0x70);//59
data_out(0x73);//60
data_out(0x76);//61
data_out(0x79);//62
data_out(0x7c);//63
```

```
cleanDDR();                 //Clear the whole DDRAM

comm_out(0xaf);//Display on
}
```

```
void cleanDDR(void)
{
int i,j;
comm_out(0x15);
data_out(0x00);
data_out(0xaf);
comm_out(0x75);
data_out(0x00);
data_out(0xaf);

comm_out(0x5c);

for(i=0;i<176;i++)
 {
  for(j=0;j<176;j++)
  {
  data_out(0x00);
  data_out(0x00);
  }
 }
}

write_red_data(void)
{
int i;
ram _address( );
comm_out(0x5c);

for(i=0;i<176;i++)
 {
  for(j=0;j<176;j++)
  {
  data_out(0xf8);//RED
  data_out(0x00);
  }
 }
}
```

```
write_green_data(void)
{
int i;
ram _address( );
comm_out(0x5c);

for(i=0;i<176;i++)
 {
   for(j=0;j<176;j++)
   {
   data_out(0x07);//GREEN
   data_out(0xe0);
   }
 }
}

write_blue_data(void)
{
int i;
ram _address( );
comm_out(0x5c);

for(i=0;i<176;i++)
 {
   for(j=0;j<176;j++)
   {
   data_out(0x00);//BLUE
   data_out(0x1f);
   }
 }
}

write_white_data(void)
{
int i;
ram _address( );
comm_out(0x5c);
```

```
for(i=0;i<176;i++)
  {
    for(j=0;j<176;j++)
    {
    data_out(0xff); //WHITE
    data_out(0xff);
    }
  }
}

ram _address(void);
{
comm_out(0x15);
data_out(0x00);
data_out(0xaf);
comm_out(0x75);
data_out(0x00);
data_out(0xaf);
}
```

For 80 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode1 (void);
{
comm_out(0xc7);//Master Contrast Current Control
data_out(0x000f);
comm_out(0xc1);//Set Contrast Current for Color A,B,C
data_out(0x003c);
data_out(0x0039);
data_out(0x0043);
}
```

For 70 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode1 (void);
{
comm_out(0xc7);//Master Contrast Current Control
data_out(0x000f);
comm_out(0xc1);//Set Contrast Current for Color A,B,C
data_out(0x0030);
data_out(0x0028);
data_out(0x0039);
}
```

For 50 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode2 (void);
{
comm_out(0xc7);//Master Contrast Current Control
data_out(0x000f);
comm_out(0xc1);//Set Contrast Current for Color A,B,C
data_out(0x001c);
data_out(0x001d);
data_out(0x0029);
}
```

For 30 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode3 (void);
{
comm_out(0xc7);//Master Contrast Current Control
data_out(0x000f);
comm_out(0xc1);//Set Contrast Current for Color A,B,C
```

```
data_out(0x000f);
data_out(0x0012);
data_out(0x001b);
}
```

For 20 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode4 (void);
{
comm_out(0xc7);//Master Contrast Current Control
data_out(0x000f);
comm_out(0xc1);//Set Contrast Current for Color A,B,C
data_out(0x0009);
data_out(0x000e);
data_out(0x0014);
}
```

Thank You