P42502

265x96 White OLED
Application Notes

(for IIC Interface)

Revision History

Version	REVISION DESCRIPTION
X01	First release

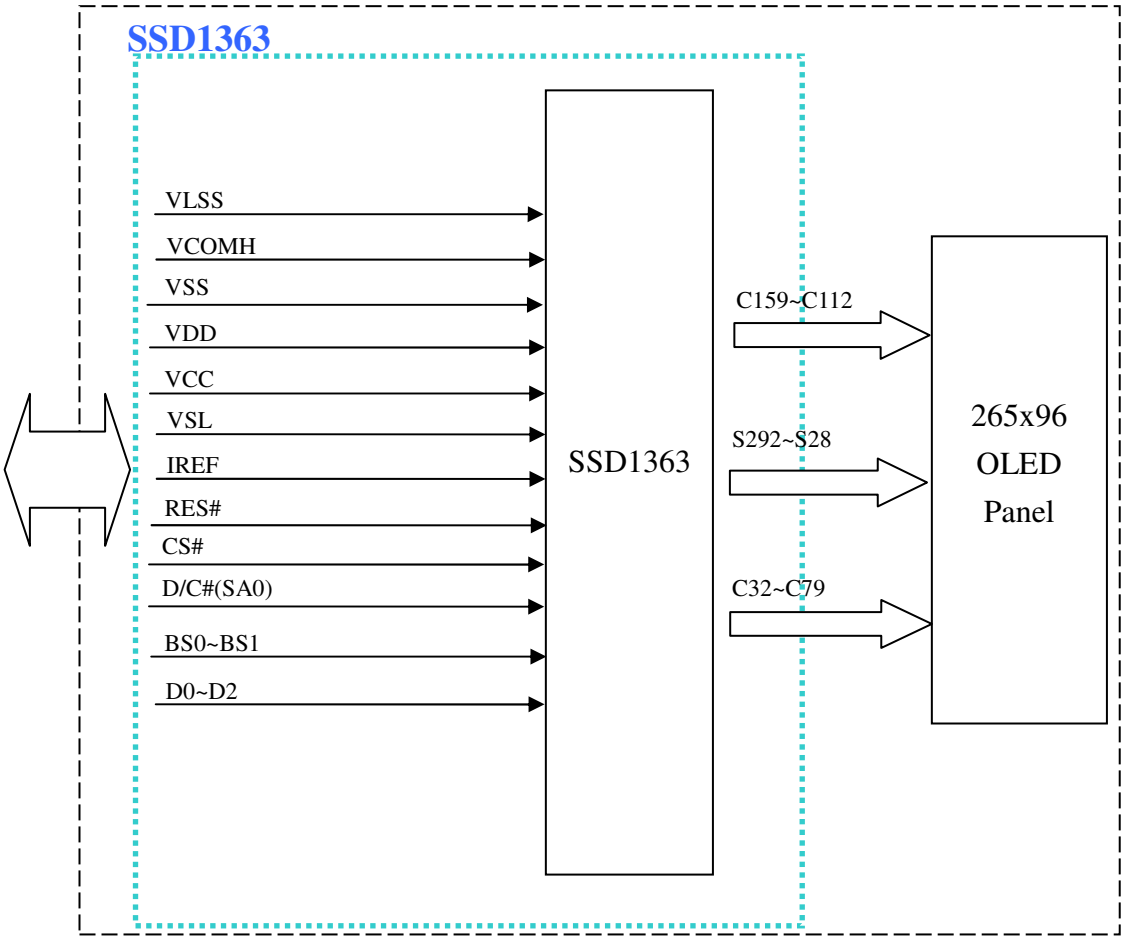
DESCRIPTION

P42502 is a 265x96 dot matrix White passive OLED module with controller for many compact portable applications.

FEATURE

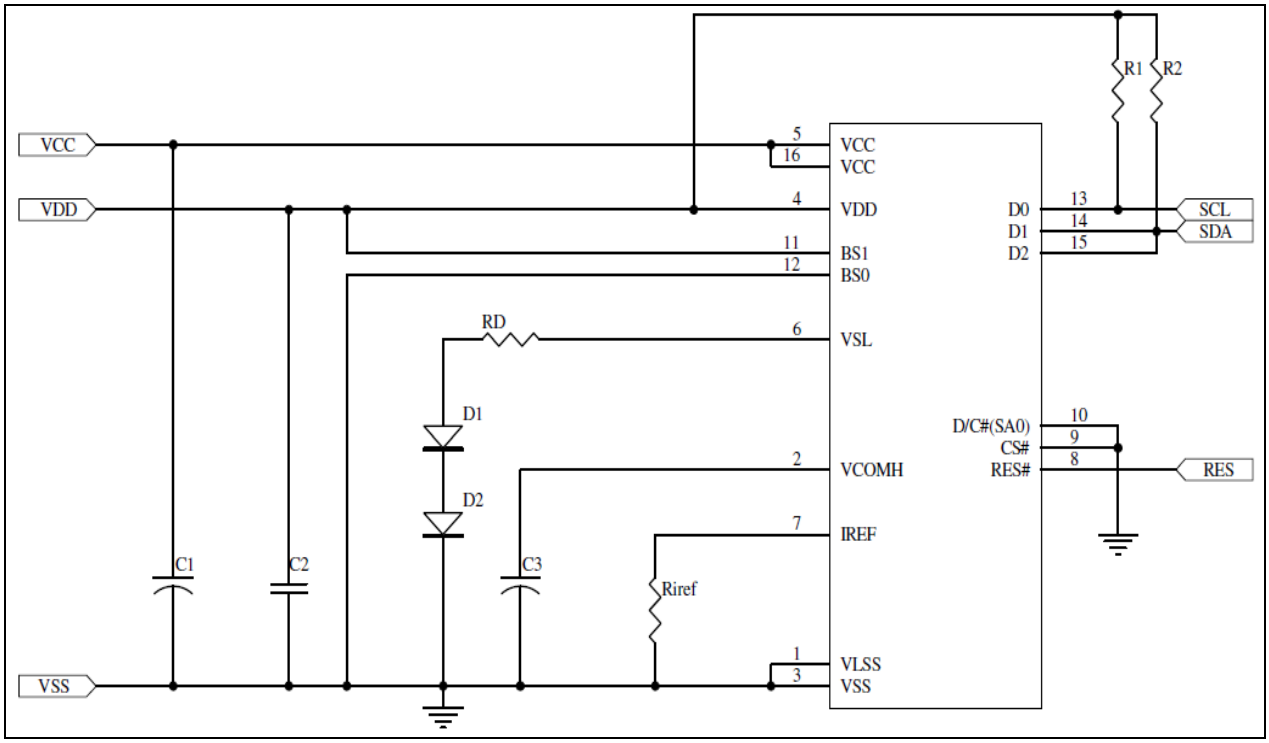
- Panel matrix 265x96.
- Driver IC: SSD1363.
- VCC=12V.
- VDD=1.65V~ 3.5V.
- 16 gray scale level supported by embedded 320 x 160 x 4 bit SRAM display buffer.
- 3/4 wire Serial Peripheral Interface,I^2C Interface.

FUNCTION BLOCK DIAGRAM



RiTdisplay 265X96 OLED Module

APPLICATION CIRCUIT



Recommend components:

C1, C3 : 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)

C2: 1uF/16V(0603)

Riref : 1M ohm 1%(0603)

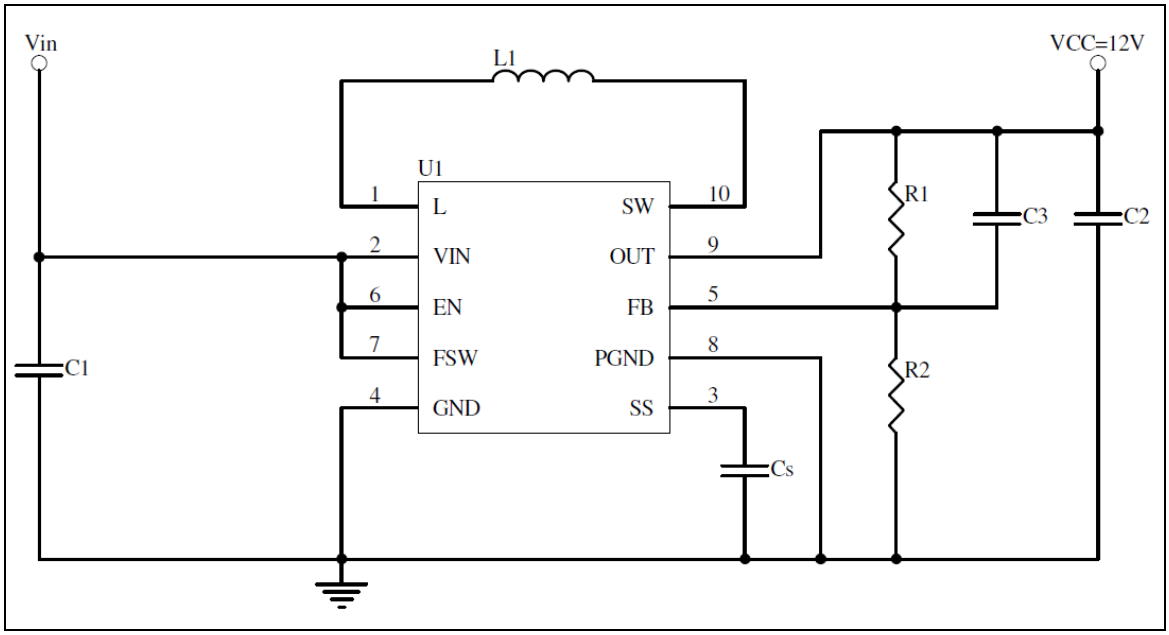
R1, R2: 10K ohm(0603)

RD : 49.9 ohm 1/4W

D1, D2 : RB480K(ROHM)

This circuit is for I^2C interface.

DC-DC application circuit for OLED module(For External DC/DC)



Recommend components:

The C1: 4.7uF/6.3V.

The C2: 4.7 uF/25V Tantalum type capacitor.

The C3: 50pF/16V.

The Cs: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 136K ohm/ 1%.

The L1: 4.7uH.

The U1: TPS61080

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

PIN No.	PIN Name.	DESCRIPTION	Setting at each interface		
			8080 parallel	SPI	IIC
1	VLSS	Analog system ground pin. It must be connected to external ground.			
2	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
3	VSS	Ground pin.			
4	VDD	Power supply pin for core logic operation.			
5	VCC	Power supply for panel driving voltage.			
6	VSL	This is segment voltage (output low level) reference pin. This pin has to be connected with resistor and diode to ground (details depends on application).			
7	IREF	This pin is the segment output current reference pin.			
8	RES#	This pin is reset signal input.	NA	NA	RES#
9	CS#	This pin is the chip select input connecting to the MCU.	NA	CS#	Low
10	D/C#(SA0)	This pin is Data/Command control pin connecting to the MCU.	NA	D/C#	SA0
11	BS1	MCU bus interface selection pins.	NA	Low	High
12	BS0		NA	Low	Low
13	D0	These pins are bi-directional data bus connecting to the MCU data bus. When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL	NA	SCLK	SCL
14	D1		NA	SDIN	SDA_{IN}
15	D2		NA	SDIN	SDA_{OUT}
16	VCC	Power supply for panel driving voltage.			

Note

(1) Low is connected to VSS

(2) High is connected to VDD

Application Initial Setting

```
/*265x96 OLED driver program*/
/* The more detail of I2C sequence please refer to the SSD1363 datasheet */
//Slave Address:0x78

void initial(void)
{
comm_out(0xae); //Display OFF

comm_out(0xfd); //Set Command Lock
data_out(0x12);

comm_out(0xa0); //Set Re-map and Dual COM Line mode
data_out(0x22);
data_out(0x00);

comm_out(0xa1); //Set Display Start Line
data_out(0x1f);

comm_out(0xa2); //Set Display Offset
data_out(0x60);

comm_out(0xa6); //Normal Display

comm_out(0xb1); //Set Phase Length
data_out(0x8f);

comm_out(0xb3); //Set Front Clock Divider/Oscillator Frequency
data_out(0xa1);//105Hz

comm_out(0xb6); //Set Second Precharge Period
data_out(0x08);

comm_out(0xb9); //Select Default Linear Gray Scale table

comm_out(0xbb); //Set Pre-charge voltage
data_out(0x1f);
```

```
comm_out(0xbe); //Set VCOMH
data_out(0x07); //0.86*VCC

comm_out(0xc1); //Set Contrast Current
data_out(0x88);//VCC:12V

comm_out(0xca); //Set MUX Ratio
data_out(0x5f);//96 Duty

cleanDDR();

comm_out(0xaf);//Display ON
}
```

```
/*After power on the OLED driver IC, please clean the DDRAM.*/
void cleanDDR(void)
{
int i,j;
comm_out(0x15); //set column address
comm_out (0x00);
comm_out (0x4f);
comm_out(0x75); //set row address
comm_out (0x00);
comm_out (0x9f);
comm_out (0x5c);
for(i=0;i<160;i++)
{
      for(j=0;j<80;j++)
      {
      data_out(0x00);
      data_out(0x00);
      }
   }
}
```

```
void show_data(void)
{
int i,j;
comm_out(0x15); //set column address
comm_out (0x06);
comm_out (0x48);
comm_out(0x75); //set row address
comm_out (0x1f);
comm_out (0x7f);
comm_out (0x5c);
for(i=0;i<96;i++)
 {
      for(j=0;j<67;j++)
      {
      data_out(0xff);
      data_out(0xff);
      }
   }
}
```

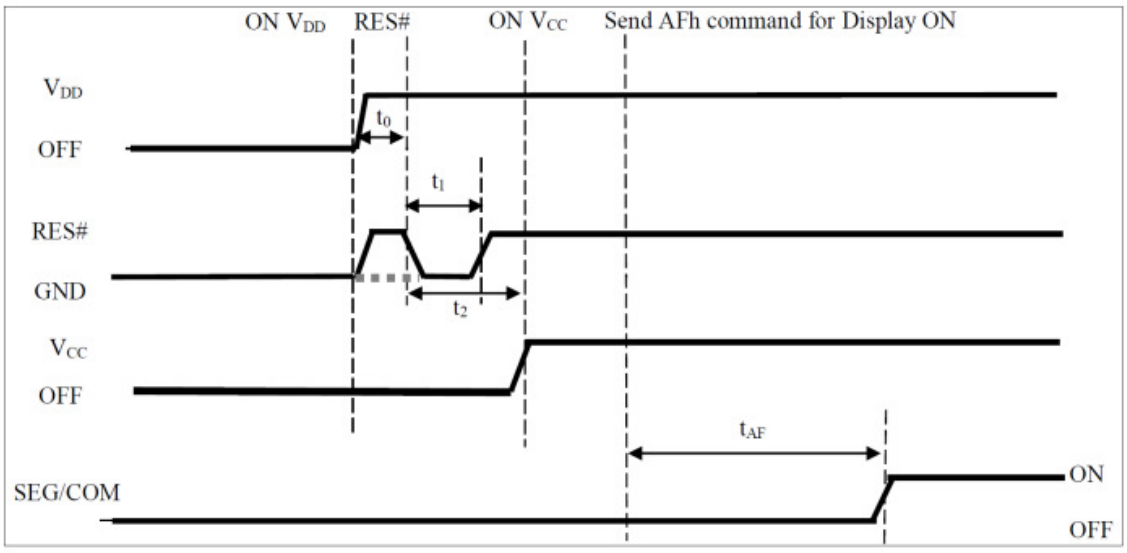
Power ON / OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1363.

***Power ON sequence*:**

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

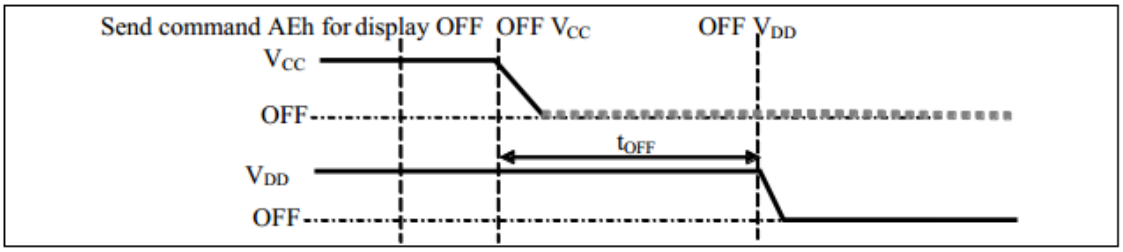
The Power ON sequence



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC} [1], [2]
3. Wait for t_{OFF}. Power OFF V_{CI}.(where Minimum t_{OFF}=80ms[5], Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1)V_{CC} should be kept float (i.e. disable) when it is OFF.

(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

(3) The register values are reset after t_1.

(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

Graphic Display Data RAM Address Map

The GDDRAM address map in Table shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D25440[3:0] in Table corresponds to the pixel located in (COM159, SEG2). So the lower nibble and higher nibble of D0, D1, D2, …, D25597, D25598, D25599 in Table represent the 320x160 data nibblesin the GDDRAM.

GDDRAM in Gray Scale mode (RESET)

		SEG0	SEG1	SEG2	SEG3		SEG316	SEG317	SEG31	SEG319	SEG Outputs
		00		00			4F		4F		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D159[3:0]	D159[7:4]	D158[3:0]	D158[7:4]	
COM1	01	D161[3:0]	D161[7:4]	D160[3:0]	D160[7:4]		D319[3:0]	D319[7:4]	D318[3:0]	D318[7:4]	
|	|									
COM158	9E	D25281[3:0]	D25281[7:4]	D25280[3:0]	D25280[7:4]		D25439[3:0]	D25439[7:4]	D25438[3:0]	D25438[7:4]	
COM159	9F	D25441[3:0]	D25441[7:4]	D25440[3:0]	D25440[7:4]		D25599[3:0]	D25599[7:4]	D25598[3:0]	D25598[7:4]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

Thank You