P42401

256x64 Yellow OLED
Application Notes
(for 8080 8bits Interface)

Revision History

Version	Content
X01	First release(For 8080 8bits Interface)

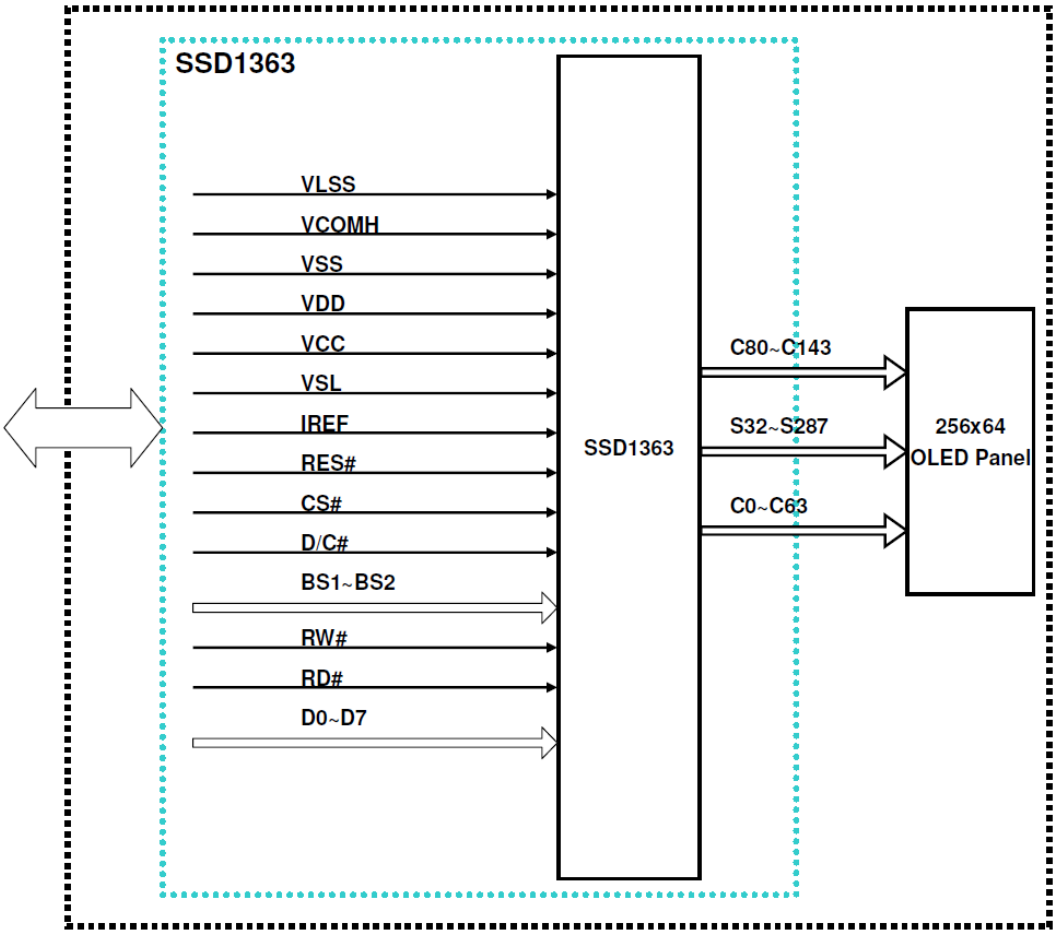
DESCRIPTION

P42401 is a 256 x 64 dot matrix yellow passive OLED module with controller for many compact portable applications.

FEATURE

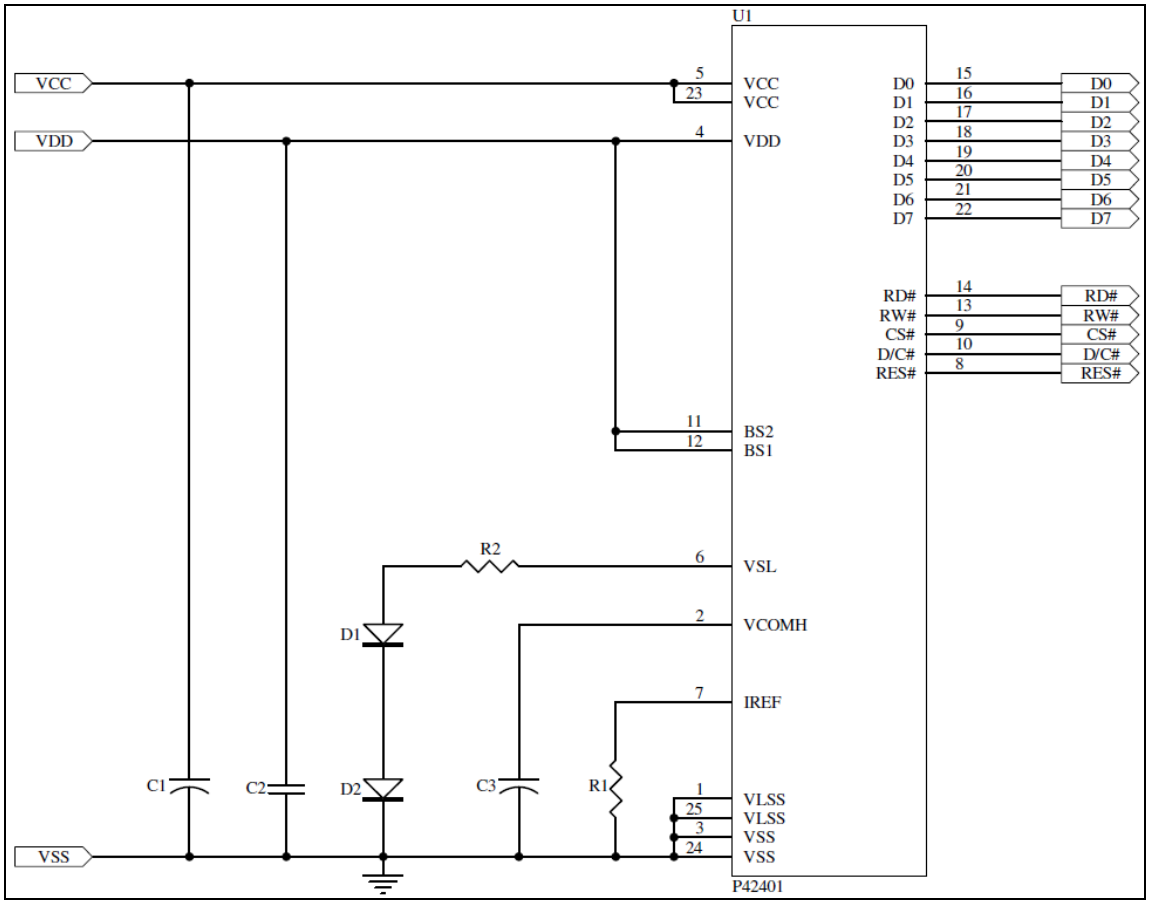
- Panel matrix：256x64.
- Driver IC：SSD1363.
- VCC=14V.
- VDD=1.65V~3.5V.
- 8 bits 6800/8080-series parallel Interface, 4 wire Serial Peripheral Interface, I^2C Interface.
- Display data RAM：320 x 160 x 4 bit SRAM display buffer.
- Screen saving continuous scrolling function in both horizontal and vertical direction.
- Screen saving infinite content scrolling function.

FUNCTION BLOCK DIAGRAM



RiTdisplay 256x64 OLED Module

APPLICATION CIRCUIT



Recommend components:

C1 : 4.7uF/25V(0805)

C3 : 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)

C2 : 1uF/16V(0603)

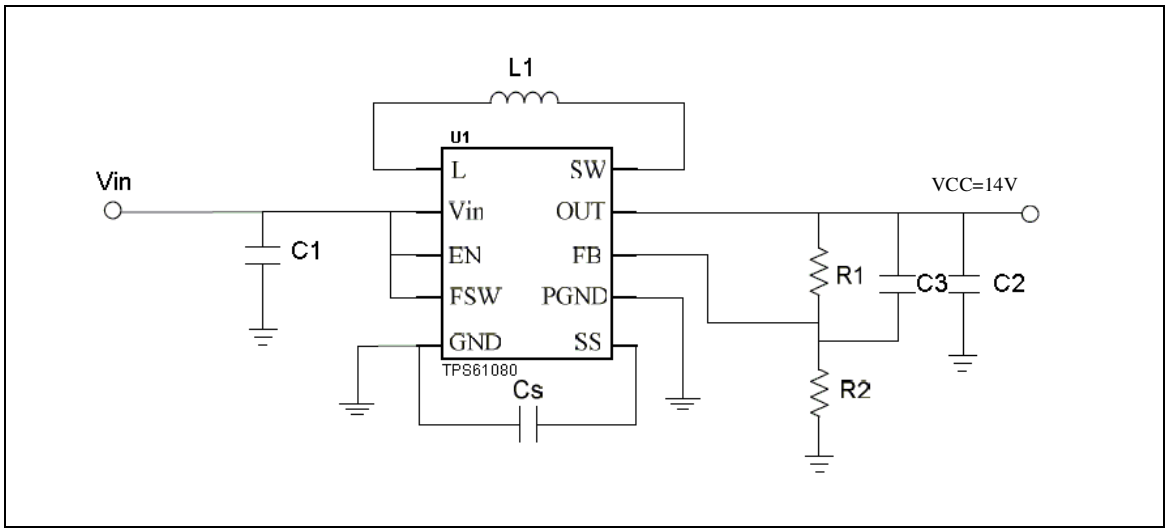
R1: 1M ohm (0603) 1%

R2: 49.9 ohm 1/4W

D1,D2: RB480K (ROHM)

This circuit is for 8080 8bit interface.

DC-DC application circuit for OLED module(For External DC/DC)



Recommend components:

The C1: 4.7uF/6.3V.

The C2: 4.7 uF/25V Tantalum type capacitor.

The C3: 50pF/16V.

The Cs: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 115K ohm/ 1%.

The L1: 4.7uH.

The U1: TPS61080

The R1, R2 and C3 value should be fine tune by customer.

Pin Assignments

Pin No.	Pin Name	Description	Setting at each interface		
			8080 parallel	SPI	IIC
1	VLSS	Analog system ground pin.			
2	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
3	VSS	Ground pin.			
4	VDD	Power supply pin for core logic operation.			
5	VCC	Power supply for panel driving voltage.			
6	VSL	This is segment voltage reference pin.			
7	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.			
8	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.			
9	CS#	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).	CS#	CS#	Tie LOW
10	D/C#	This is Data/Command control pin.	D/C#	D/C#	SA0
11	BS2	MCU bus interface selection pins.	High	Low	Low
12	BS1		High	Low	High
13	RW#	This pin is read / write control input pin connecting to the MCU interface. 8080: data write enable pin; 6800:Read/Write select pin.	WR#	Tie LOW	Tie LOW
14	RD#	8080: data read enable pin; 6800:Read/Write enable pin.When serial interface is selected, this pin must be connected to VSS.	RD#	Tie LOW	Tie LOW
15	D0	These pins are bi-directional data bus connecting to the MCU data bus. When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.	D0	SCLK	SCL
16	D1		D1	SDIN	SDA_{IN}
17	D2		D2	SDIN	SDA_{OUT}
18	D3		D3	Tie LOW	Tie LOW
19	D4		D4	Tie LOW	Tie LOW

20	D5		D5	Tie LOW	Tie LOW
21	D6		D6	Tie LOW	Tie LOW
22	D7		D7	Tie LOW	Tie LOW
23	VCC	Power supply for panel driving voltage.			
24	VSS	Ground pin.			
25	VLSS	Analog system ground pin.			

Note

(1) Low is connected to VSS

(2) High is connected to VDD

Application Initial Setting

```
/* 256 x 64 OLED driver program */

void initial(void)
{
comm_out(0xae);//Set Display OFF

comm_out(0xfd);//Set Command Lock
data_out(0x12);

comm_out(0xa0);//Set Re-map and Dual COM Line mode
data_out(0x02);
data_out(0x10);

comm_out(0xa1);//Set Display Start Line
data_out(0x00);

comm_out(0xa2);//Set Display Offset
data_out(0x00);

comm_out(0xa6);//Normal Display

comm_out(0xad);//Set IREF
data_out(0x80);

comm_out(0xb1);//Set Reset (Phase 1)/Pre-charge (Phase 2)period
data_out(0x74);

comm_out(0xb3);//Set Front Clock Divider/Oscillator Frequency
data_out(0xb1);

comm_out(0xb6);//Set Second Pre-charge Period
data_out(0x08);

comm_out(0xb9);//Select Default Linear Gray Scale table

comm_out(0xba);//Set Pre-charge voltage configuration
data_out(0x02);

comm_out(0xbb);//Set Pre-charge voltage
data_out(0x07);

comm_out(0xbe);//Set VCOMH
data_out(0x07);

comm_out(0xc1);//Set Contrast Current
data_out(0x4f);//VCC=14V
```

```
comm_out(0xca);//Set MUX Ratio
data_out(0x7f);

CleanDDR();

comm_out(0xaf);//Set Display ON
}
```

```
void CleanDDR(void)
{
int i,j;
comm_out(0x15);
data_out(0x00);
data_out(0x4f);

comm_out(0x75);
data_out(0x00);
data_out(0x9f);

comm_out(0x5c);

for(i=0;i<160;i++)
  {
    for(j=0;j<160;j++)
    {
    data_out(0x00);
    }
  }
}
```

After initial the driver IC, user can display all pixels on.

```
void show_data(void)
{
int i,j;
comm_out(0x15);
data_out(0x08);
data_out(0x47);

comm_out(0x75);
data_out(0x00);
data_out(0x3f);

comm_out(0x5c);

for(i=0;i<64;i++)
  {
    for(j=0;j<128;j++)
    {
    data_out(0xff);
    }
  }
}
```

Graphic Display Data RAM (GDDRAM)

The GDDRAM address map in Table shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D25440[3:0] in Table corresponds to the pixel located in (COM159, SEG2). So the lower nibble and higher nibble of D0, D1, D2, …, D25597, D25598, D25599 in Table represent the 320x160 data nibbles in the GDDRAM.

Table : GDDRAM in Gray Scale mode (RESET)

		SEG0	SEG1	SEG2	SEG3		SEG316	SEG317	SEG31	SEG319	SEG Outputs
		00		00			4F		4F		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D159[3:0]	D159[7:4]	D158[3:0]	D158[7:4]	
COM1	01	D161[3:0]	D161[7:4]	D160[3:0]	D160[7:4]		D319[3:0]	D319[7:4]	D318[3:0]	D318[7:4]	
|	|									
COM158	9E	D25281[3:0]	D25281[7:4]	D25280[3:0]	D25280[7:4]		D25439[3:0]	D25439[7:4]	D25438[3:0]	D25438[7:4]	
COM159	9F	D25441[3:0]	D25441[7:4]	D25440[3:0]	D25440[7:4]		D25599[3:0]	D25599[7:4]	D25598[3:0]	D25598[7:4]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

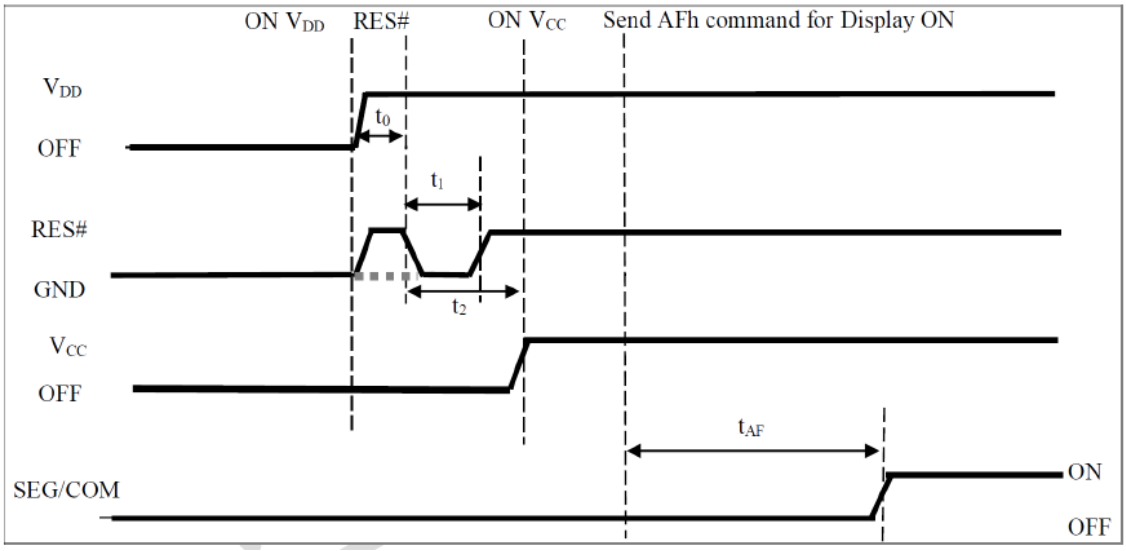
POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1363.

Power ON sequence:

1. Power ON VDD
2. After VDD become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1)[4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON VCC.[1]
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).

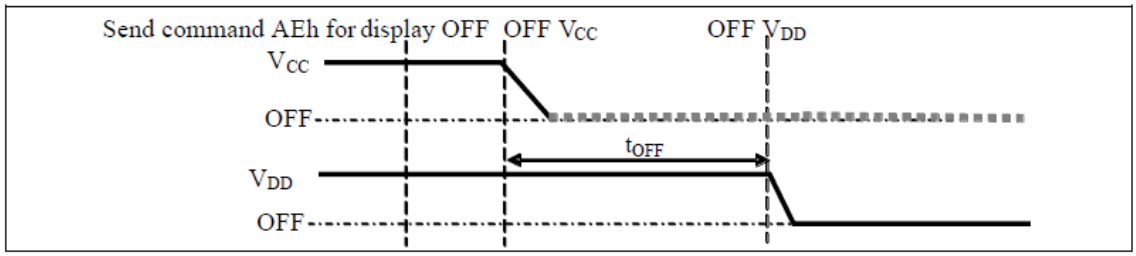
The Power ON sequence



Power OFF sequence:

1.Send command AEh for display OFF.
2.Power OFF VCC.[1],[2]
3.Power OFF VDD after t_{OFF}.[4] (where Minimum t_{OFF}=80ms, typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1)V_{CC} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

Thank You