P42101

128x128 White OLED
Application Note
(For SPI Interface)

Revision History

Version	Content
X01	First release(For SPI Interface)

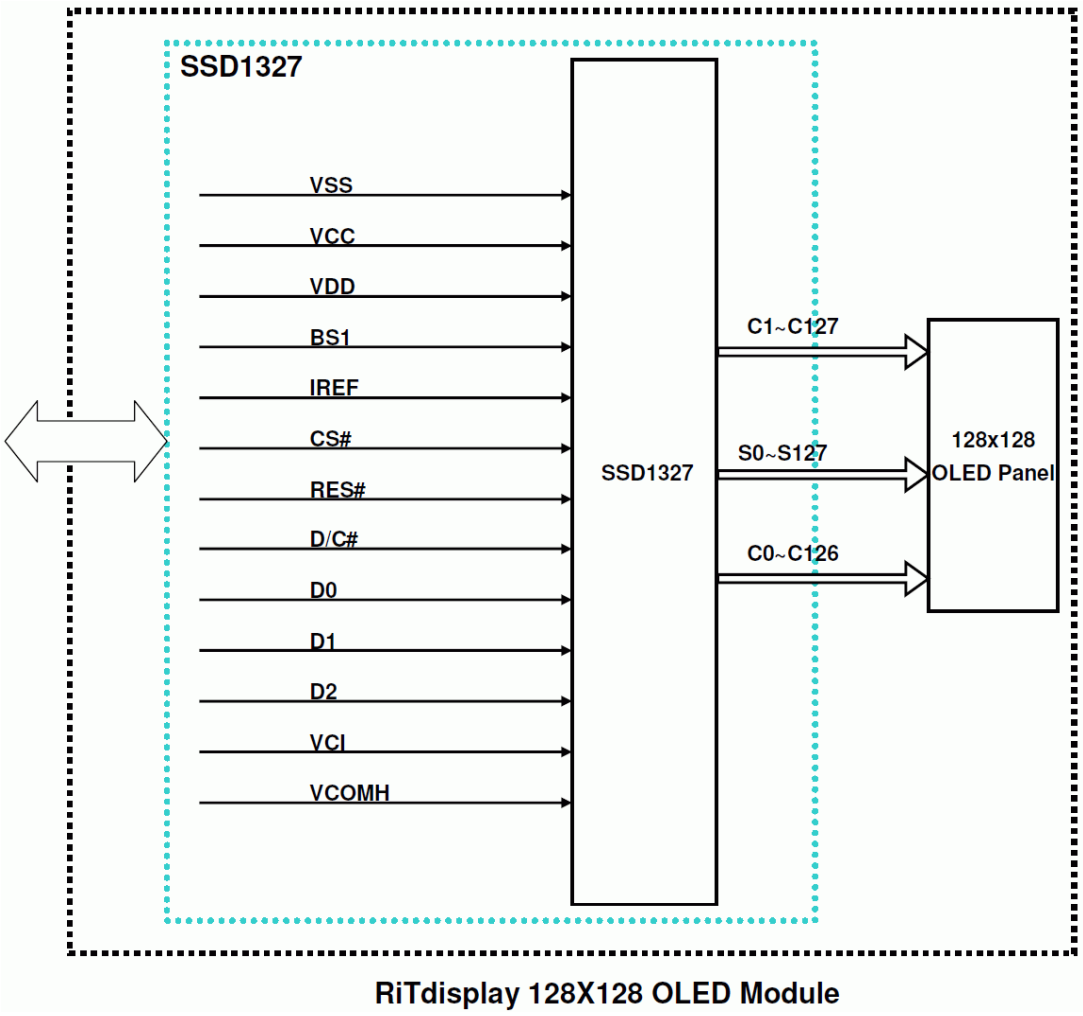
DESCRIPTION

P42101 is a 128X128 dot matrix white passive OLED module with controller for many compact portable applications.

FEATURE

- Panel matrix: 128x128.
- Driver IC: SSD1327.
- 16 gray scale
- V_{CC} =14V
- **Internal VDD:** VCI =2.6V~3.5V
- (Must use relative the circuit and the initial code.)
- **External VDD**: VCI =1.65V~2.6V
- (Must use relative the circuit and the initial code.)
- Serial Peripheral Interface, I^2C Interface.

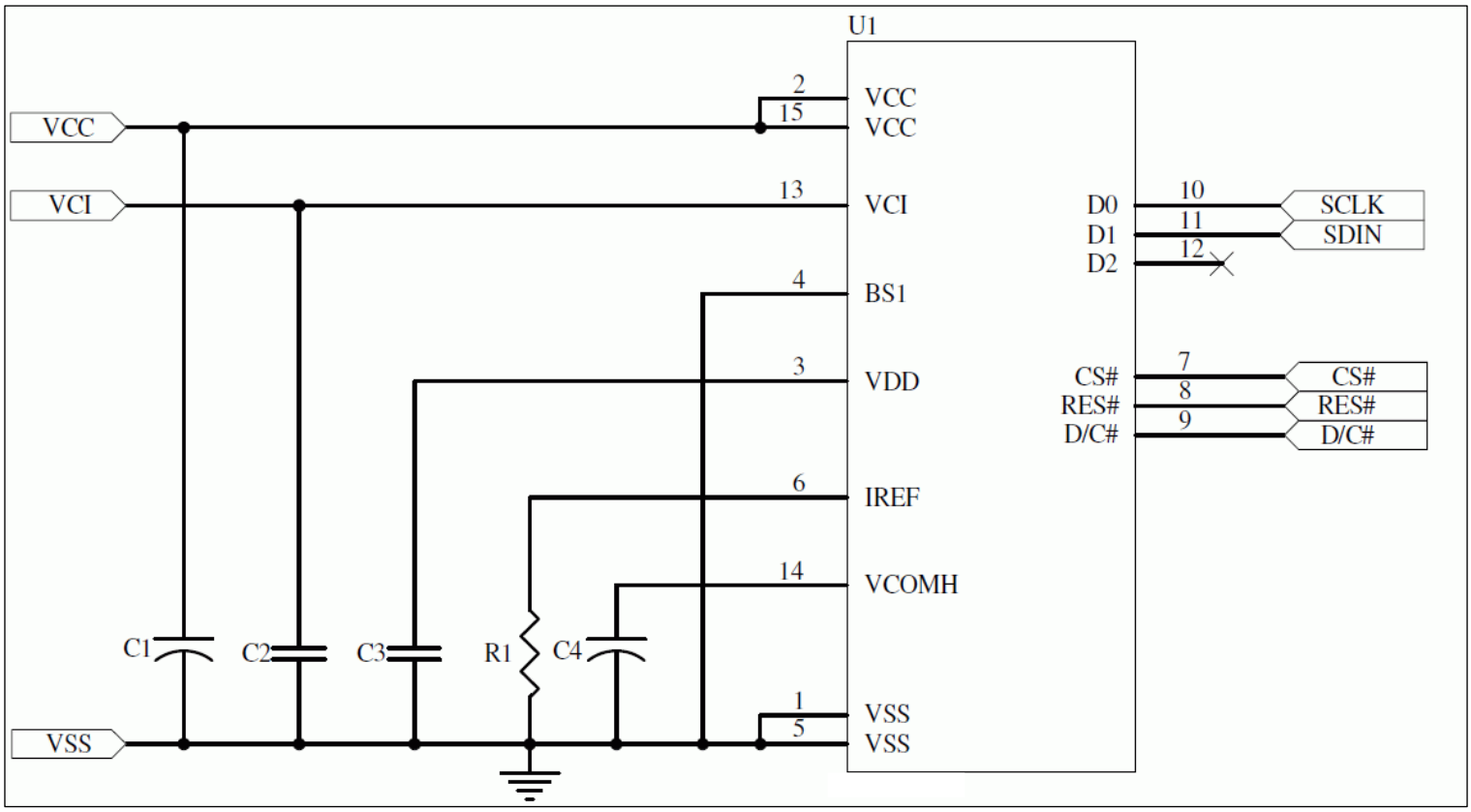
FUNCTION BLOCK DIAGRAM



RiTdisplay 128X128 OLED Module

Application circuit

(*Internal VDD*: VCI =2.6V~3.5V)



Recommend components:

C1, C4: 4.7uF/25V or 35V (Tantalum type) or VISHAY (572D475X0025A2T)

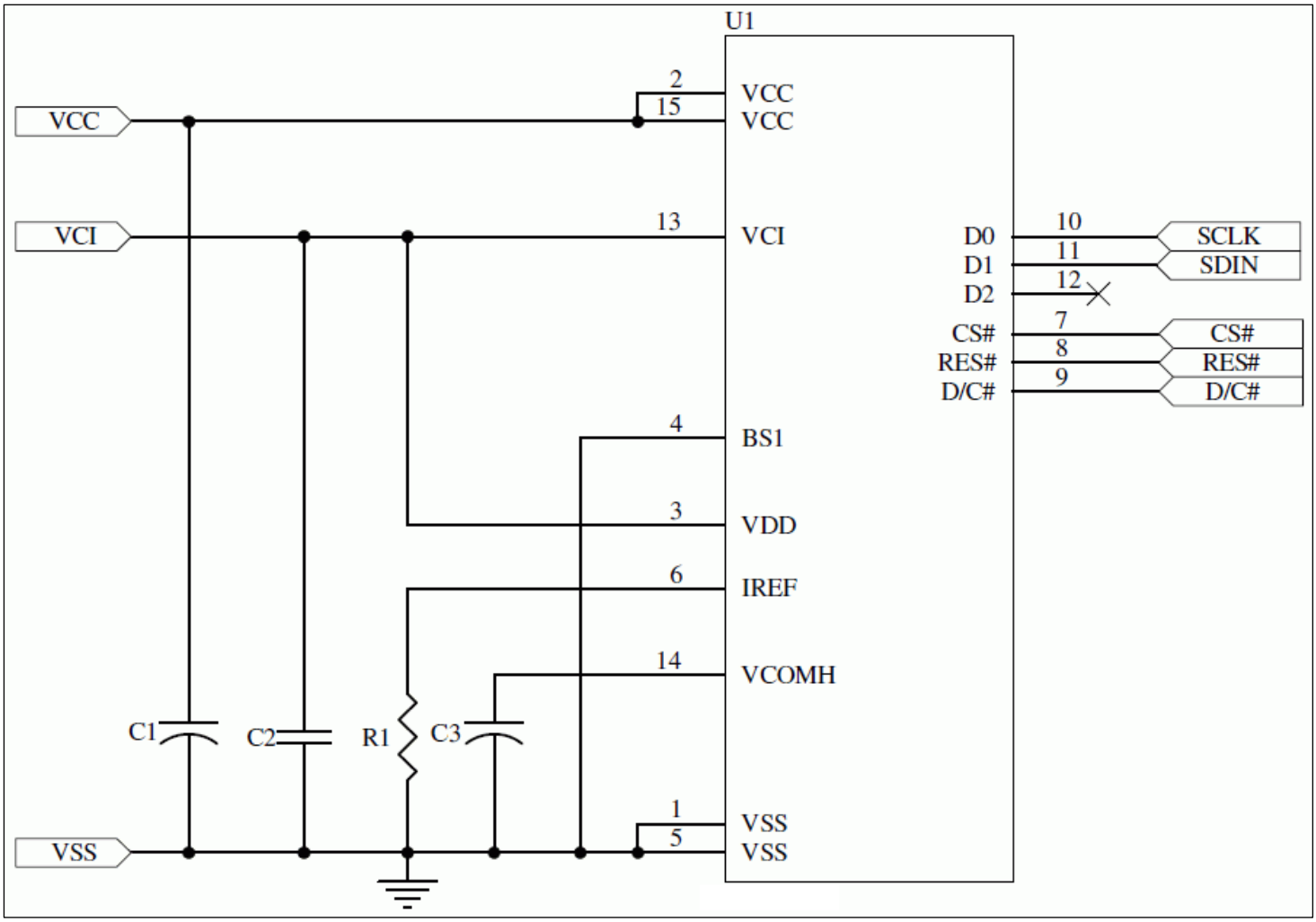
C2, C3: 1uF/16V

R1: 1M ohm 1 %(0603)

Note: This circuit is for SPI interface.

Application circuit

(*External VDD*: VCI =1.65V~2.6V)



Recommend components:

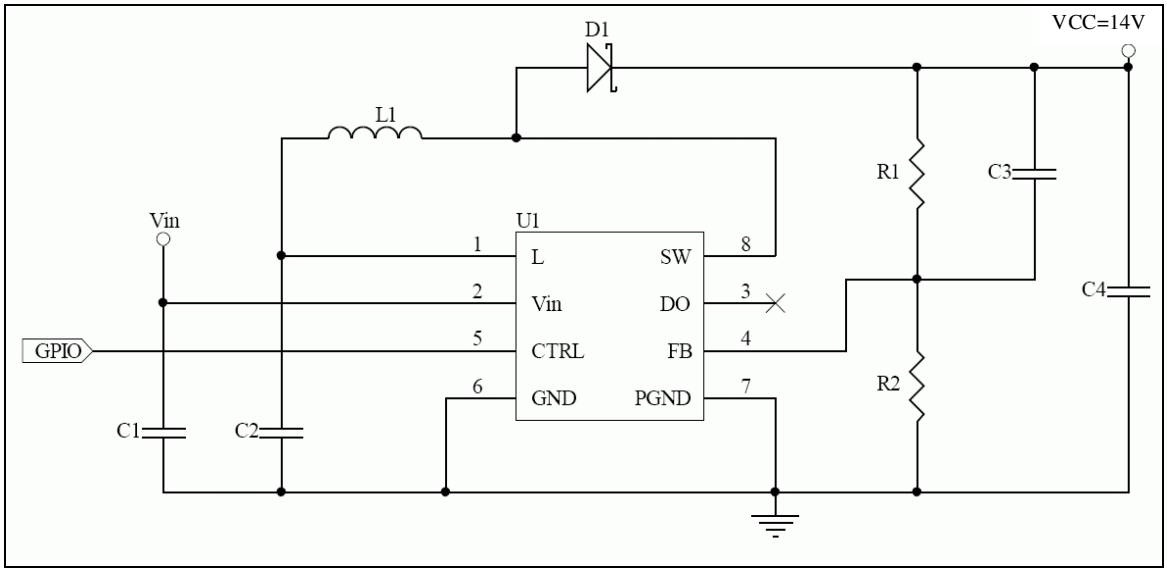
C1, C3: 4.7uF/25V or 35V (Tantalum type) or VISHAY (572D475X0025A2T)

C2: 1uF/16V

R1: 1M ohm 1 %(0603)

Note: This circuit is for SPI interface.

DC-DC application circuit for OLED module



Recommend components:

The C1: 0.1uF/6.3V.

The C2: 4.7 uF/6.3V.

The C3: 22pF/16V.

The C4: 4.7uF/25V Tantalum type capacitor.

The R1: 1.2M ohm1%.

The R2: 115K ohm1%.

The D1: SCHOTTY DIODE.

The L1: 10uH.

The U1: TPS61045

Note: The R1, R2 and C3 value should be fine tune by customer.

Pin Assignments

PIN NAME	PIN NO.	DESCRIPTION	Setting at each interface		
			8080 Parallel	SPI	IIC
VSS	1	Ground pin.			
VCC	2	Power supply for panel driving voltage.			
VDD	3	Power supply pin for core logic operation.			
BS1	4	MCU bus interface selection pins.	NC	Low	High
VSS	5	Ground pin.			
IREF	6	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.			
CS#	7	This pin is the chip select input connecting to the MCU.	NA	CS#	Low
RES#	8	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.	NA	RES#	RES#
D/C#	9	This pin is Data/Command control pin connecting to the MCU.	NA	D/C#	Low
D0	10	When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDAout,SDAin in application and D0 is the serial clock input, SCL.	NA	SCLK	SCL
D1	11		NA	SDIN	SADIN
D2	12		NA	**NC**	SDAOUT
VCI	13	Low voltage power supply and power supply for interface logic level.			
VCOMH	14	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
VCC	15	Power supply for panel driving voltage.			

Note

(1) Low is connected to VSS

(2) High is connected to VCI

Application Initial Setting (*Internal VDD*: VCI =2.6V~3.5V)

```
/*128x128 OLED driver program */
void initial(void)
{
comm_out(0xae);//Set display off

comm_out(0xa0);//Set re-map
comm_out(0x43);

comm_out(0xa1);//Set display start line
comm_out(0x00);

comm_out(0xa2);//Set display offset
comm_out(0x00);

comm_out(0xa4);//Normal Display

comm_out(0xa8);//Set multiplex ratio
comm_out(0x7f);

comm_out(0xab);//Function Selection A
comm_out(0x01);//Enable internal VDD regulator

comm_out(0x81);//Set contrast
comm_out(0x53);//For VCC=14V

comm_out(0xb1);//Set Phase Length
comm_out(0x31);

comm_out(0xb3);//Set Front Clock Divider /Oscillator Frequency
comm_out(0xc1);//105 Hz

comm_out(0xb4); //For brightness enhancement
comm_out(0xb5);

comm_out(0xb6);//Set Second pre-charge Period
comm_out(0x0d);
```

```
comm_out(0xbc);//Set Pre-charge voltage
comm_out(0x04);

comm_out(0xbe);//Set VCOMH
comm_out(0x07);

comm_out(0xd5);//Function Selection B
comm_out(0x60);

cleanDDR ();//Clear the whole DDRAM

comm_out(0xaf);//Display on
}
```

Application Initial Setting (*External VDD*: VCI =1.65V~2.6V)

```
/*128x128 OLED driver program */
void initial(void)
{
comm_out(0xae);//Set display off

comm_out(0xa0);//Set re-map
comm_out(0x43);

comm_out(0xa1);//Set display start line
comm_out(0x00);

comm_out(0xa2);//Set display offset
comm_out(0x00);

comm_out(0xa4);//Normal Display

comm_out(0xa8);//Set multiplex ratio
comm_out(0x7f);

comm_out(0xab);//Function Selection A
comm_out(0x00);//Select external VDD

comm_out(0x81);//Set contrast
comm_out(0x53);//For VCC=14V

comm_out(0xb1);//Set Phase Length
comm_out(0x31);

comm_out(0xb3);//Set Front Clock Divider /Oscillator Frequency
comm_out(0xc1);//105Hz

comm_out(0xb4); //For brightness enhancement
comm_out(0xb5);

comm_out(0xb6);//Set Second pre-charge Period
comm_out(0x0d);
```

```
comm_out(0xbc);//Set Pre-charge voltage
comm_out(0x04);

comm_out(0xbe);//Set VCOMH
comm_out(0x07);

comm_out(0xd5);//Function Selection B
comm_out(0x60);

cleanDDR ();//Clear the whole DDRAM

comm_out(0xaf);//Display on
}
```

```
void cleanDDR(void)
{
   int i,j;
   comm_out(0x15);//Set column address
   comm_out(0x00);//Column Start Address
   comm_out(0x3f);//Column End Address
   comm_out(0x75);//Set row address
   comm_out(0x00);//Row Start Address
   comm_out(0x7f);//Row End Address
   for(i=0;i<128;i++)
   {
      for(j=0;j<64;j++)
      {
        data_out(0x00);
      }
   }
}
```

After initial the driver IC, user can display all pixels on.

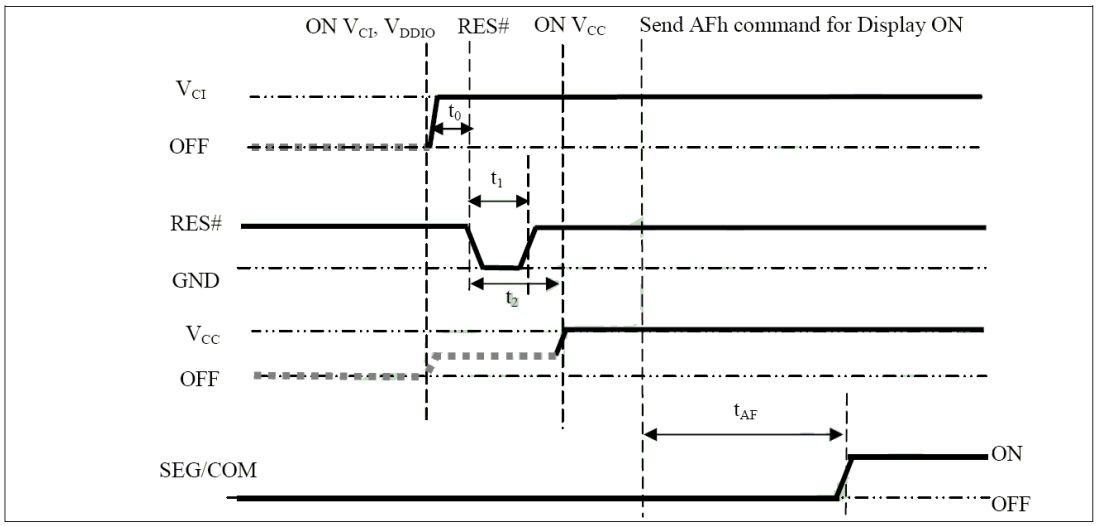
```
void show_data(void)
{
   int i,j;
   comm_out(0x15);//Set column address
   comm_out(0x00);//Column Start Address
   comm_out(0x3f);//Column End Address
   comm_out(0x75);//Set row address
   comm_out(0x00);//Row Start Address
   comm_out(0x7f);//Row End Address
   for(i=0;i<128;i++)
   {
      for(j=0;j<64;j++)
      {
        data_out(0xff);
      }
   }
}
```

Power ON / OFF Sequence

Power ON sequence:

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

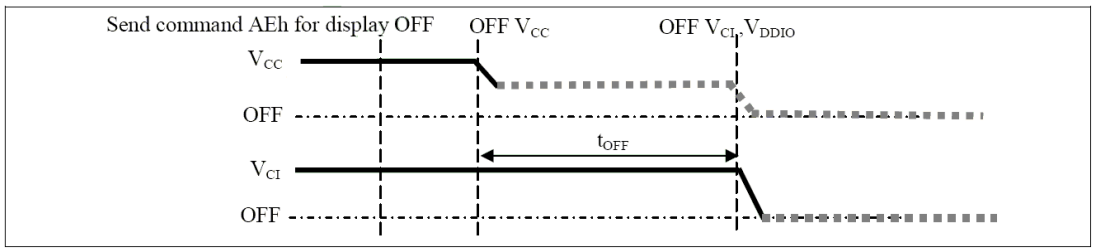
The Power ON sequence.



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Wait for t_{OFF}. Power OFF V_{CI}.(where Minimum t_{OFF}=80ms [5], Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
(2) V_{CC} should be kept disable when it is OFF.
(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.
(4) The register values are reset after t_1.
(5) V_{CI} should not be Power OFF before V_{CC} Power OFF.

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs

Row Address (HEX)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]
|	|								
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Enable Column Address Re-map (A[0]=1)
  - Enable Nibble Re-map (A[1]=1)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|								
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble re-map A[1]=1

The example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs

Row Address (HEX)

(Display Startline=78H)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

GDDRAM address map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs Column Address (HEX)

COM Outputs

Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

Thank You