P41002

28x120 White OLED
Application Notes
(for SPI Interface)

Revision History

Version	Content
X01	First release(For SPI Interface)

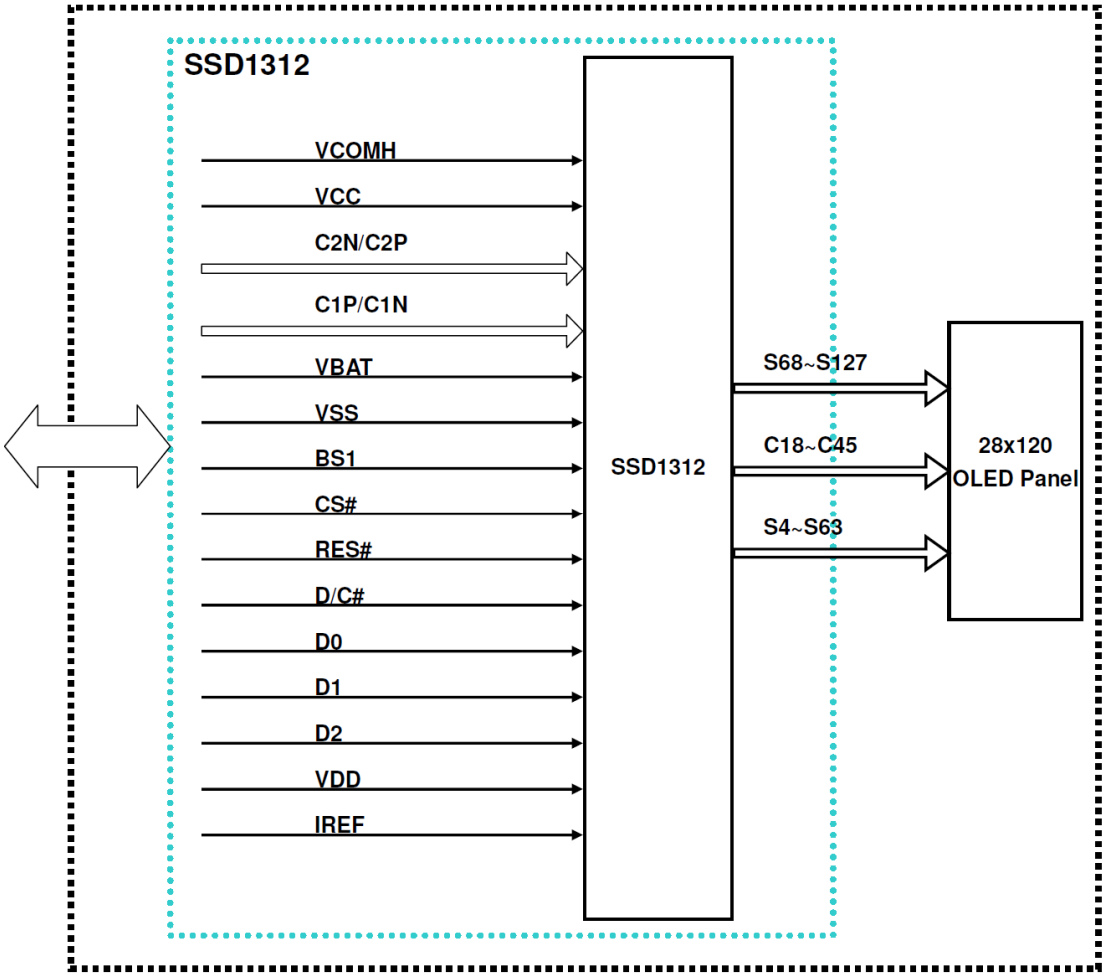
DESCRIPTION

P41002 is a 28x120 dot matrix white passive OLED module with controller for many compact portable applications.

FEATURE

- Panel matrix: 28x120.
- Driver IC is SSD1312.
- VBAT=3.5V~4.5V(For Charge Pump).
- VDD=1.65V~3.5V.
- Embedded 128 x 64 bit SRAM display buffer.
- 4 wire Serial Peripheral Interface, I^2C Interface.
- Screen saving continuous scrolling function in both horizontal and vertical direction.

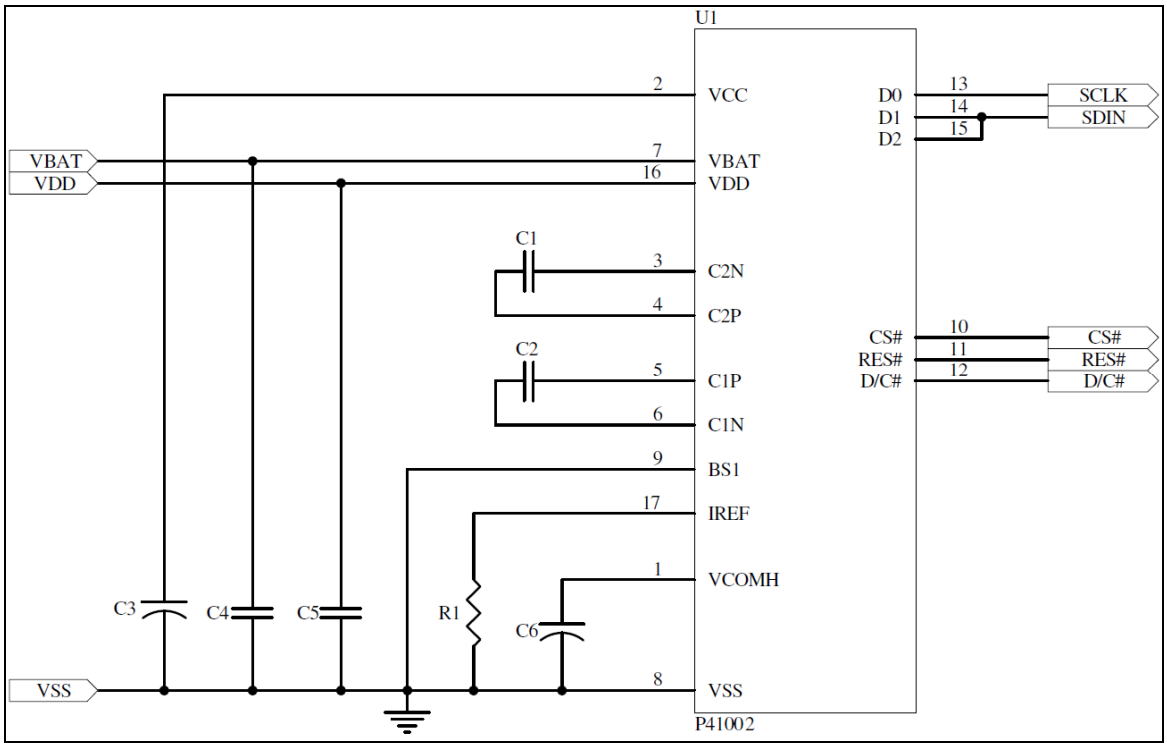
FUNCTION BLOCK DIAGRAM



RiTdisplay 28x120 OLED Module

Application circuit

(Charge Pump)



Recommend components:

C3, C6: 4.7uF/16V(0805)

C1, C2, C4, C5: 1uF/16V(0603)

R1: 2M ohm (0603) 1%

This circuit is for 4 wire SPI interface.

Pin Assignments

Pin No.	Pin Name	Description	Setting at each interface		
			8080 parallel	SPI	IIC
1	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.			
2	VCC	Power supply for panel driving voltage.			
3	C2N	C2N/C2P – Pin for charge pump capacitor; Connect to each other with a capacitor.			
4	C2P				
5	C1P	C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor.			
6	C1N				
7	VBAT	Power supply for charge pump regulator circuit.			
8	VSS	Ground pin.			
9	BS1	MCU bus interface selection pins.	NA	Low	High
10	CS#	This pin is the chip select input connecting to the MCU.	NA	CS#	Low
11	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.			
12	D/C#	This pin is Data/Command control pin connecting to the MCU.	NA	D/C#	SA0
13	D0	When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.	NA	SCLK	SCL
14	D1		NA	SDIN	SDA_{IN}
15	D2		NA	SDIN	SDA_{OUT}
16	VDD	Power supply pin for core logic operation.			
17	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.			

Note

(1) Low is connected to VSS

(2) High is connected to VDD

Application Initial Setting

/*28x120 OLED driver program (For Charge Pump) */

```
void initial(void)
{
comm_out(0xae);//Set Display OFF

comm_out(0xa8);//Set Multiplex Ratio
comm_out(0x1b);

comm_out(0xad);//External or Internal IREF Selection
comm_out(0x40);

comm_out(0xd3);//Set Display Offset
comm_out(0x12);

comm_out(0xa0);//Set Segment Remap

comm_out(0xc8);//Set COM Output Scan Direction

comm_out(0xa6);//Set Normal Display

comm_out(0x40);//Set Display Start Line

comm_out(0xa4);//Entire Display ON/Off

comm_out(0x81);//Set Contrast Control
comm_out(0x30);

comm_out(0xd9);//Set Pre-charge Period
comm_out(0x22);

comm_out(0xd5);//Set Display Clock Divide Ratio/Oscillator Frequency
comm_out(0x41);

comm_out(0xda);//Set SEG Pins Hardware Configuration
comm_out(0x10);

comm_out(0x20);//Set Memory Addressing Mode
```

```
comm_out(0x02);//Page Addressing Mode

comm_out(0xdb);//Set VCOMH Deselect Level
comm_out(0x30);

comm_out(0x8d);//Charge Pump Setting
comm_out(0x52);

cleanDDR();         //Clear the whole DDRAM

comm_out(0xaf);//Set Display ON
}
```

```
void cleanDDR(void)
{
int i,j;
for(i=0;i<8;i++)
 {
   comm_out(0xb0+i);   //Set Page
   comm_out(0x00);     //Lower Column Address
   comm_out(0x10);     //Higher Column Address
   for(j=0;j<128;j++)
   {
   data_out(0x00);
   }
 }
}
```

After initial the driver IC, user can display all pixels on.

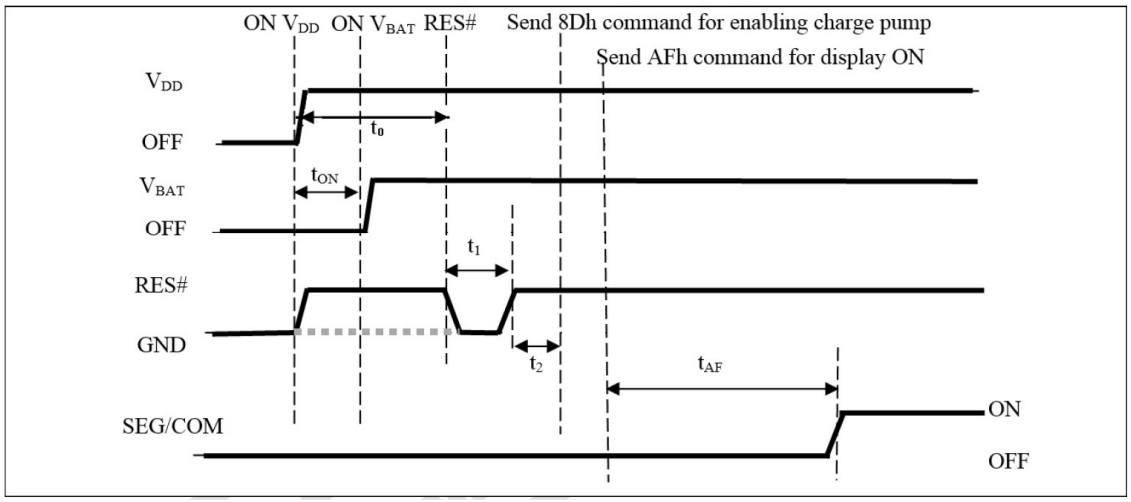
```
void show_data(void)
{
int i,j;
for(i=0;i<4;i++)
 {
   comm_out(0xb0+i);   //Set Page
   comm_out(0x08);     //Lower Column Address
   comm_out(0x10);     //Higher Column Address
   for(j=0;j<120;j++)
   {
   data_out(0xff);
   }
 }
}
```

Power ON and OFF sequence with Charge Pump Application

Power ON sequence:

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}. (where Minimum t_{ON} = 0ms)
3. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1)[3]and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then input commands with below sequence:
   a. 8Dh for enabling internal charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms (t_{AF}).

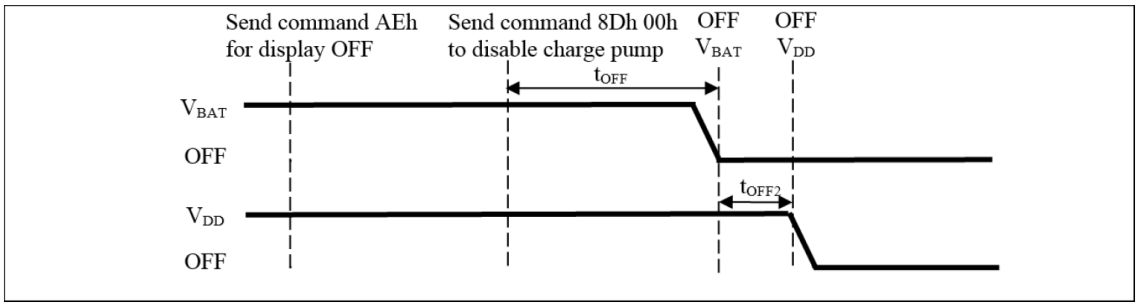
The Power ON sequence with Charge Pump Application



Power OFF sequence:

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}.[1], [2] (Typical t_{OFF} =100ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2} = 0ms[4] , Typical t_{OFF2}=5ms)

The Power OFF sequence with Charge Pump Application



Note:

(1)V_{BAT} should be kept float (i.e. disable) when it is OFF.
(2)Power Pins (V_{BAT}) can never be pulled to ground under any circumstance.
(3)The register values are reset after t_1.
(4)V_{DD} should not be Power OFF before V_{BAT} Power OFF.

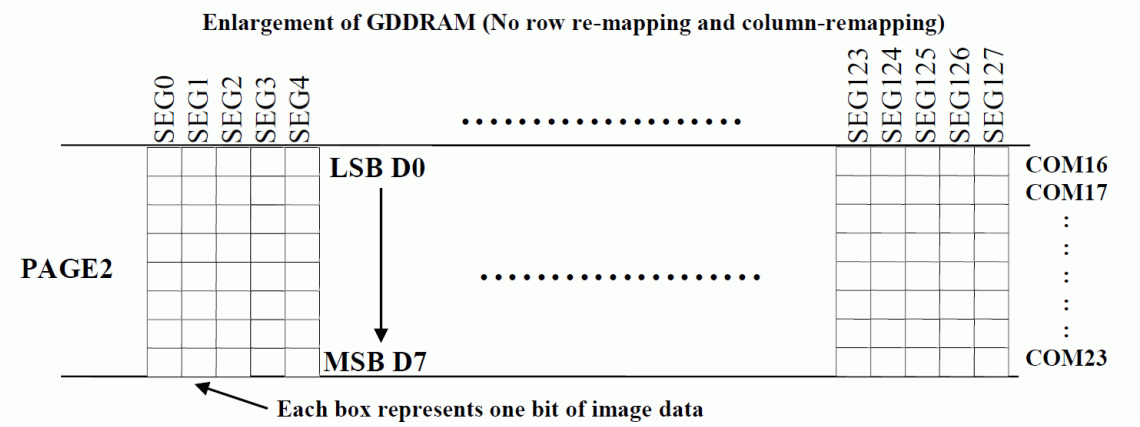
Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown below figures.

GDDRAM pages structure

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown below figures.



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

Thank You