P31601

256x32 White OLED
IIC Application Notes

Revision History

Version	REVISION DESCRIPTION
X01	First release

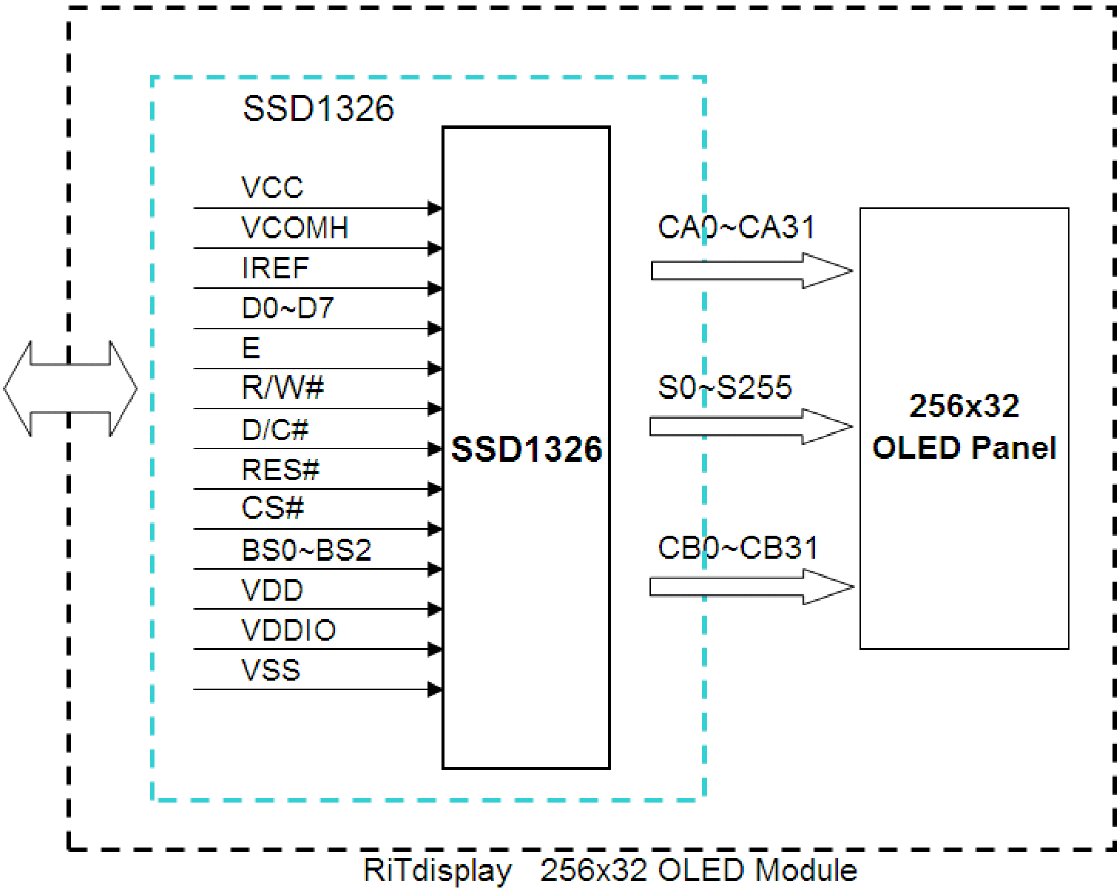
DESCRIPTION

P31601 is a 256x32 dot matrix White passive OLED module with controller for many compact portable applications.

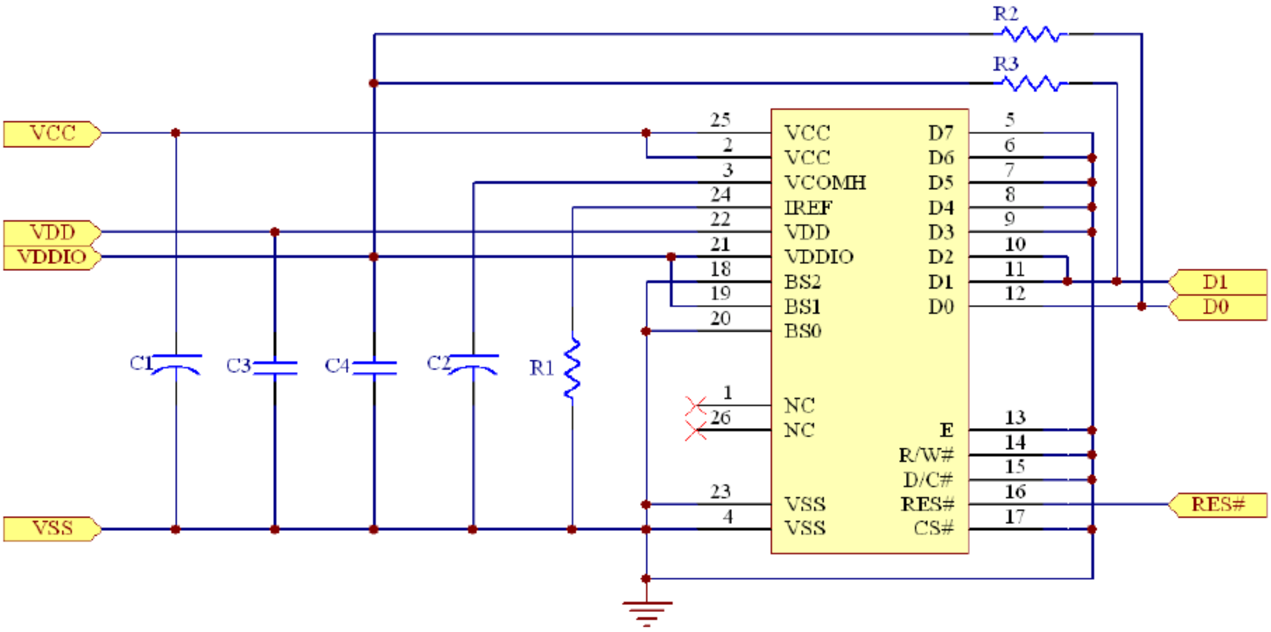
FEATURE

- Panel resolution：256×32
- Driver IC：SSD1326
- VCC = 12V
- VDD = 2.4V ~ 3.5V
- VDDIO = 1.7V ~ VDD
- 8-bit 8080-series parallel interface, serial peripheral interface and I^2C interface.
- Display data RAM : 256x32 = 8192 bits

FUNCTION BLOCK DIAGRAM



APPLICATION CIRCUIT



Recommend components：

C1、C2：4.7uF/25V Tantalum type or VISHAY(572D475X0025A2T)

C3、C4：0.1uF/16V

R1 ：680K ohm 1% (0603)

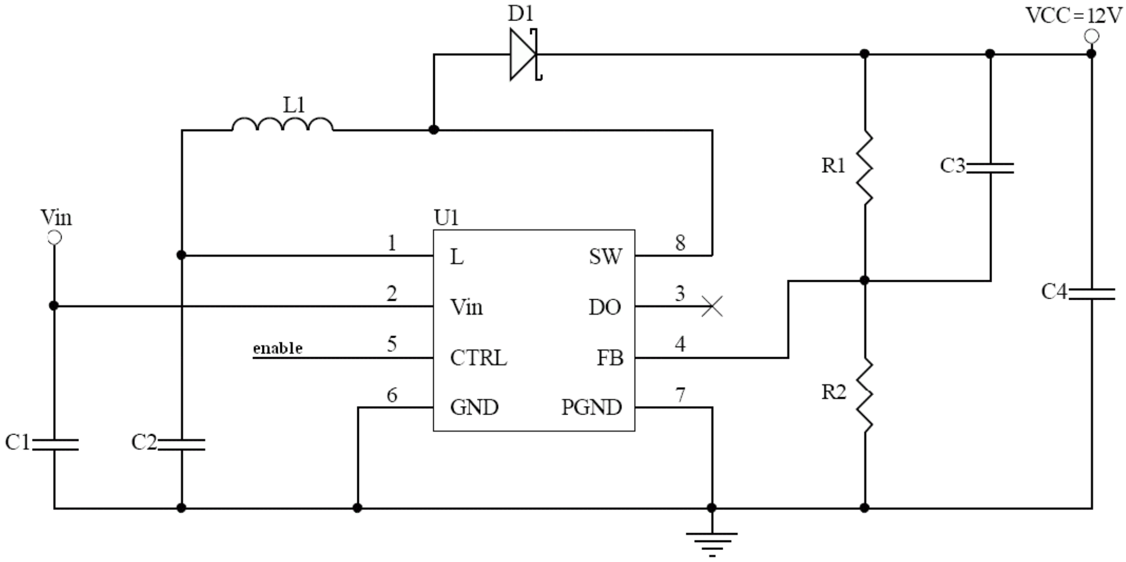
R2, R3: 10k ohm (0603)

Note:

This circuit is designed for IIC interface.

The R2 and R3 value should be find turn by customer.

External DC-DC application circuit



Recommend components：

C1：0.1uF/6.3V

C2：4.7uF/6.3V

C3：10pF/16V

C4：4.7uF/25V Tantalum type or VISHAY(572D475X0025A2T)

R1：1.2M ohm/ 1%

R2：137K ohm/ 1%

D1：SCHOTTY DIODE

L1：10uH

U1：TPS61045

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

Pin No.	Pin Name	Description	Setting at each interface		
			8080 parallel	SPI	IIC
1	NC	No connection.			
2	VCC	OLED drive power supply			
3	VCOMH	The COM voltage reference pin			
4	VSS	This is ground pin.			
5	D7	Data Bus	D7	Tie LOW	Tie LOW
6	D6		D6		
7	D5		D5		
8	D4		D4		
9	D3		D3		
10	D2		D2	NC	SDA_{OUT}
11	D1		D1	SDIN	SDA_{IN}
12	D0		D0	SCLK	SCL
13	E	Read select	E	Tie LOW	Tie LOW
14	R/W#	Write select	R/W#		
15	D/C#	Data/Command control.	D/C#	D/C#	SA0
16	RES#	Reset			
17	CS#	Chip select	CS#	CS#	Tie LOW
18	BS2	Interface select	High	Low	Low
19	BS1		High	Low	High
20	BS0		Low	Low	Low
21	VDDIO	Power supply for interface logic level.			
22	VDD	Power supply for core logic.			
23	VSS	This is ground pin.			
24	IREF	ISEG is derived from IREF.			
25	VCC	OLED drive power supply			
26	NC	No connection.			

Note

(1) Low is connected to V_{SS}

(2) High is connected to V_{DDIO}

Application Software

```
void initial_SSD1326(void)
{
   start();
   comm_out(0x78); //Mast code
   comm_out(0x00);
   comm_out ( 0xfd ) ;    //unluck MCU interface from entering command
   comm_out ( 0x12 ) ;
   comm_out ( 0xae ) ;    //display off
   comm_out ( 0xa8 ) ;    //set MUx ratio
   comm_out ( 0x1f ) ;    //32MUX
   comm_out ( 0xa4 ) ;    //set display mode
   comm_out ( 0xa2 ) ;    //set display offset
   comm_out ( 0x00 ) ;
   comm_out ( 0xa1 ) ;    //set display start line
   comm_out ( 0x00 ) ;
   comm_out ( 0xa0 ) ;    //set re_map and gray scale / mono mode
   comm_out ( 0x04 ) ;
   comm_out ( 0x87 ) ;    //full current
   comm_out ( 0x81 ) ;    //set contrast current
   comm_out ( 0x3d ) ;    //normal mode (type brightness)
   comm_out ( 0xbe ) ;    //output level high voltage for COM signal
   comm_out ( 0x0f ) ;
   comm_out ( 0xbc ) ;    //set Pre-charge voltage,
   comm_out ( 0x1f ) ;
   comm_out ( 0xb1 ) ;    //set phase length
   comm_out ( 0x11 ) ;
   comm_out ( 0xb3 ) ;    //set front clock divider/oscillator frequency
   comm_out ( 0x82 ) ;   //105Hz
   stop();
   cleanDDR ( ) ;         //Clear the whole DDRAM
   start();
   comm_out(0x78); //Mast code
   comm_out(0x00);
   comm_out ( 0xaf ) ;    //set display on
   stop();
}
```

```
void cleanDDR(void)
{
  int i,j；
   start();
   comm_out(0x78); //Mast code
   comm_out(0x00);
  comm_out ( 0x15 )；  //Set column address
  comm_out ( 0x00 )；  //Column Start Address
  comm_out ( 0x7F)；  //Column End Address
  comm_out ( 0x75 )；  //Set row address
  comm_out ( 0x00 )；  //Row Start Address
  comm_out ( 0x1F )；  //Row End Address
   stop();

start();
comm_out(0x78); //Mast code
comm_out(0x40);
for ( i=0；i<32；i++ )
  {
    for ( j=0；j<128；j++ )
    {
      data_out(0x00)；
     }
  }
stop();
}
```

After initial the driver IC, user can display all pixels on.

```
void show_data(void)
{
   int i,j；
   start();
   comm_out(0x78); //Mast code
   comm_out(0x00);
   comm_out ( 0x15 )；  //Set column address
   comm_out ( 0x00 )；  //Column Start Address
   comm_out ( 0x7F)；  //Column End Address
   comm_out ( 0x75 )；  //Set row address
   comm_out ( 0x00 )；  //Row Start Address
   comm_out ( 0x1F )；  //Row End Address
   stop();

start();
comm_out(0x78); //Mast code
comm_out(0x40);
for ( i=0；i<32；i++ )
   {
      for ( j=0；j<128；j++ )
      {
         data_out(0xFF)；
       }
   }
stop();
}
```

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 256x32 = 8192 bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

Display Data RAM Map

Colum	0~7								8~15								……	248~255							
ROW	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0
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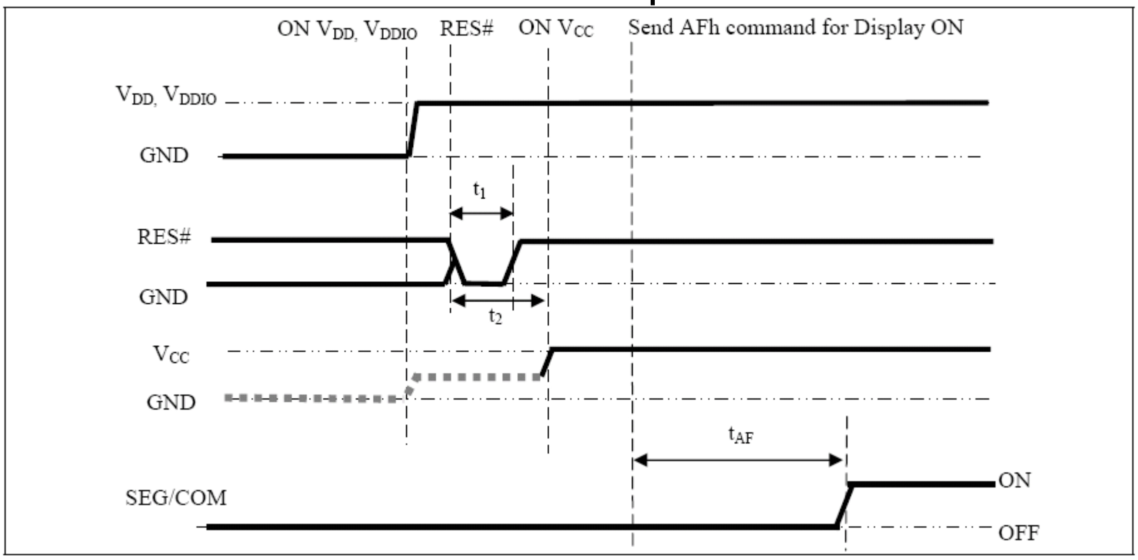
POWER ON and OFF SEQUENCE

The following figures illustrate the power ON and power OFF sequence of SSD1326.

***Power ON sequence*：**

1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 2us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW(logic low), wait for at least 2us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).

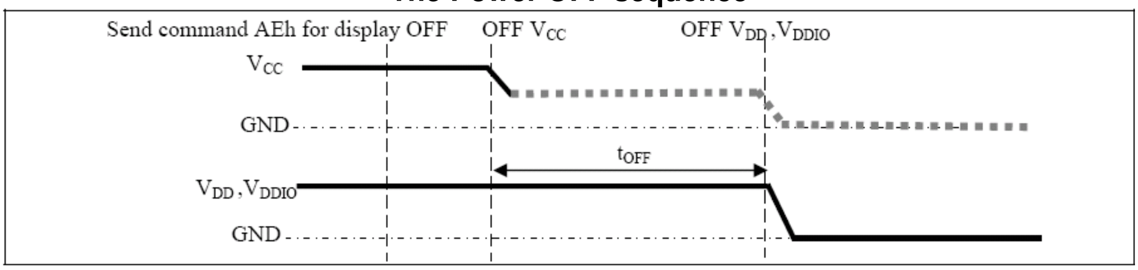
The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}.(where Minimum t_{OFF}=80ms,Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} are ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above Figures.

(2) V_{CC} should be kept disabled when it is OFF.

Thank You