P23901
P23902
128x128 Full OLED
3-Wire SPI Application Notes

Revision History

Version	REVISION DESCRIPTION
X01	First release

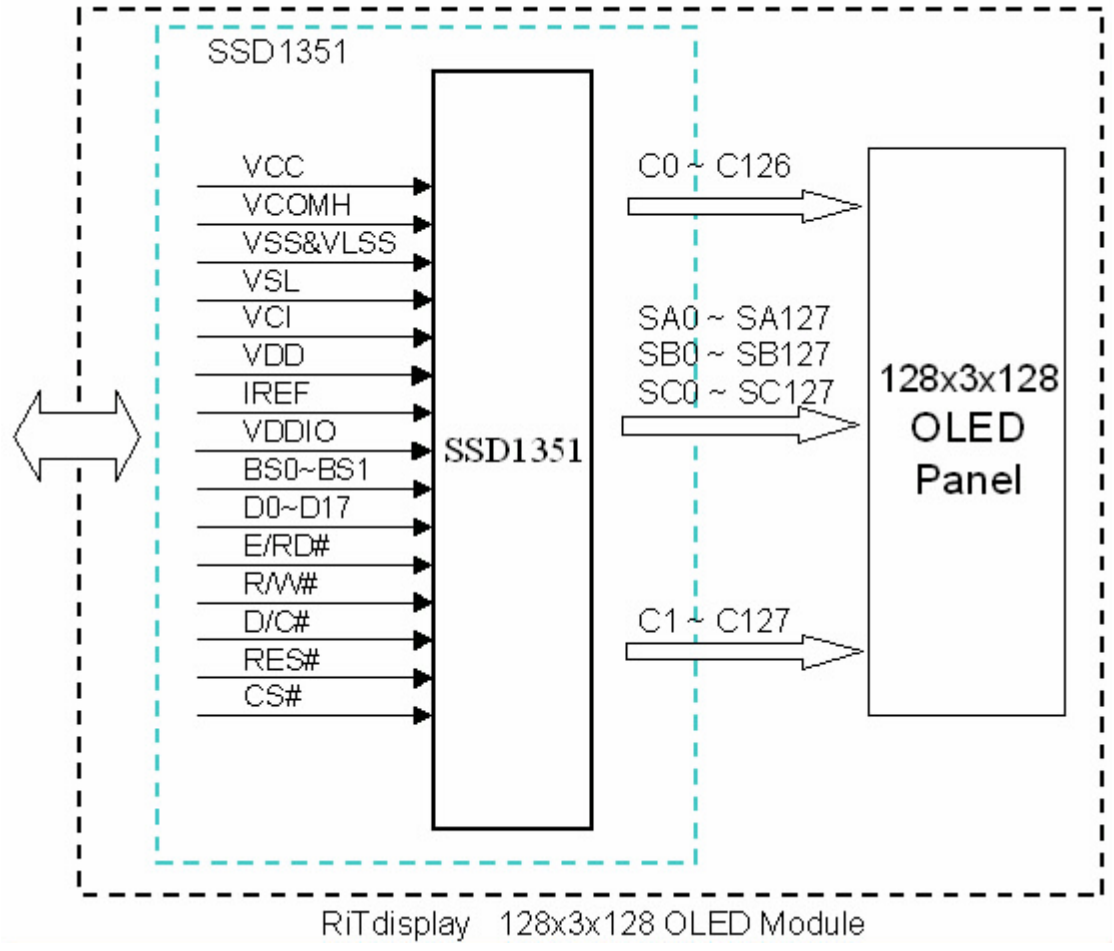
DESCRIPTION

P23901 & P23902 is a 128x3x128 dot matrix full passive OLED module with controller for many compact portable applications.

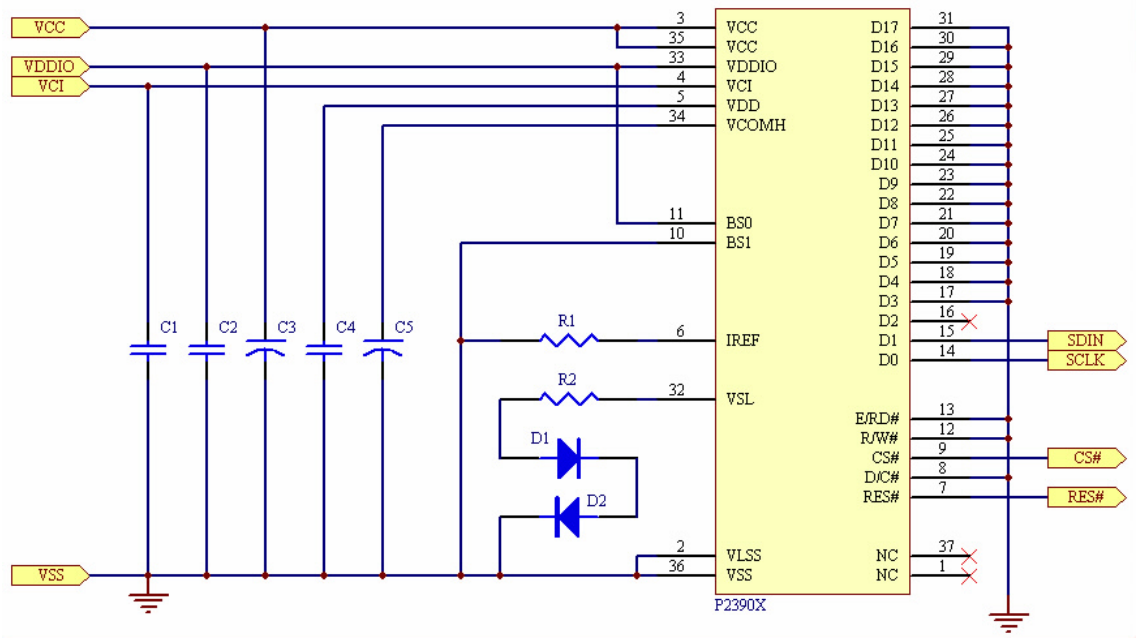
FEATURE

- Panel matrix：128x3x128
- Driver IC : SSD1351
- VCC = 16.5V
- VCI = 2.4V ~ 3.5V
- VDDIO =1.65V~ VCI
- Embedded 128x128x18 bit SRAM display buffer.
- 8/16/18 bits 6800-series parallel interface, 8/16/18 bits 8080-series parallel interface, Serial Peripheral interface.
- Vertical and Horizontal Scrolling.
- Programmable color mode of 65K,262K.

FUNCTION BLOCK DIAGRAM



APPLICATION CIRCUIT



Recommend components：

C1, C2, C4: 1uF/16V(0805)

C3,C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

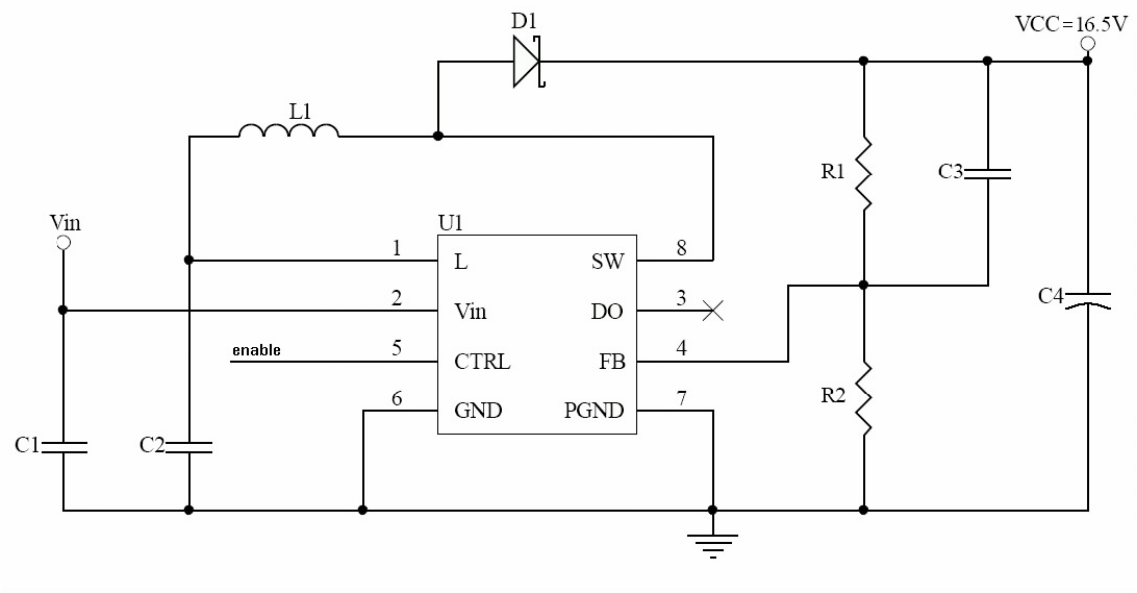
R1: 1M ohm 1% (0603)

R2: 50 ohm 1/4W

D1, D2: RB480K (ROHM)

This circuit is designed for SPI interface.

External DC-DC application circuit



Recommend components：

The C1: 4.7uF/6.3V.

The C2: 4.7uF/35V (Tantalum type capacitor).

The C3: 50pF/16V.

The C4: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 96K ohm/ 1%.

The L1: 4.7uH.

The U1: TPS61080

The R1, R2 and C3 value should be fine tune by customer.

NOTE：

a. The HPA00483DRBR is low cost DC/DC for TI.

b. The HPA00483DRBR specification is same as TPS61045.

PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	NC	No connection.
2	VLSS	Analog system ground pin.
3	VCC	Power supply for panel driving voltage.
4	VCI	Voltage power supply for logic.
5	VDD	A capacitor should be connected to this pin and V_{SS}.
6	IREF	A resistor should be connected between this pin and V_{SS}.
7	RES#	Hardware reset signal.
8	D/C#	When serial interface is selected, this pin must be connected to V_{SS}.
9	CS#	This is a chip select control pin.
10	BS1	Interface select pin.
11	BS0	Interface select pin.
12	R/W#	When serial interface is selected, this pin must be connected to V_{SS}.
13	E/RD#	When serial interface is selected, this pin must be connected to V_{SS}.
14	D0	These pins are bi-directional data bus connecting to the MCU data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
15	D1	
16	D2	
17	D3	
18	D4	
19	D5	
20	D6	
21	D7	
22	D8	In 8-bit parallel interface, D8~D17 should be connected VSS.
23	D9	
24	D10	
25	D11	
26	D12	
27	D13	
28	D14	
29	D15	
30	D16	
31	D17	
32	VSL	This is segment voltage reference pin.
33	VDDIO	Power supply for interface logic level.
34	VCOMH	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
35	VCC	Power supply for panel driving voltage.
36	VSS	Ground pin.
37	NC	No connection.

Application Software

```
/* 128x3x128 OLED driver program */
/* The more detail of SPI sequence please refer the SSD1351 datasheet */

void initial_SSD1351(void)
 {
     comm_out(0xfd);  //Set Command Lock
     data_out(0xb1);    //Unlock OLED driver IC
     comm_out(0xae); //Display off
     comm_out(0xa0); //Set Re-map Color Depth
     data_out(0x74);    //65K Color
     comm_out(0xa1); //Set Display Start Line
     data_out(0x00);
     comm_out(0xa2); //Set Display Offset
     data_out(0x00);
     comm_out(0xa6); //Normal display
     comm_out(0xab); //Function Selection
     data_out(0x01);
     comm_out(0xb1); //Set Reset (Phase 1) /Pre-charge (Phase 2) period
     data_out(0x53);
     comm_out(0xb3); //Set frame rate
     data_out(0x60);
     comm_out(0xb4); //External VSL
     data_out(0xa0);
     data_out(0xb5);
     data_out(0x55);
     comm_out(0xb9); //Use Built-in Linear LUT
     comm_out(0xbb); //Set Pre-charge voltage
     data_out(0x00);
     comm_out(0xbe); //Set VCOMH
     data_out(0x02);
     comm_out(0xc1); //Set contrast level for R,G,B
     data_out(0x70);    //Red contrast set
     data_out(0x71);    //Green contrast set
     data_out(0x94);    //Blue contrast set
     comm_out(0xc7); //Master current control
     data_out(0x0b);
     comm_out(0xca); //Set MUX Ratio
     data_out(0x7f);
     cleanDDR();
     comm_out(0xaf);  //Display on
 }
```

```
void cleanDDR(void)
{
      int i,j;
      ram _address( );
      comm_out(0x5c);
      for(i=0;i<128;i++)
      {
            for(j=0;j<128;j++)
            }
               data_out(0x00);
               data_out(0x00);
            }
      }
}

write_red_data(void)
{
      int I,j;
      ram _address( );
      comm_out(0x5c);
      for(i=0;i<128;i++)
      {
            for(j=0;j<128;j++)
            }
                  data_out(0xf8); //RED
                  data_out(0x00);
            }
      }
}

write_green_data(void)
{
      int I,j;
      ram _address( );
      comm_out(0x5c);
      for(i=0;i<128;i++)
      {
            for(j=0;j<128;j++)
            }
                  data_out(0x07); //GREEN
                  data_out(0xe0);
            }
```

```
    }
}

write_blue_data(void)
{
    int I,j;
    ram _address( );
    comm_out(0x5c);
    for(i=0;i<128;i++)
    {
        for(j=0;j<128;j++)
        }
            data_out(0x00); //BLUE
            data_out(0x1f);
        }
    }
}

write_white_data(void)
{
    int I,j;
    ram _address( );
    comm_out(0x5c);
    for(i=0;i<128;i++)
    {
        for(j=0;j<128;j++)
        }
            data_out(0xff); //WHITE
            data_out(0xff);
        }
    }
}

ram _address(void);
{
    comm_out(0x15); //Set Column Address
    data_out(0x00);   //Column Start Address
    data_out(0x7f);   //Column End Address
    comm_out(0x75); //Set Row Address
    data_out(0x00);   //Row Start Address
    data_out(0x7f);   //Row End Address
}
```

For 90 cd/m2 setting, user could follow the below setting.

```
Brightness_mode1 (void);
{
      comm_out((0xc7);//Master current control
      data_out(0x0b);
      comm_out(0xc1); //Set contrast level
      data_out(0x70);   //Red contrast set
      data_out(0x71);   //Green contrast set
      data_out(0x94);   //Blue contrast set
}
```

For 80 cd/m2 setting, user could follow the below setting.

```
Brightness_mode2 (void);
{
      comm_out((0xc7);//Master current control
      data_out(0x0a);
      comm_out(0xc1); //Set contrast level
      data_out(0x6c);   //Red contrast set
      data_out(0x6c);   //Green contrast set
      data_out(0x90);   //Blue contrast set
}
```

For 70 cd/m2 setting, user could follow the below setting.

```
Brightness_mode3 (void);
{
      comm_out((0xc7);//Master current control
      data_out(0x09);
      comm_out(0xc1); //Set contrast level
      data_out(0x66);   //Red contrast set
      data_out(0x6a);   //Green contrast set
      data_out(0x89);   //Blue contrast set
}
```

For 60 cd/m2 setting, user could follow the below setting.

```
Brightness_mode4 (void);
{
    comm_out((0xc7);//Master current control
    data_out(0x08);
    comm_out(0xc1); //Set contrast level
    data_out(0x64);   //Red contrast set
    data_out(0x69);   //Green contrast set
    data_out(0x85);   //Blue contrast set
}
```

For 40 cd/m2 setting, user could follow the below setting.

```
Brightness_mode5 (void);
{
    comm_out((0xc7);//Master current control
    data_out(0x06);
    comm_out(0xc1); //Set contrast level
    data_out(0x5b);   //Red contrast set
    data_out(0x60);   //Green contrast set
    data_out(0x7c);   //Blue contrast set
}
```

For 20 cd/m2 setting, user could follow the below setting.

```
Brightness_mode6 (void);
{
    comm_out((0xc7);//Master current control
    data_out(0x04);
    comm_out(0xc1); //Set contrast level
    data_out(0x4e);   //Red contrast set
    data_out(0x53);   //Green contrast set
    data_out(0x6e);   //Blue contrast set
}
```

Graphic Display Data RAM Address Map(GDDRAM)

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128x128x18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	.....	.....	126	127		
	Remapped	127			126			125	.....	.....	1	0		
Color		A	B	C	A	B	C	A			C	A	B	C
Data / Format		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3
Common Address		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0
Normal	Remapped													Common output
0	127	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM2
3	124	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM3
4	123	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM5
6	121	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6	COM6
7	120								.....	.....	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
123	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6	:
124	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM127

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

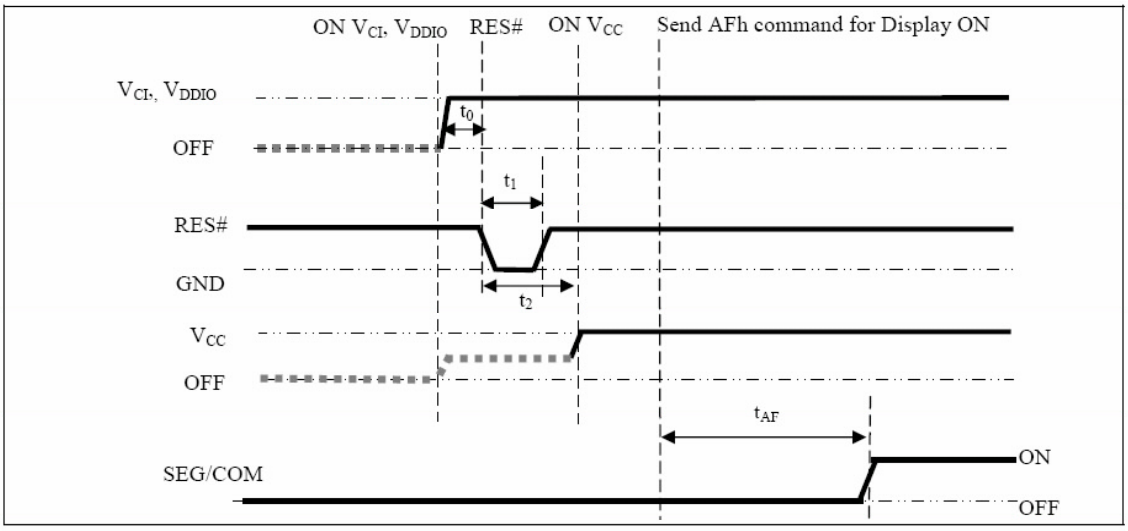
POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351.

Power ON sequence：

1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1)(4) and then HIGH(logic high).
3. After set RES# pin LOW(logic low), wait for at least 2us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).
5. After V_{CI} become stable, wait for at least 300ms to send command.

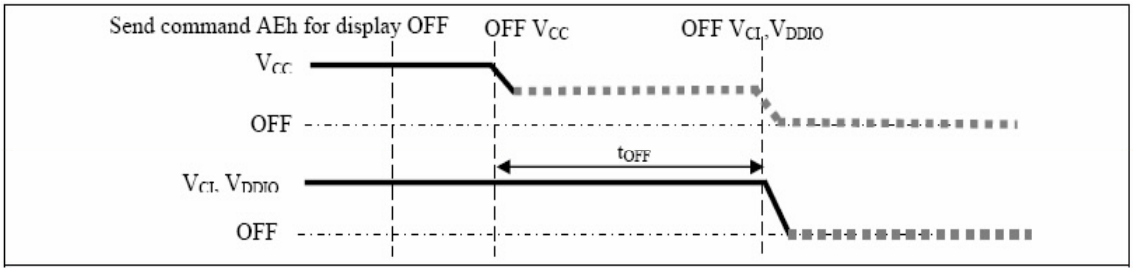
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO} (where Minimum t_{OFF}=80ms(3),Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above Figure.

(2) V_{CC} should be disable when it is OFF.

(3) V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

(4) The register values are reset after t_1.

(5) Power pins (V_{CI}, V_{DDIO} and V_{CC}) can never be pulled to ground under any circumstance.

Thank You