P22201

128x3x96 Full Color
Application Notes
(For 8080 8 bits Interface)

Revision History

Version	Content
X01	First release (For 8080 8bits Interface)

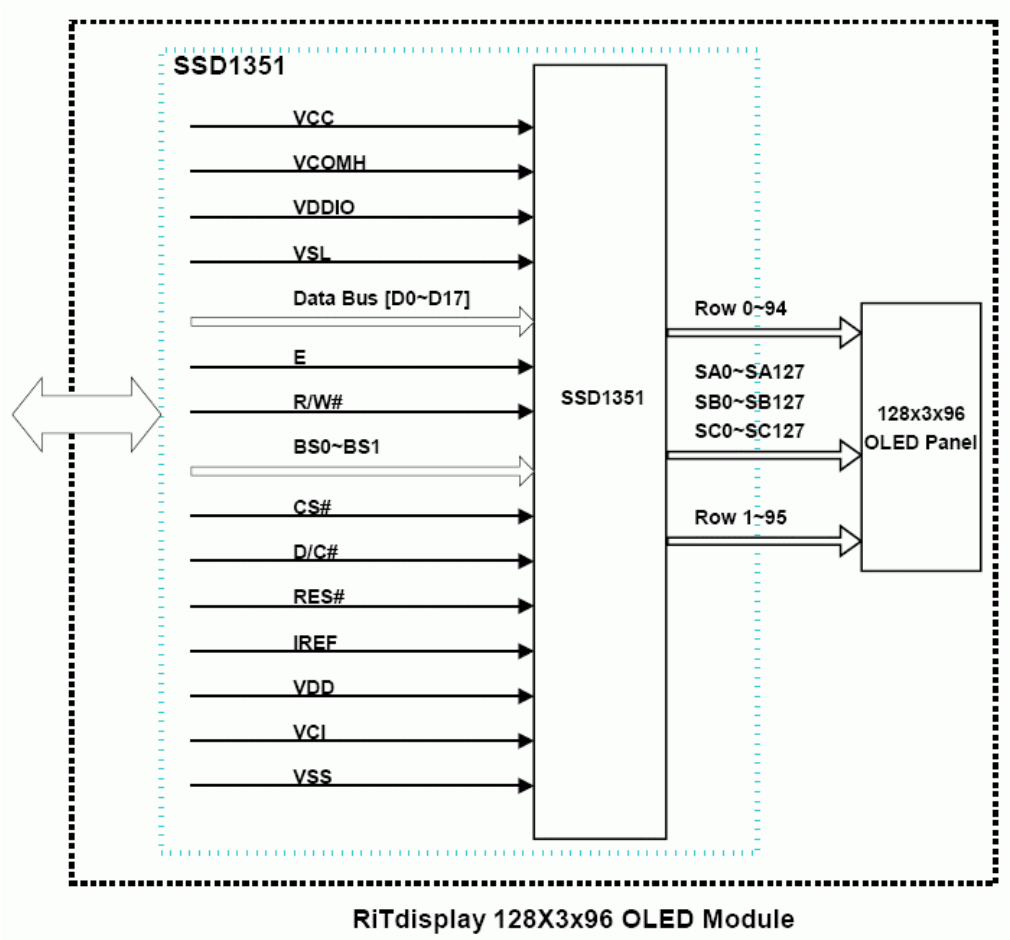
DESCRIPTION

P22201 is a 128x3x96 full color passive OLED module with controller for many compact portable applications.

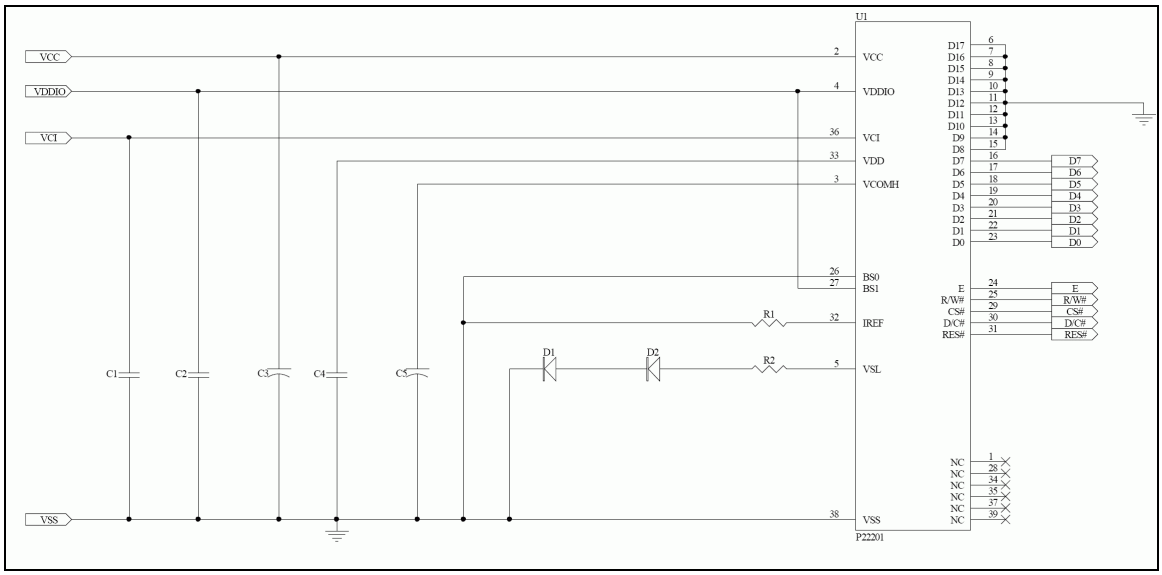
FEATURE

- 128x3x96 dot matrix full color OLED panel.
- Driver IC is SSD1351.
- VCC =15V
- VCI =2.4V~3.5V
- VDDIO =1.65V~ VCI
- Embedded 128x128x18 bit SRAM display buffer.
- 8/16/18 bits 6800-series parallel interface, 8/16/18 bits 8080-series parallel interface, Serial Peripheral Interface.
- Vertical and horizontal scrolling.
- Programmable color mode of 65k, 262k.
- Programmable Frame Rate and Multiplexing Ratio.

FUNCTION BLOCK DIAGRAM



Application circuit



Recommend components:

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

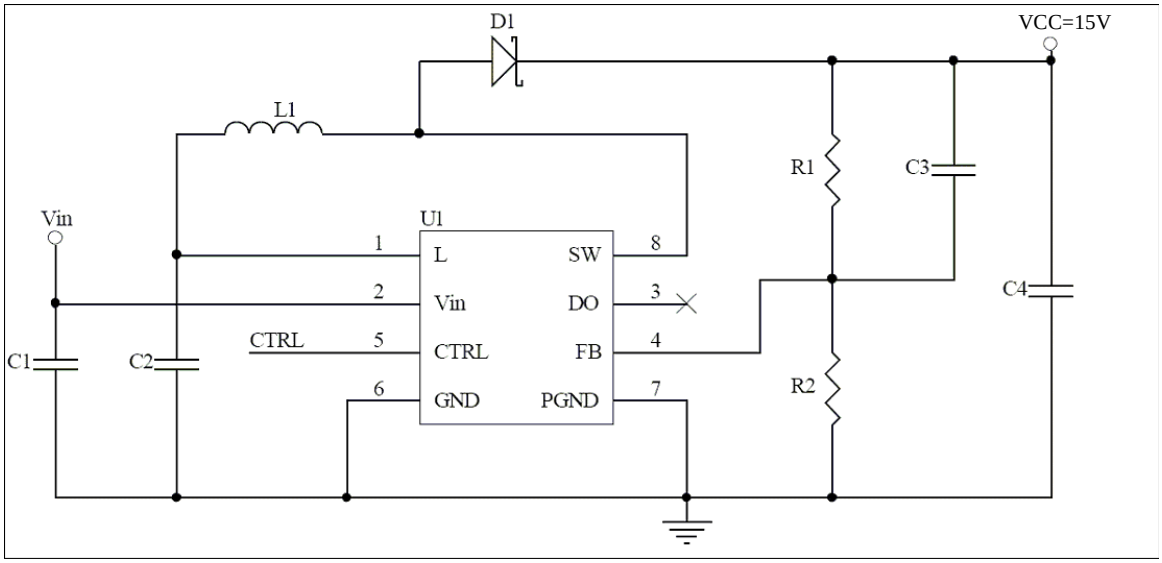
R1: 1M ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 8bits interface

DC-DC application circuit for OLED module



Recommend components:

The C1: 0.1uF/6.3V.

The C2: 4.7 uF/6.3V.

The C3: 22pF/16V.

The C4: 4.7uF/35V Tantalum type capacitor.

The R1: 1.2M ohm 1%.

The R2: 108K ohm 1%.

The D1: SCHOTTY DIODE.

The L1: 10uH.

The U1: HPA00483DRBR

The R1, R2 and C3 value should be fine tune by customer.

NOTE a. The HPA00483DRBR is low cost DC/DC for TI.

b. The HPA00483DRBR spec. is same as TPS61045.

Pin Assignments

PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VCC	2	Power supply for panel driving voltage.
VCOMH	3	COM signal deselected voltage level. A capacitor should be connected between this pin an VSS.
VDDIO	4	Power supply for interface logic level.
VSL	5	This is segment voltage reference pin.
D17	6	These pins are bi-directional data bus connecting to the MCU data bus.
D16	7	
D15	8	
D14	9	
D13	10	
D12	11	
D11	12	
D10	13	
D9	14	
D8	15	
D7	16	
D6	17	
D5	18	
D4	19	
D3	20	
D2	21	
D1	22	
D0	23	
E	24	8080: data read enable pin; 6800:Read/Write enable pin.
R/W#	25	8080: data write enable pin; 6800:Read/Write select pin.
BS0	26	Interface select pin.
BS1	27	Interface select pin.
NC	28	No connection.
CS#	29	Chip select pin.
D/C#	30	H: Data, L: Command.
RES#	31	Hardware Reset pin (Low active).
IREF	32	A resistor should be connected between this pin and VSS.
VDD	33	Power supply pin for core logic operation.
NC	34	No connection.
NC	35	No connection.
VCI	36	Digital voltage power supply.
NC	37	No connection.
VSS	38	Ground.
NC	39	No connection.

Application Initial Setting

```
/*128x3x96 OLED driver program */
void initial(void)
{
comm_out(0xfd);      //Set Command Lock
data_out (0xb1);      //Unlock OLED driver IC

comm_out(0xae);      //Display off

comm_out(0xa0);      //Set Re-map Color Depth
data_out (0x64);      //65K Color

comm_out(0xa1);      //Set Display Start Line
data_out (0x00);

comm_out(0xa2);      //Set Display Offset
data_out (0x00);

comm_out(0xa6);      //Normal display

comm_out(0xab);      //Function Selection
data_out (0x01);

comm_out(0xb1);      //Set Reset (Phase 1) /Pre-charge (Phase 2) period
data_out (0x53);

comm_out(0xb3);      //Set frame rate
data_out (0xf1);

comm_out(0xb4);      //External VSL
data_out (0xa0);
data_out (0xb5);
data_out (0x55);

comm_out(0xb9);      //Use Built-in Linear LUT

comm_out(0xbb);      //Set Pre-charge voltage
data_out (0x00);
```

```
comm_out(0xbe);       //Set VCOMH
data_out (0x07);

comm_out(0xc1);       //Set contrast level for R,G,B
data_out (0x6c);      //Red contrast set
data_out (0x99);      //Green contrast set
data_out (0x79);      //Blue contrast set

comm_out(0xc7);       //Master current control
data_out (0x06);

comm_out(0xca);       //Set MUX Ratio
data_out (0x5f);      //96 duty

comm_out(0xaf);       //Display on
}
```

```
write_red_data(void)
{
int i,j;
   ram _address( );
   comm_out(0x5c);
      for(i=0;i<96;i++)
       {
         for(j=0;j<128;j++)
         {
         data_out(0xf8);//Red
         data_out(0x00);
         }
       }
}
write_green_data(void)
{
int i,j;
   ram _address( );
   comm_out(0x5c);
      for(i=0;i<96;i++)
       {
         for(j=0;j<128;j++)
         {
         data_out(0x07);//Green
         data_out(0xe0);
         }
}
write_blue_data(void)
{
int i,j;
   ram _address( );
   comm_out(0x5c);
      for(i=0;i<96;i++)
       {
         for(j=0;j<128;j++)
         {
         data_out(0x00);//Blue
         data_out(0x1f);
```

```
        }
      }
}
write_white_data(void)
{
int i,j;
   ram _address( );
   comm_out(0x5c);
      for(i=0;i<96;i++)
       {
         for(j=0;j<128;j++)
         {
         data_out(0xff);//White
         data_out(0xff);
         }
       }
}
ram _address(void);
{
comm_out(0x15);
data_out(0x00);          //column start address
data_out(0x7f);           //column end address
comm_out(0x75);
data_out(0x00);          //row start address
data_out(0x5f);          //row end address
}
```

For 120 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode1 (void);
{
comm_out(0xc7);       //Master current control
data_out(0x07);
comm_out(0xc1);       //Set contrast level
data_out(0x72);       //Red contrast set
data_out(0xa4);       //Green contrast set
data_out(0x7e);       //Blue contrast set
}
```

For 100 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode2 (void);
{
comm_out(0xc7);       //Master current control
data_out(0x06);
comm_out(0xc1);       //Set contrast level
data_out(0x6c);       //Red contrast set
data_out(0x99);       //Green contrast set
data_out(0x79);       //Blue contrast set
}
```

For 80 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode3 (void);
{
comm_out(0xc7);       //Master current control
data_out(0x05);
comm_out(0xc1);       //Set contrast level
data_out(0x69);       //Red contrast set
data_out(0x91);       //Green contrast set
data_out(0x72);       //Blue contrast set
}
```

For 60 cd/m^2 setting, user could follow the below setting.

```
Brightness_mode4 (void);
{
comm_out(0xc7);       //Master current control
data_out(0x04);
```

```
comm_out(0xc1);        //Set contrast level
data_out(0x66);        //Red contrast set
data_out(0x87);        //Green contrast set
data_out(0x6d);        //Blue contrast set
}
```

For 40 cd/m^2 setting, user could follow the below setting.

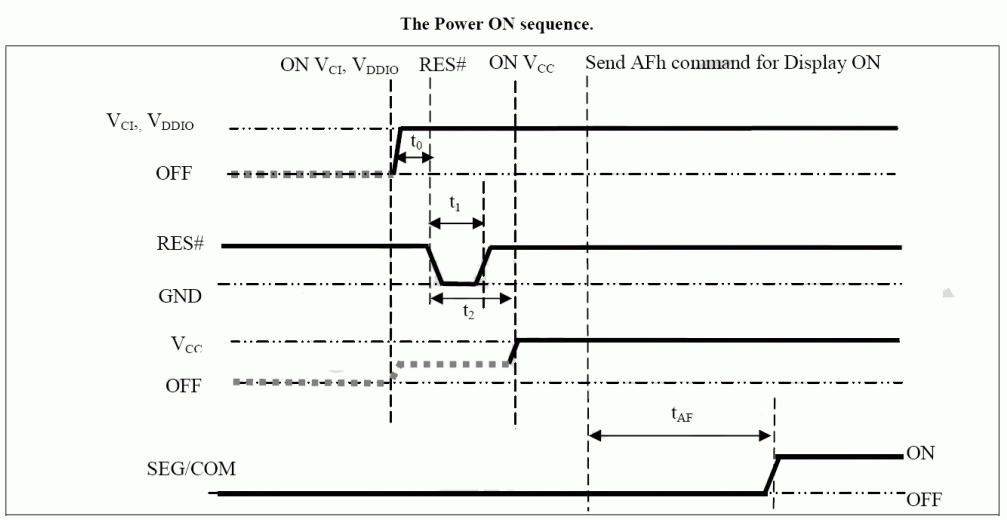
```
Brightness_mode5 (void);
{
comm_out(0xc7);        //Master current control
data_out(0x03);
comm_out(0xc1);        //Set contrast level
data_out(0x61);        //Red contrast set
data_out(0x7c);        //Green contrast set
data_out(0x67);        //Blue contrast set
}
```

Power ON / OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

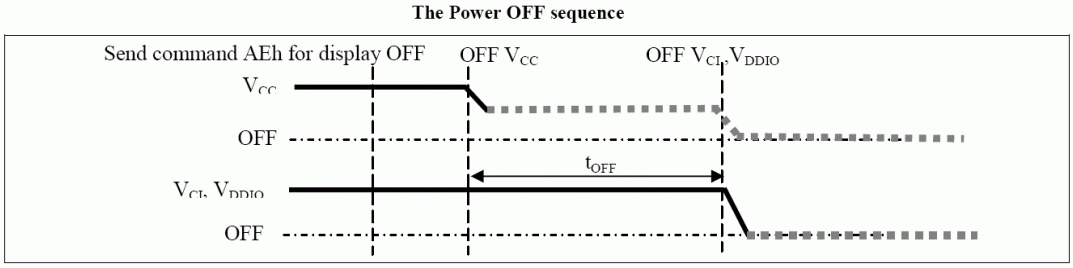
***Power ON sequence*:**

1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2)
3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO}.(where Minimum t_{OFF}=80ms (3), Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI},V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be kept float (disable) when it is OFF.

(3) V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

(4) The register values are reset after t_1.

(5) Power pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	.....	.....	126	127		
	Remapped	127			126			125	.....	.....	1	0		
Color		A	B	C	A	B	C	A			C	A	B	C
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0
Normal	Remapped													
0	127	6	6	6	6	6	6	6	.....	.....	6	6	6	6
1	126	6	6	6	6	6	6	6	.....	.....	6	6	6	6
2	125	6	6	6	6	6	6	6	.....	.....	6	6	6	6
3	124	6	6	6	6	6	6	6	.....	.....	6	6	6	6
4	123	6	6	6	6	6	6	6	.....	.....	6	6	6	6
5	122	6	6	6	6	6	6	6	.....	.....	6	6	6	6
6	121	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6
7	120								.....	.....	6	6	6	6
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
123	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6
124	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6
125	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6
126	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6
127	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

Common output
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
:
:
:
:
COM124
COM125
COM126
COM127

Thank You