P16807

160x3x128 Full Color

Application Notes

Revision History

Version	Content
X01	First release
A01	Modified Initial Setting (remove 0xad command) Modified Power On/Off Sequence.
A02	Add Brightness 60cd/m^2 、40cd/m^2 Setting
A03	Modify Application Initial Setting

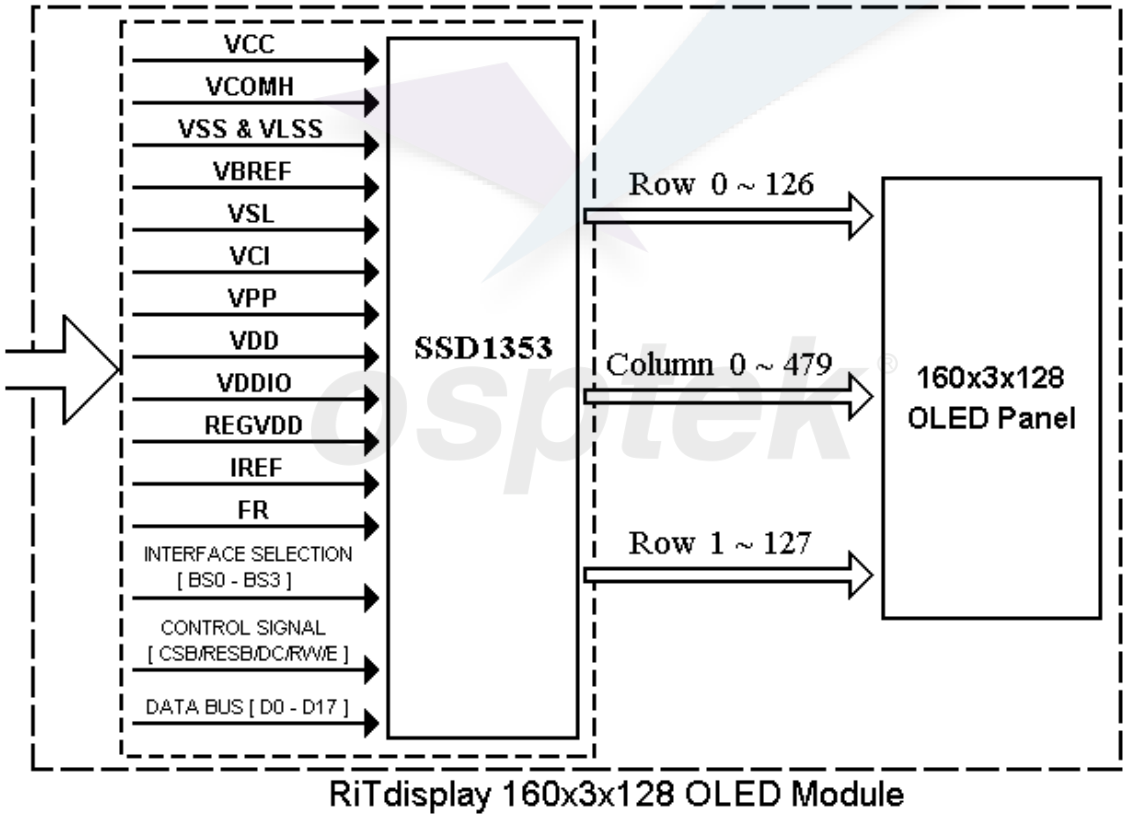
DESCRIPTION

P16807 is a 160x3x128 dot for the 262k-Color OLED module.

FEATURE

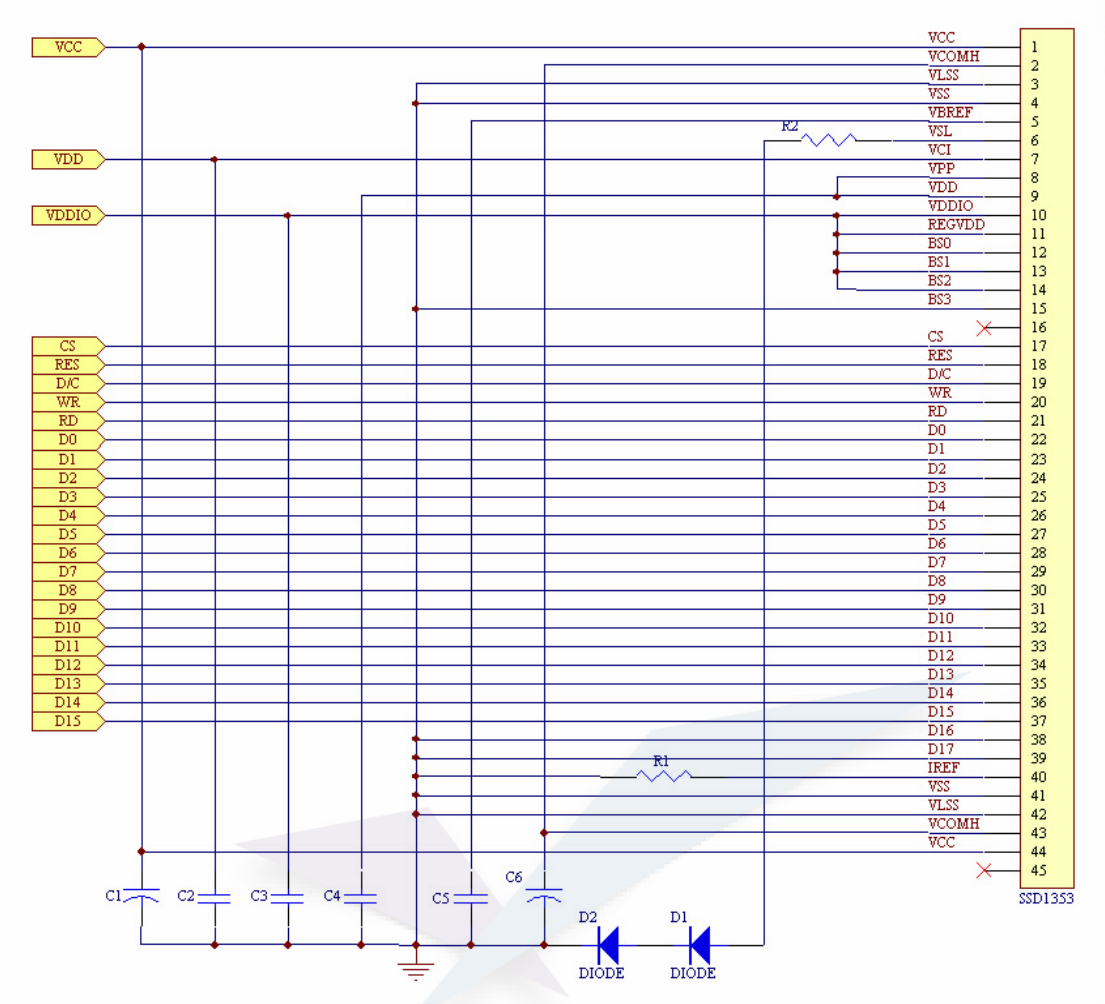
- 160x3x128 dot matrix full color OLED panel.
- Driver IC SSD1353.
- VCC = 17V
- VCI = 2.4V~3.5V
- VDDIO = 1.6V~VCI
- Embedded 160x132x18 bit SRAM display buffer.
- 8/16/18bits -6800 / 8080 series parallel interface, Serial Peripheral interface.
- Horizontal Scrolling.
- Programmable color mode of 256, 65k, 262k.
- Programmable Frame Rate.

FUNCTION BLOCK DIAGRAM



RiTdisplay 160x3x128 OLED Module

APPLICATION CIRCUIT



Recommend components:

C1, C6: 4.7 uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C2, C3, C4: 1 uF/16V(0805)

C5: 0.1 uF/16V

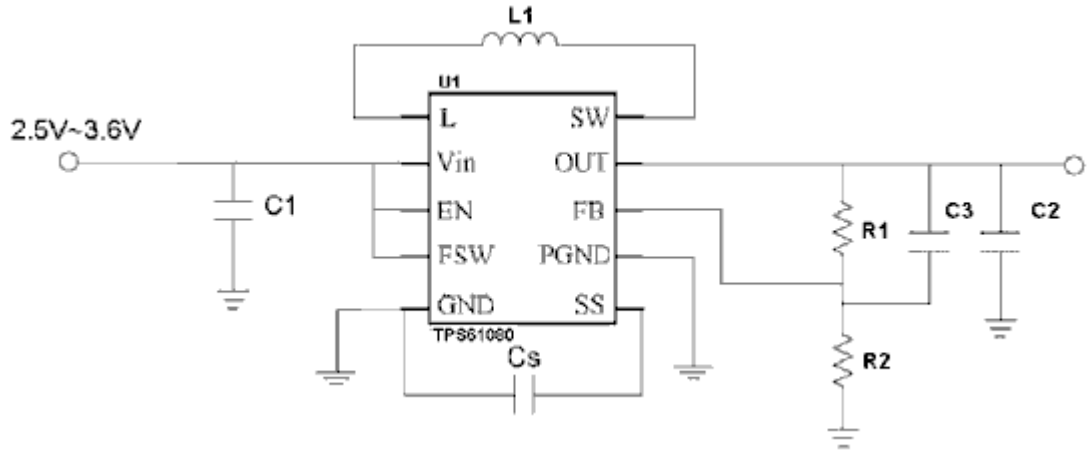
R1: 1.2M ohm 1%(0603)

R2: 50ohm 1/4W

D1 and D2: RB480K (ROHM)

This circuit is for 8080 16bits interface

DC-DC application circuit for OLED module



Recommend components:

The C1: 4.7uF/6.3V.

The C2: 4.7 uF/35V Tantalum type capacitor.

The C3: 50pF/16V.

The Cs: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 96K ohm/ 1%.

The L1: 4.7uH.

The U1: TPS61080

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	VCC	Power supply for panel driving voltage.
2	VCOMH	A capacitor should be connected between this pin and VSS.
3	VLSS	Analog system ground pin.
4	VSS	Ground pin.
5	VBREF	Connect to ground with a capacitor.
6	VSL	This is segment voltage reference pin.
7	VCI	Low voltage power supply.
8	VPP	Connect to VDD.
9	VDD	Power supply input for logic.
10	VDDIO	Power supply for interface logic level.It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VCI.
11.	REGVDD	Internal VDD regulator selection pin. When this pin is pulled high,internal VDD regulator is enabled. When this pin is pulled low,external VDD regulator is used.
12	BS0	Interface selection pins.
13	BS1	
14	BS2	
15	BS3	
16	FR	It should be kept NC.
17	CSB	This pad is the chip select input. Low active.
18	RESB	This is a reset signal input. Low active.
19	DC	D/C=”H”: Data. D/C=”L”: Command.
20	RW	When connected to 8080-series MPU. WR pin. When RW =”L”: Write signal input. When connected to 6800-series MPU. When RW =”H”: Read. When RW =”L”: Write.
21	E	When connected to 8080-series MPU. RD pin. When E =”L”: Read signal input. When connected to 6800-series MPU. Enable clock input of the 6800 series MPU.
22	D0	18 bit / 16bit / 9bit / 8 bit Data bus I/O.
23	D1	
24	D2	
25	D3	
26	D4	
27	D5	
28	D6	
29	D7	

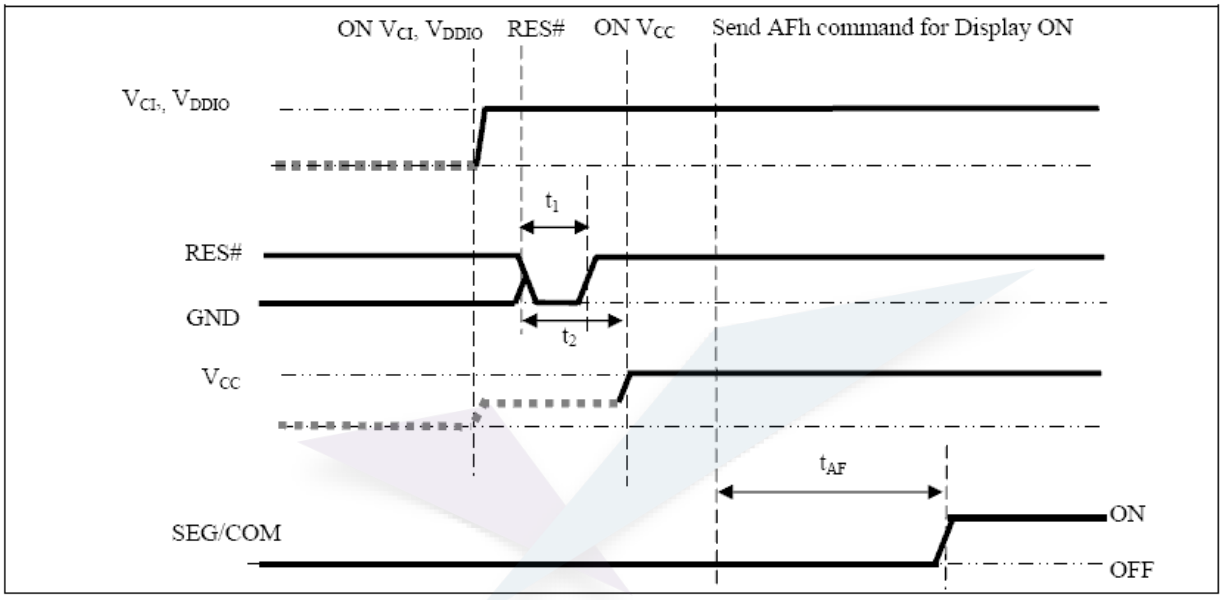
30	D8	
31	D9	
32	D10	
33	D11	
34	D12	
35	D13	
36	D14	
37	D15	
38	D16	
39	D17	
40	IREF	A resistor should be connected between this pin and VSS.
41	VSS	Ground pin.
42	VLSS	Analog system ground pin.
43	VCOMH	A capacitor should be connected between this pin and VSS.
44	VCC	Power supply for panel driving voltage.
45	NC	No connection.

Power ON / OFF Sequence

Power ON sequence:

1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 100us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} (1).
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

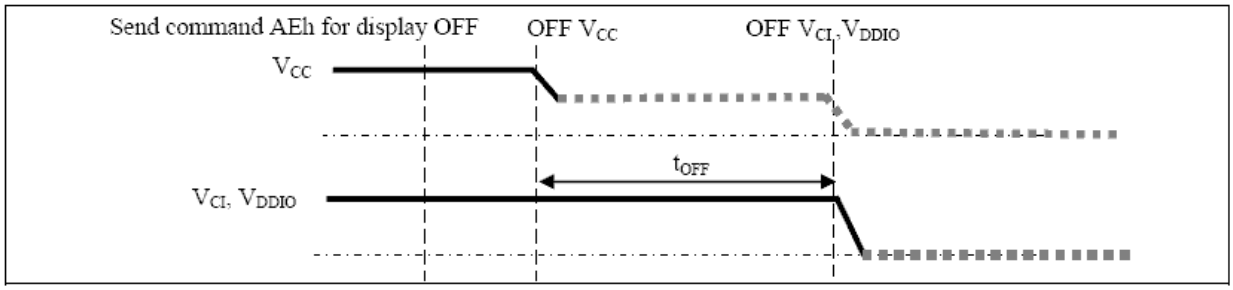
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2).
3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO}.(Where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI},V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
(2) V_{CC} should be disabled when it is OFF.

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160x132x18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment	Normal	0			1			2	.....	.....	158	159			
Address	Remapped	159			158			157	.....	.....	1	0			
Color		A	B	C	A	B	C	A	.....	.....	C	A	B	C	
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common output
Normal	Remapped														
0	131	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	130	6	6	6					.....	.....					COM1
2	129								.....	.....					COM2
3	128								.....	.....					COM3
4	127								.....	.....					COM4
5	126								.....	.....					COM5
6	125			no of bits in this cell					.....	.....					COM6
7	124								.....	.....					COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
127	4								.....	.....					
128	3								.....	.....					COM128
129	2								.....	.....					COM129
130	1								.....	.....					COM130
131	0								.....	.....					COM131

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC158	SA159	SB159	SC159

Application Initial Setting

```
/* 160x3x128 OLED driver program */
void initial(void)
{
comm_out(0xae);        //Display off
comm_out(0xa8);        //Set MUX ratio
data_out(0x7f);
comm_out(0xa1);        //Display start line
data_out(0x00);
comm_out(0xa2);        //Set display offset
data_out(0x00);
comm_out(0xa4);        //Normal display
comm_out(0xa0);        //Set re-map
data_out(0x64);
comm_out(0x87);        //Master current control
data_out(0x0f);
comm_out(0x81);        //Set contrast level for R
data_out(0x75);         //Red contrast set
comm_out(0x82);        //Set contrast level for G
data_out(0x60);         //Green contrast set
comm_out(0x83);        //Set contrast level for B
data_out(0x6a);         //Blue contrast set
comm_out(0xb1);        //Phase adjust
data_out(0x22);
comm_out(0xb3);        //Set frame rate
data_out(0x40);
comm_out(0xbb);        //Set Pre-charge level
data_out(0x08);
comm_out(0xbe);        //VCOMH setting
data_out(0x3c);
comm_out(0xb9);
comm_out(0xaf);         //Display on
}

write_red_data(void)
{
int i;
ram _address( );
```

```
comm_out(0x5c);
for(i=0;i<20480;i++)
   {
    data_out(0xf800);     //RED
   }
}

write_green_data(void)
{
int i;
ram _address( );
comm_out(0x5c);
for(i=0;i<20480;i++)
   {
    data_out(0x07e0);     //GREEN
   }
}

write_blue_data(void)
{
int i;
ram _address( );
comm_out(0x5c);
for(i=0;i<20480;i++)
   {
    data_out(0x001f);     //BLUE
   }
}

write_white_data(void)
{
int i;
ram _address( );
comm_out(0x5c);
for(i=0;i<20480;i++)
   {
    data_out(0xffff);      //WHITE
    }
```

```
}

ram _address(void);
{
comm_out(0x15);          //Set Column Address
data_out(0x00);          //Column Start Address
data_out(0x9f);          //Column End Address
comm_out(0x75);          //Set Row Address
data_out(0x00);          //Row Start Address
data_out(0x7f);          //Row End Address
```

For 80 cd/m2 setting, user could follow the below setting.

```
Brightness_mode3 (void);
{
comm_out(0x87);        //Master current control
data_out(0x0f);
comm_out(0x81);        //Set contrast level for R
data_out(0x75);         //Red contrast set
comm_out(0x82);        //Set contrast level for G
data_out(0x60);         //Green contrast set
comm_out(0x83);        //Set contrast level for B
data_out(0x6a);         //Blue contrast set
}
```

For 60 cd/m2 setting, user could follow the below setting.

```
Brightness_mode4 (void);
{
comm_out(0x87);        //Master current control
data_out(0x0b);
comm_out(0x81);        //Set contrast level for R
data_out(0x86);         //Red contrast set
comm_out(0x82);        //Set contrast level for G
data_out(0x69);         //Green contrast set
comm_out(0x83);        //Set contrast level for B
data_out(0x7c);         //Blue contrast set
}
```

For 40 cd/m2 setting, user could follow the below setting.

```
Brightness_mode5 (void);
{
comm_out(0x87);        //Master current control
data_out(0x05);
comm_out(0x81);        //Set contrast level for R
data_out(0x80);         //Red contrast set
comm_out(0x82);        //Set contrast level for G
data_out(0x6b);         //Green contrast set
comm_out(0x83);        //Set contrast level for B
data_out(0x7f);         //Blue contrast set
}
```

Thank You