Osptek Display

OLED SPECIFICATION

Model No:

OED208-25664W003-C14

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2016. 08. 05	

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by Osptek. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

2. WARRANTY

Osptek warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Osptek is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored in the original packages at 25℃±5℃, 55%±10%RH or used as the conditions specified in the specifications.

Nevertheless, Osptek is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- 16 gray scale.
- Panel resolution : 256x64
- Driver IC : SH1122G
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism desi gn : 1.61 mm
- High contrast : 10,000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 4 wire serial peripheral interface.
- Wide range of operating temperature : -40 to 70℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	256 x 64	dot
2	Dot Size	0.18 (W) x 0.18 (H)	mm^2
3	Dot Pitch	0.2 (W) x 0.2 (H)	mm^2
4	Aperture Rate	81	%
5	Active Area	51.18 (W) x 12.78 (H)	mm^2
6	Panel Size	62.5 (W) x 20.6 (H)	mm^2
7*	Panel Thickness	1.61 ± 0.1	mm
8	Module Size	88.0 (W) x 20.6 (H) x 1.61 (T)	mm^3
9	Diagonal A/A size	2.08	inch
10	Module Weight	4.45 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD1})	-0.3	3.6	V	Ta = 25℃	IC maximum rating
Supply Voltage (V_{PP})	8	14.5	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃	-	-
Storage Temp	-40	85	℃	-	Note (2)

Note:

(1) Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the section 6. Electrical Characteristics tables.

(2) The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{PP}	Analog power supply (for OLED panel)	Ta 25℃	11.5	12	12.5	V
V_{DD1}	Digital power supply	Ta 25℃	1.65	-	3.5	V
V_{IH}	High logic input level		0.8* V_{DD1}	-	V_{DD1}	V
V_{IL}	Low logic input level		V_{SS}	-	0.2* V_{DD1}	V
V_{OH}	High logic output level	I_{OH} = -0.5mA	0.8* V_{DD1}	-	V_{DD1}	V
V_{OL}	Low logic output level	I_{OL} = 0.5mA	V_{SS}	-	0.2* V_{DD1}	V

Note: The V_{PP} input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current (IPP)	-	38	43	mA	All pixels on (1)
	-	15	16	mA	30% pixels on (1)
Standby mode current (IPP)	-	3	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	456	516	mW	All pixels on (1)
	-	180	192	mW	30% pixels on (1)
Standby mode power consumption	-	36	48	mW	Standby mode 10% pixels on (2)
IDD1 sleep mode current	-	-	5	uA	Sleep mode Current (3)
IPP sleep mode current	-	-	5	uA	Sleep mode Current (3)
Normal mode Luminance	130	180		cd/m^2	Display Average
Standby Luminance		70		cd/m^2	
CIEx (White)	0.27	0.30	0.33		CIE1931
CIEy (White)	0.30	0.33	0.36		CIE1931
Dark Room Contrast	10000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x3a
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x02
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Sleep mode condition :

When send 0xae command OLED display off and memory data will be maintained.

(4) Wake up condition :

When send 0xaf command OLED will be turned on.

7. LIFETIME SPECIFICATION

ITEM	MIN	UNIT	Condition	Remark
Life Time	6,000	Hrs	230 cd/m^2, 50% checkerboard	Note (1)
Life Time	10,000	Hrs	180 cd/m^2, 50% checkerboard	Note (2)
Life Time	19,000	Hrs	130 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under VPP = 12V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 230 cd/m^2 :

- Contrast setting : 0x55
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 180 cd/m^2 :

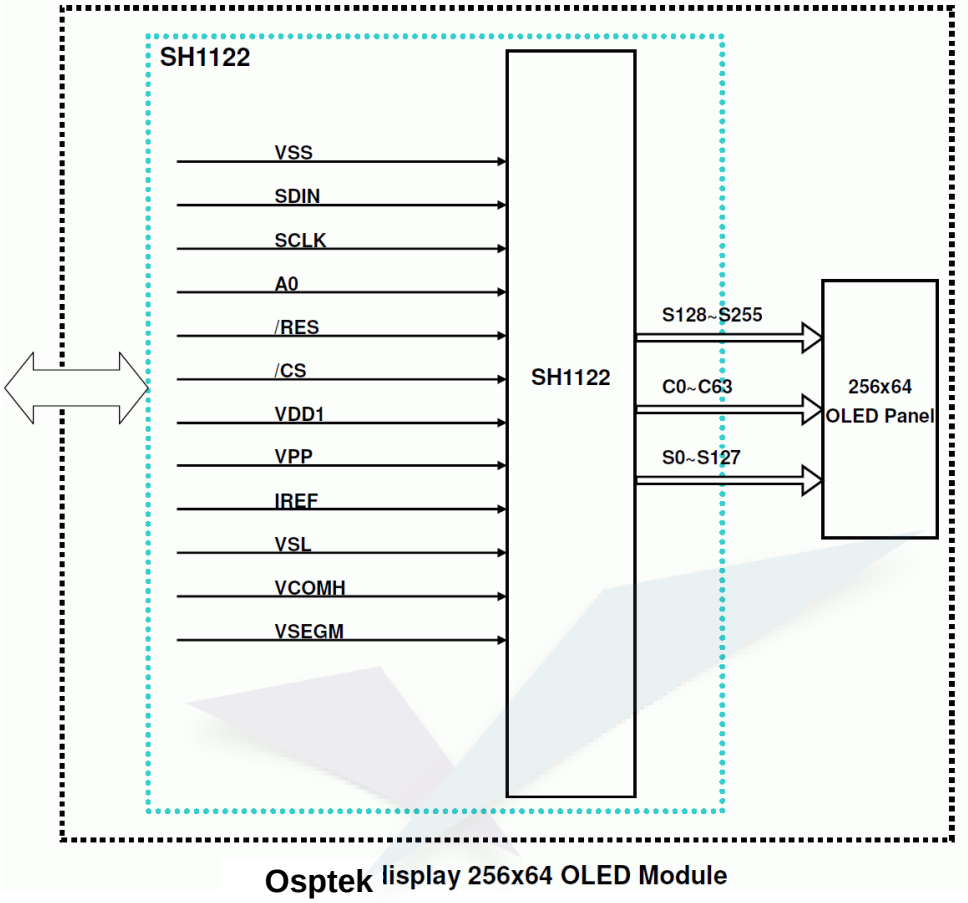
- Contrast setting : 0x3a
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 130 cd/m^2 :

- Contrast setting : 0x1e
- Frame rate : 105Hz
- Duty setting : 1/64

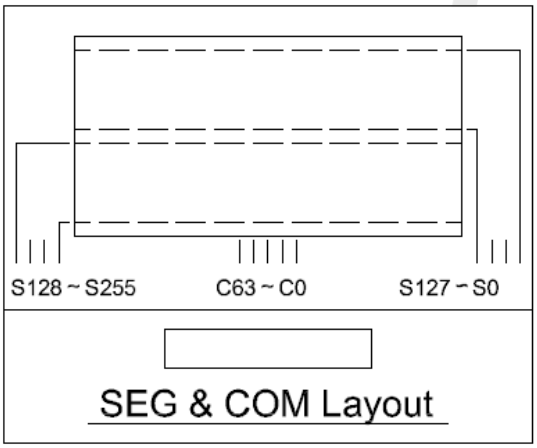
8. INTERFACE

8.1 FUNCTION BLOCK DIAGRAM



Osptek lisplay 256x64 OLED Module

8.2 PANEL LAYOUT DIAGRAM



8.3 PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION
VSS	1	Ground pin.
SDIN	2	When the serial interface is selected, then D0 serves as the serial clock input pin (SCL) and D1 serves as the serial data input pin (SI).
SCLK	3	
A0	4	This is the Data/Command control pin that determines whether the data bits are data or a command.
/RES	5	This is a reset signal input pin. When RES is set to “L”, the settings are initialized.
/CS	6	This pin is the chip select input. When CS = “L”, then the chip select becomes active, and data/command I/O is enabled.
VDD1	7	Power supply for logic and input/output.
VSS	8	Ground pin.
NC	9	No connection.
VPP	10	Power supply for panel driving voltage.
IREF	11	This is a segment current reference pin. A resistor should be connected between this pin and VSS.
VSL	12	This is a segment voltage reference pin. A capacitor should be connected between this pin and VSS.
VCOMH	13	This is voltage output high level for common signals. A capacitor should be connected between this pin and VSS.
VSEGM	14	This is voltage output high level for segment pre-charge. A capacitor should be connected between this pin and VSS.

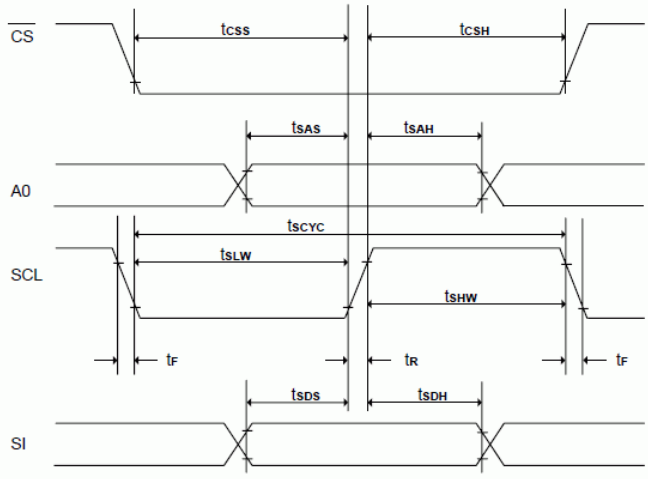
8.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 256 X 64 X 4 bits.
For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.
For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Row \ Column		COL0								---	COL127							
0		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
1		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
2		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
---										---								
62		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
63		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
ADC	= 0	SEG0				SEG1				---	SEG254				SEG255			
	= 1	SEG255				SEG254				---	SEG1				SEG0			

8.5 INTERFACE TIMING CHART

System buses Write characteristics (For 4 wire SPI)



(V_{DD1} = V_{DD2} =1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSAS	Address setup time	300	-	-	ns	
tSAH	Address hold time	300	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

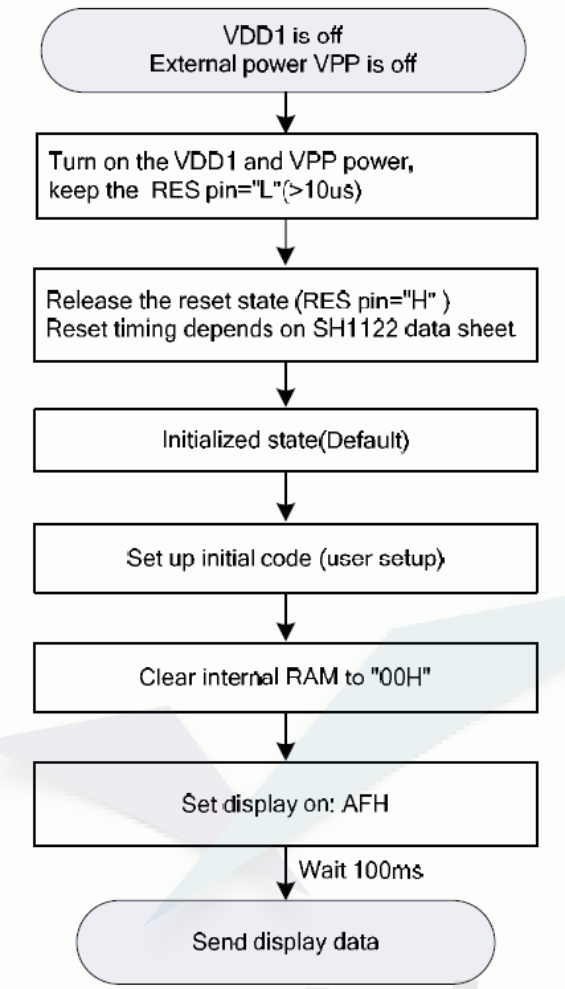
(V_{DD1} = V_{DD2} = 2.4 – 3.5V, TA = +25°C)

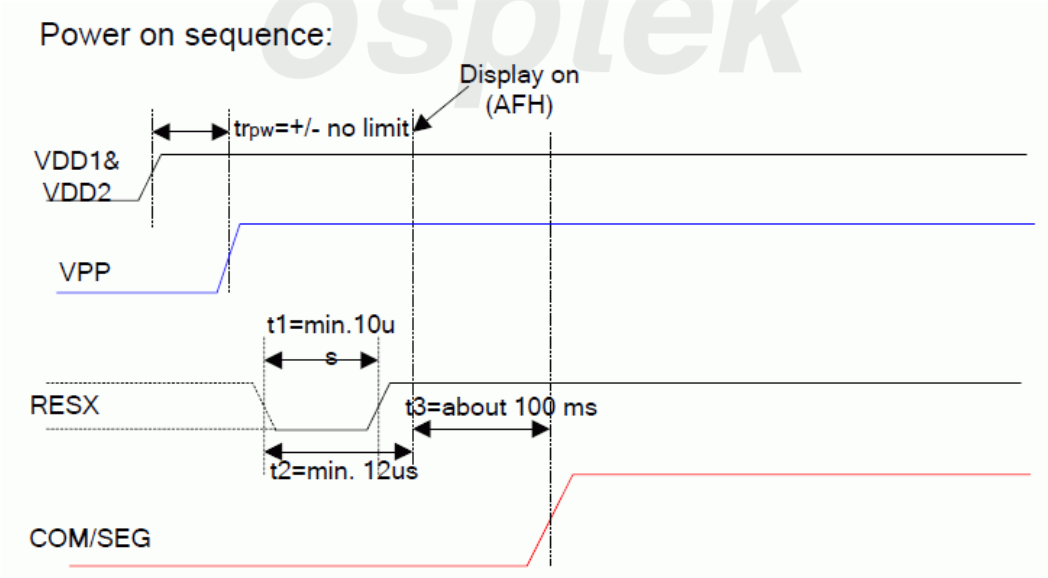
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSAS	Address setup time	150	-	-	ns	
tSAH	Address hold time	150	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

9. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

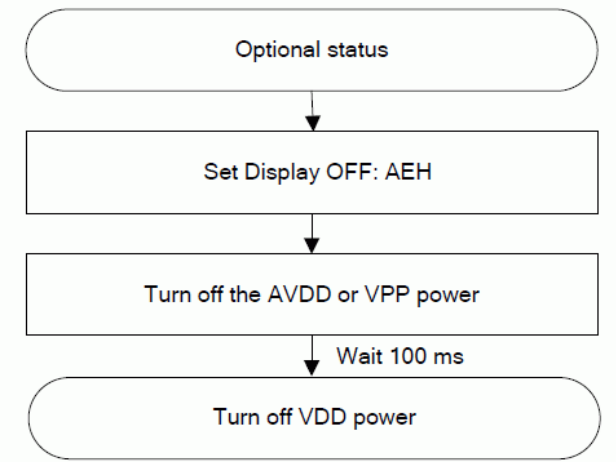
9.1 POWER ON / OFF SEQUENCE

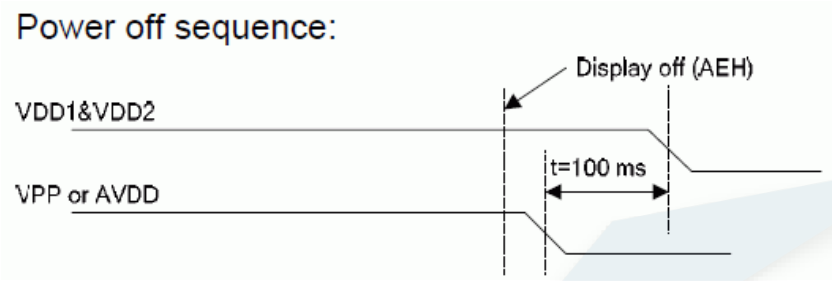
POWER ON



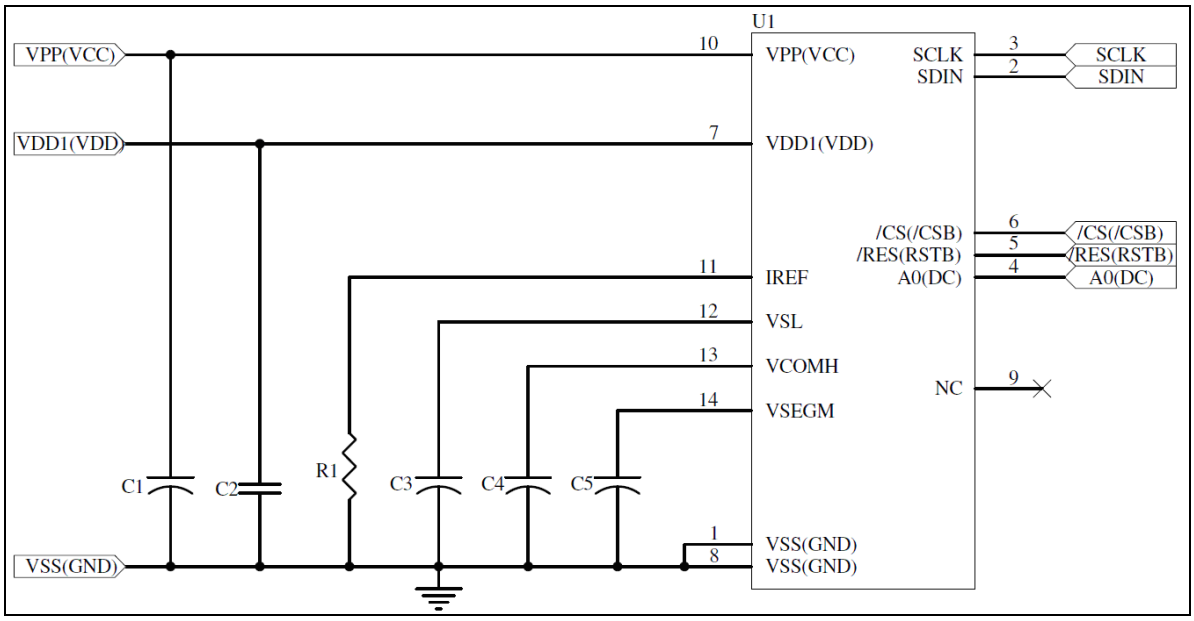


POWER OFF





9.2 APPLICATION CIRCUIT



Recommend components:

C1, C3, C4, C5: 4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C2: 1uF/16V(0603)

R1: 620K ohm 1%(0603)

This circuit is for SPI interface.

9.3 COMMAND TABLE

Refer to IC Spec.: SH1122G

10. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

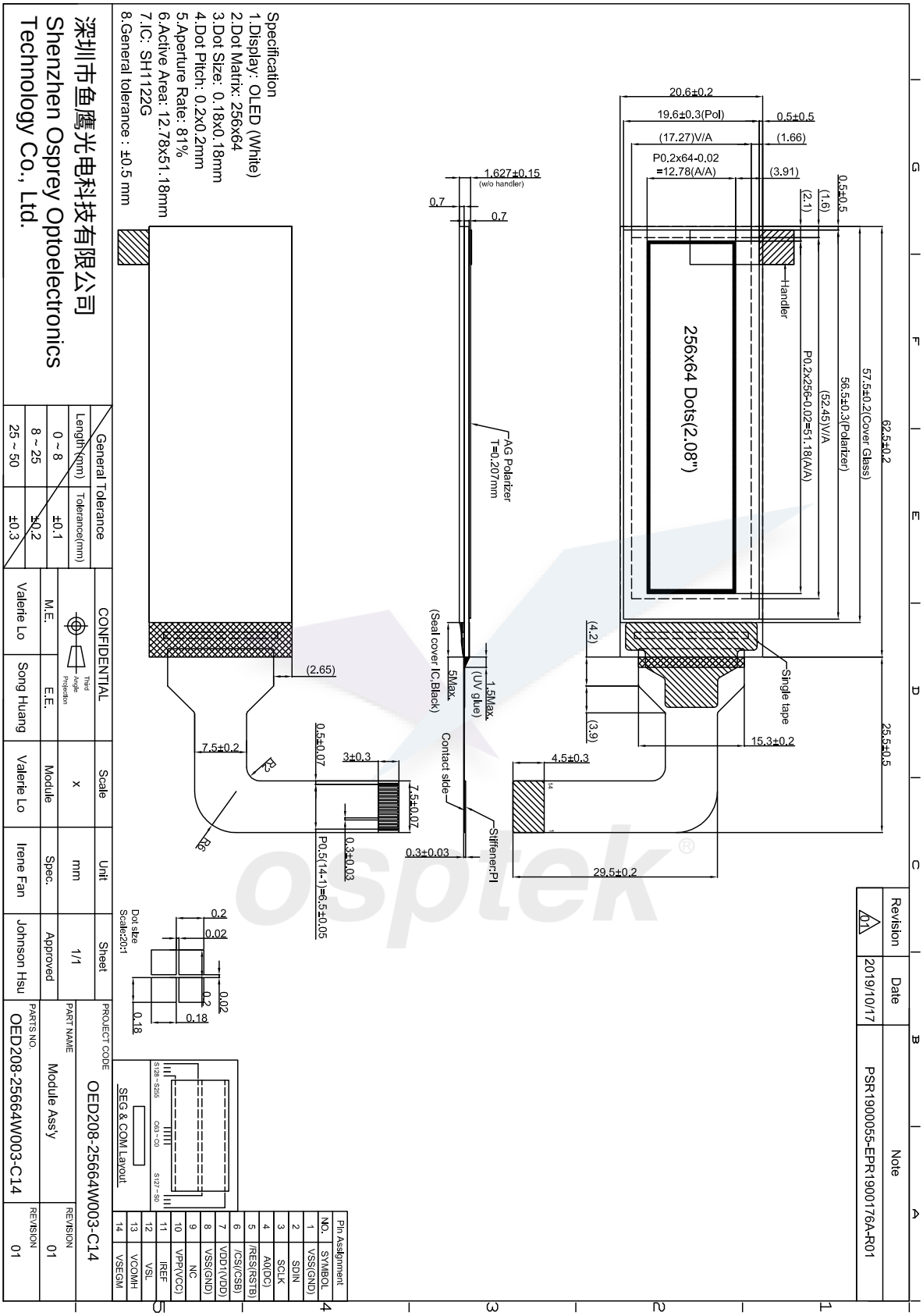
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

11. EXTERNAL DIMENSION



12. PACKING SPECIFICATION

TBD

13. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

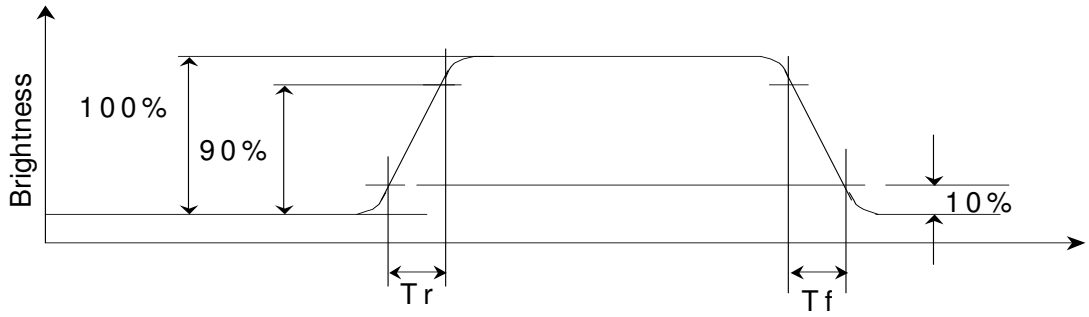


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

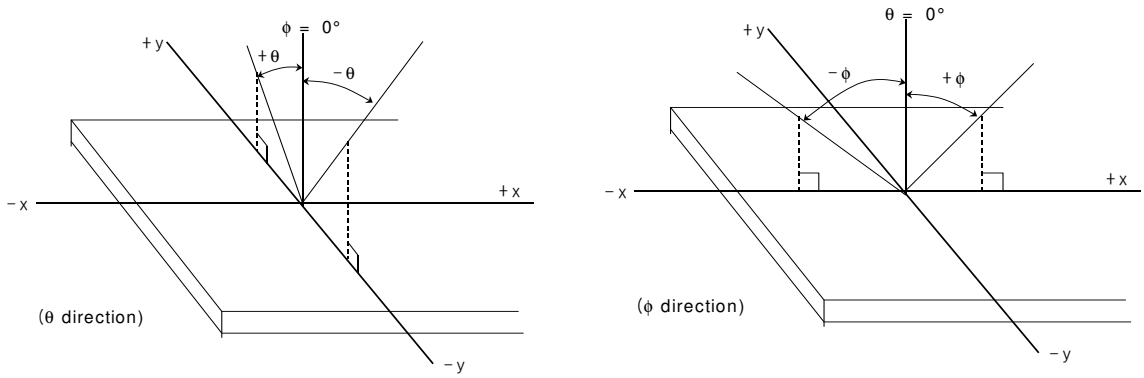
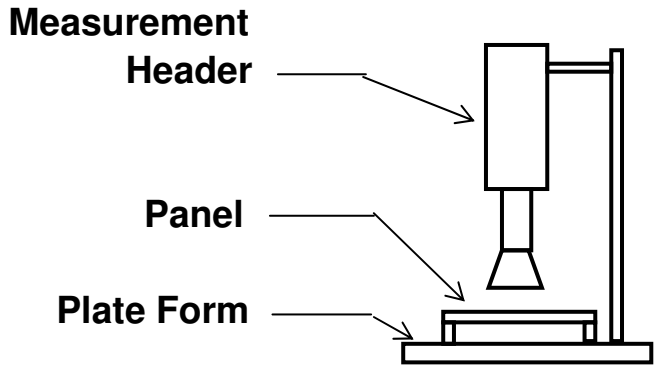


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

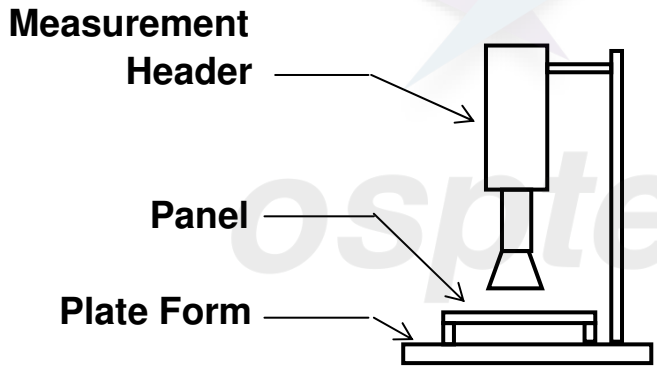
PHOTO RESEARCH PR-705, MINOLTA CS-100



PR-705 /
MINOLTA CS-100
Color Analyzer

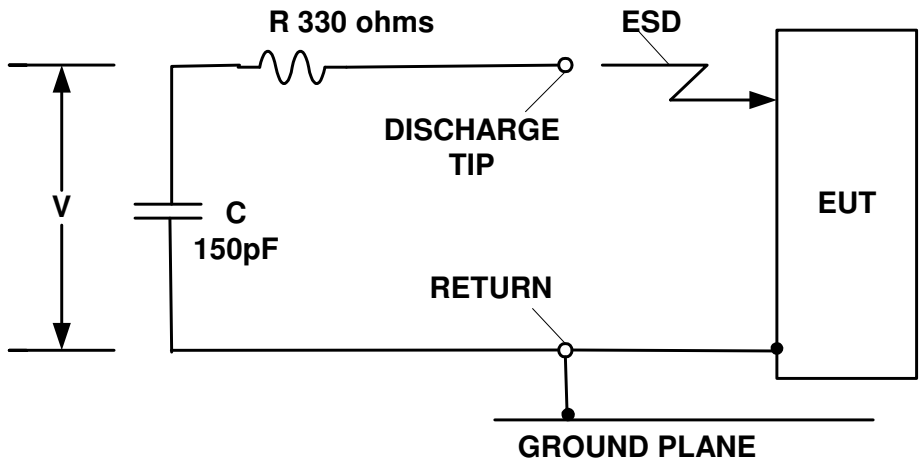
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).

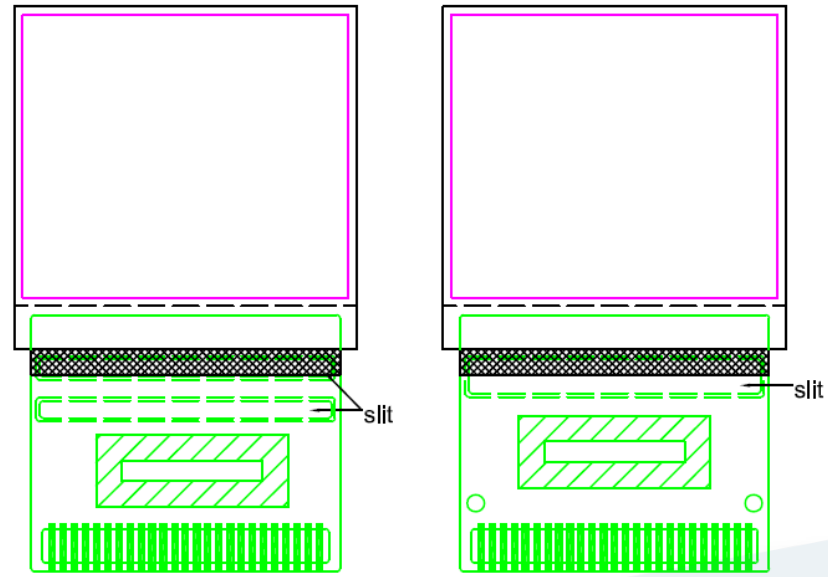
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

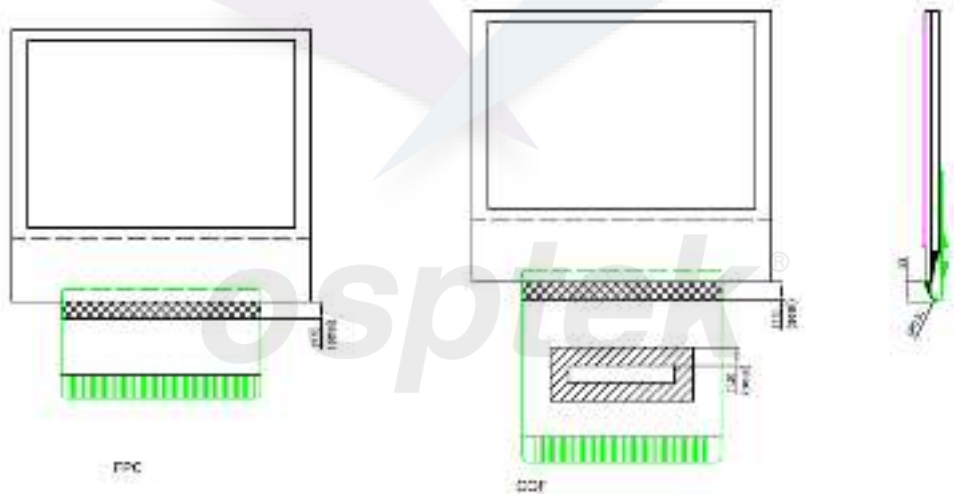
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).

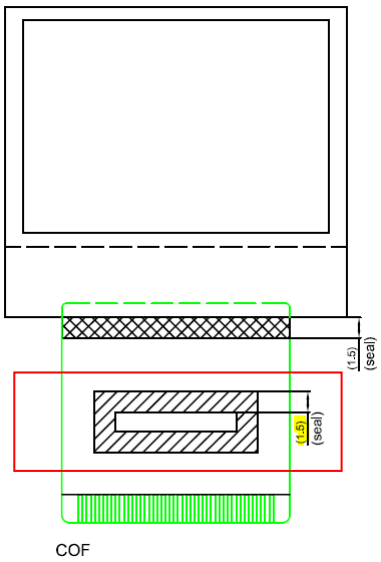


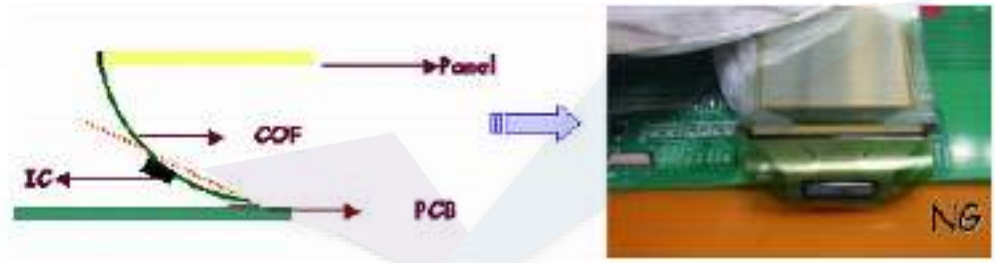
TAB TAB



FPC COF

9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.





10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.

11. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

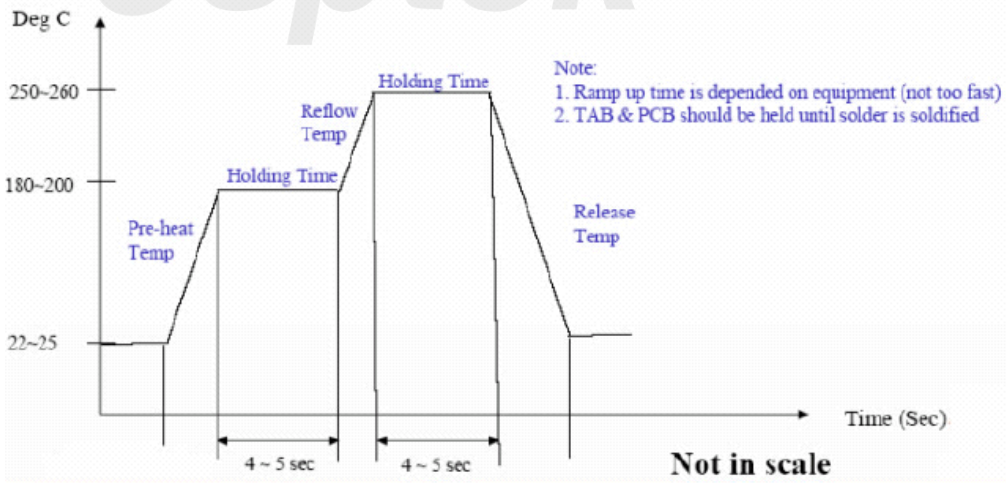
12. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

13. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

14. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

15. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

16. Suggestion for soldering process:
    i. TAB Lead- free soldering hot bar process
        1. Use pulse heated bonding tool equipment
        2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
        3. Bonding Force:--4kg per centimeter square as the starting point.
        4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.



ii. TAB Lead- free soldering wire process

In case of manual soldering (Lead- free solder wire)

1. Solder wire contact iron directly: 280±5℃ at 3-5secs
2. Solder wire contact TAB lead directly (near iron but not contact): 380±5℃, 3-5secs
3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

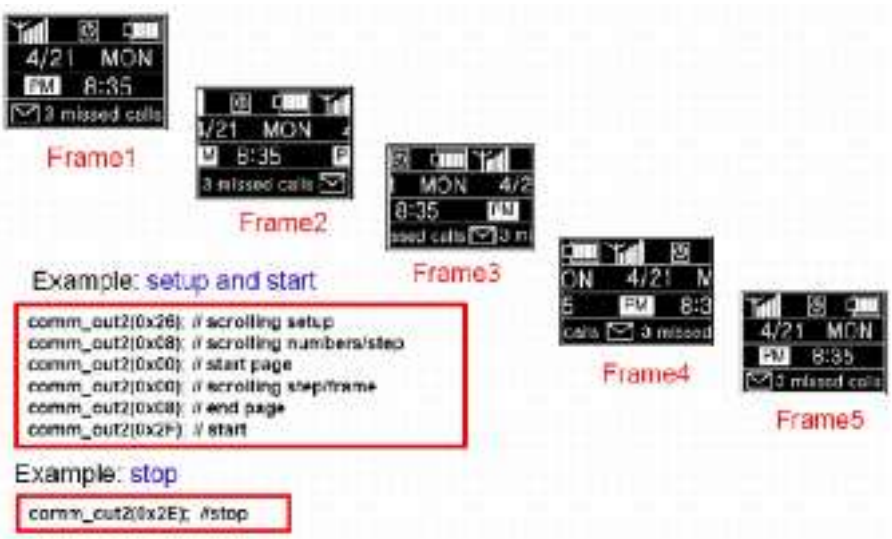
Precautions for Electrical

1. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following four strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays.
3. Avoid displaying the characters or menu with high brightness level in a fix position for a long time or repeatedly. If necessary, using the auto fadeout technology.
4. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.

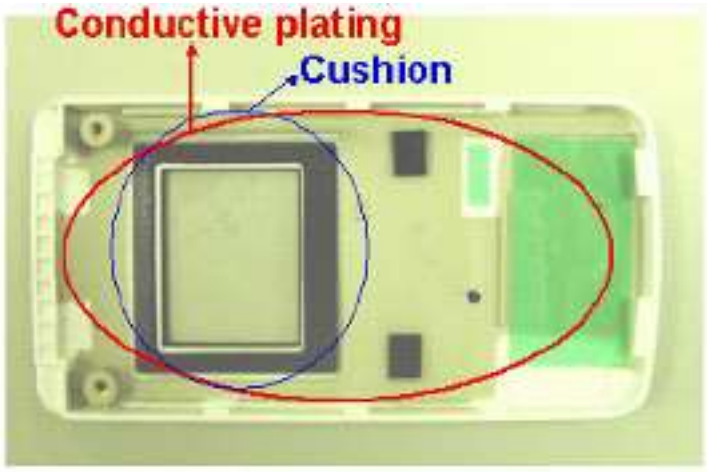
Scrolling example



Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25℃±5℃, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

Osptek only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.