

Osptek Display

OLED SPECIFICATION

Model No:

OED177-128160F003-C45

osptek[®]

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ Initial release	2010. 02. 09	
A01	■ Transfer from X version ■ Add the information of module weight ■ Add operating conditions for different luminance ■ Add the panel electrical specifications	2010. 03. 04	Page 5, 6 & 8



CONTENTS

ITEM	PAGE
<u>1. SCOPE</u>	4
<u>2. WARRANTY</u>	4
<u>3. FEATURES</u>	4
<u>4. MECHANICAL DATA</u>	5
<u>5. MAXIMUM RATINGS</u>	6
<u>6. ELECTRICAL CHARACTERISTICS</u>	7
6.1 D.C ELECTRICAL CHARACTERISTICS	
6.2 ELECTRO-OPTICAL CHARACTERISTICS	
<u>7. INTERFACE</u>	9
7.1 FUNCTION BLOCK DIAGRAM	
7.2 PANEL LAYOUT DIAGRAM	
7.3 PIN ASSIGNMENTS	
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP	
7.5 INTERFACE TIMING CHART	
<u>8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT</u>	14
8.1 POWER ON / OFF SEQUENCE	
8.2 APPLICATION CIRCUIT	
8.3 COMMAND TABLE	
<u>9. RELIABILITY TEST CONDITIONS</u>	16
<u>10. EXTERNAL DIMENSION</u>	17
<u>11. PACKING SPECIFICATION</u>	18
<u>12. APPENDIXES</u>	19

osptek®

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by Osptek. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

2. WARRANTY

Osptek warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Osptek is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored in the original packages at 25°C±5°C, 55%±10%RH or used as the conditions specified in the specifications.

Nevertheless, Osptek is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : 262 K color and 65K colors
- Panel resolution : 160*128
- Driver IC : SSD1353
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design. : 2.01 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8/9/16/18-bits 6800/8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	160 x 3x 128	dot
2	Dot Size	0.048 (W) x 0.199 (H)	mm ²
3	Dot Pitch	0.073 (W) x 0.219 (H)	mm ²
4	Aperture Rate	60	%
5	Active Area	35.015 (W) x 28.012 (H)	mm ²
6	Panel Size	42.8 (W) x 33.5 (H)	mm ²
7*	Panel Thickness	1.82 ± 0.1	mm
8	Module Size	42.8 (W) x 59.1 (H) x 2.01 (T)	mm ³
9	Diagonal A/A size	1.8	inch
10	Module Weight	5.98 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

The logo for Osptek, featuring a stylized 'X' shape composed of two overlapping triangles, one light blue and one light purple, positioned above the word 'osptek' in a lowercase, sans-serif font. A registered trademark symbol (®) is located to the upper right of the 'k'.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	3.5	V	$T_a = 25^{\circ}\text{C}$	IC maximum rating
Supply Voltage (V_{CC})	10	21	V	$T_a = 25^{\circ}\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^{\circ}\text{C}$		
Storage Temp	-40	85	$^{\circ}\text{C}$		
Humidity		85	%		
Life Time	12,000	-	Hrs	80 cd/m^2 , 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	60 cd/m^2 , 50% checkerboard	Note (2)

Note:

(A) Under $V_{CC} = 17\text{V}$, $T_a = 25^{\circ}\text{C}$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 80 cd/m^2 :

- Master contrast setting : 0x0f
- Frame rate : 85Hz
- Duty setting : 1/128

(2) Setting of 60 cd/m^2 :

- Master contrast setting : 0x0b
- Frame rate : 85Hz
- Duty setting : 1/128

osptek®

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)		16.5	17	17.5	V
V_{CI}	Low voltage power supply (for driver IC)		2.4	-	3.5	V
V_{DDIO}	Logic I/O operating voltage		1.6	-	V_{CI}	V
V_{OH}	High logic output level	$I_{out}=100\mu A$	$0.9 \cdot V_{DDIO}$		V_{DDIO}	V
V_{OL}	Low logic output level	$I_{out}=100\mu A$	0		$0.1 \cdot V_{DDIO}$	V
V_{IH}	High logic input level	$I_{out}=100\mu A$	$0.8 \cdot V_{DDIO}$		V_{DDIO}	V
V_{IL}	Low logic output level	$I_{out}=100\mu A$	0		$0.2 \cdot V_{DDIO}$	V
I_{CC}	Operating current for V_{CC} (No panel attached)	Contrast=FF		8.9	10	mA
I_{CI}	Operating current for V_{CI} (No panel attached)	Contrast=FF		890	980	μA
I_{SEG}	Segment output current (No panel attached)	Contrast=FF		160	175	μA
		Contrast=7F		80		μA

osptek[®]

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current	-	39	41	mA	All pixels on (1)
Standby mode current	-	3	5	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	663	697	mW	All pixels on (1)
Standby mode power consumption	-	51	85	mW	Standby mode 10% pixels on (2)
Pixel Luminance	60	80		cd/m ²	Display Average
Standby Luminance		20		cd/m ²	
CIE _x (White)	0.27	0.31	0.35		CIE1931
CIE _y (White)	0.29	0.33	0.37		CIE1931
CIE _x (Red)	0.62	0.66	0.70		CIE1931
CIE _y (Red)	0.29	0.33	0.37		CIE1931
CIE _x (Green)	0.26	0.30	0.34		CIE1931
CIE _y (Green)	0.59	0.63	0.67		CIE1931
CIE _x (Blue)	0.10	0.14	0.18		CIE1931
CIE _y (Blue)	0.14	0.18	0.22		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

Normal mode condition :

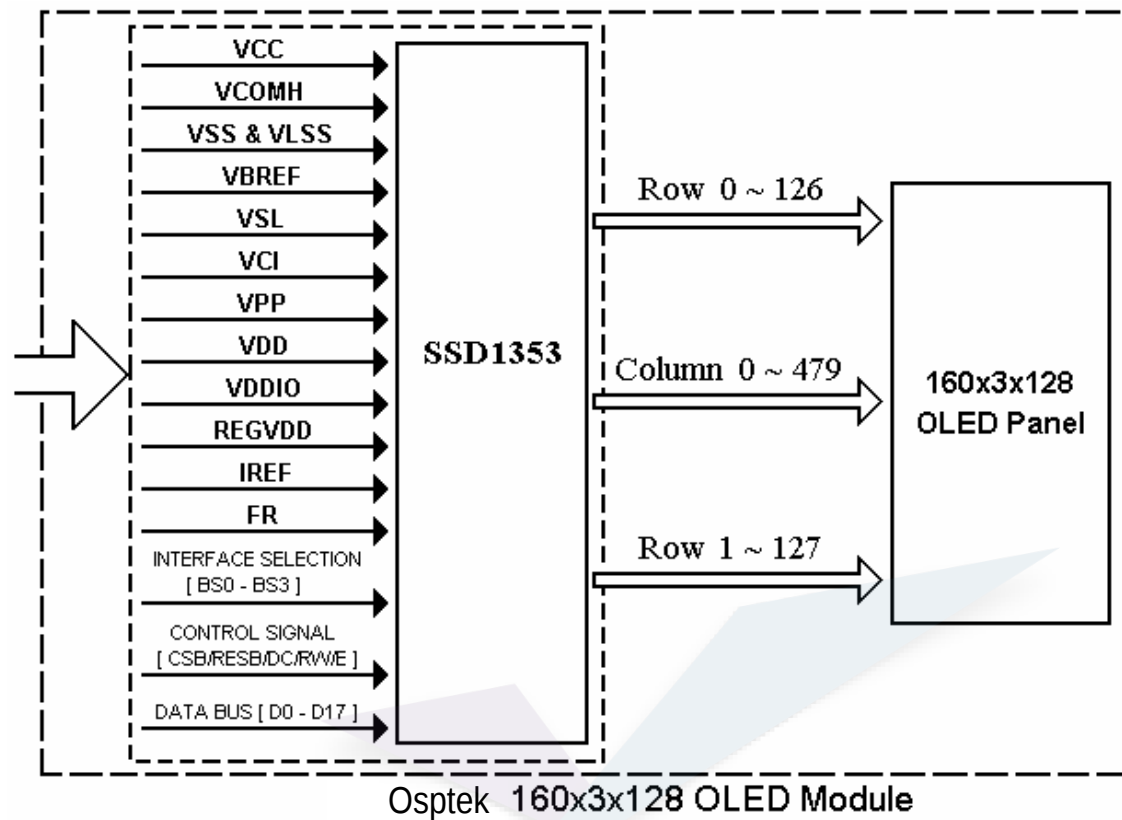
- Driving Voltage : 17V
- Contrast setting : 0x0f
- Frame rate : 85Hz
- Duty setting : 1/128

Standby mode condition :

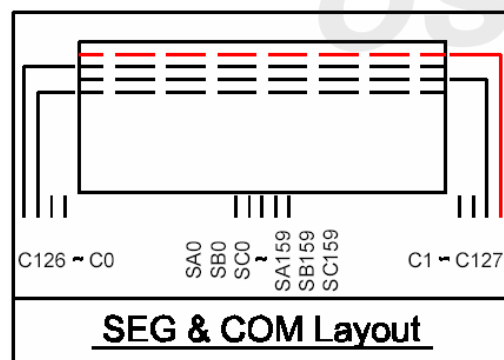
- Driving Voltage : 17V
- Contrast setting : 0x05
- Frame rate : 85Hz
- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	VCC	Power supply for panel driving voltage.
2	VCOMH	A capacitor should be connected between this pin and VSS.
3	VLSS	Analog system ground pin.
4	VSS	Ground pin.
5	VBREF	Connect to ground with a capacitor.
6	VSL	This is segment voltage reference pin.
7	VCI	Low voltage power supply.
8	VPP	Connect to VDD.
9	VDD	Power supply input for logic.
10	VDDIO	Power supply for interface logic level. It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VCI.
11.	REGVDD	Internal VDD regulator selection pin. When this pin is pulled high, internal VDD regulator is enabled. When this pin is pulled low, external VDD regulator is used.
12	BS0	Interface selection pins.
13	BS1	
14	BS2	
15	BS3	
16	FR	It should be kept NC.
17	CSB	This pad is the chip select input. Low active.
18	RESB	This is a reset signal input. Low active.
19	DC	D/C="H": Data. D/C="L": Command.
20	RW	When connected to 8080-series MPU. WR pin. When RW ="L": Write signal input. When connected to 6800-series MPU. When RW ="H": Read. When RW ="L": Write.
21	E	When connected to 8080-series MPU. RD pin. When E ="L": Read signal input. When connected to 6800-series MPU. Enable clock input of the 6800 series MPU.
22	D0	18 bit / 16bit / 9bit / 8 bit Data bus I/O.
23	D1	
24	D2	
25	D3	
26	D4	
27	D5	
28	D6	
29	D7	
30	D8	

31	D9	
32	D10	
33	D11	
34	D12	
35	D13	
36	D14	
37	D15	
38	D16	
39	D17	
40	IREF	A resistor should be connected between this pin and VSS.
41	VSS	Ground pin.
42	VLSS	Analog system ground pin.
43	VCOMH	A capacitor should be connected between this pin and VSS.
44	VCC	Power supply for panel driving voltage.
45	NC	No connection.



7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160x132x18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

Common Address \ Data Format		A5	B5	C5	A5	B5	C5	A5			C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4			C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3			C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2			C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1			C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0			C0	A0	B0	C0	
Normal	Remapped													Common output	
0	131	6	6	6	6	6	6			6	6	6	6		COM0
1	130	6	6	6											COM1
2	129														COM2
3	128														COM3
4	127														COM4
5	126														COM5
6	125			no of bits in this cell											COM6
7	124														COM7
:	:	:	:	:	:	:	:			:	:	:	:		
:	:	:	:	:	:	:	:			:	:	:	:		
:	:	:	:	:	:	:	:			:	:	:	:		
127	4														
128	3														COM128
129	2														COM129
130	1													COM130	
131	0													COM131	

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2			SC158	SA159	SB159	SA159
------------	-----	-----	-----	-----	-----	-----	-----	-------	-------	-------	-------	-------	-------

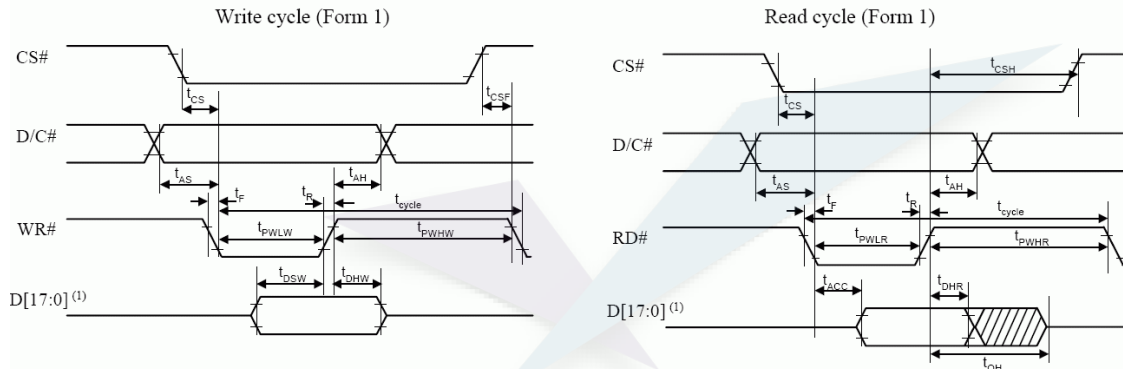
7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

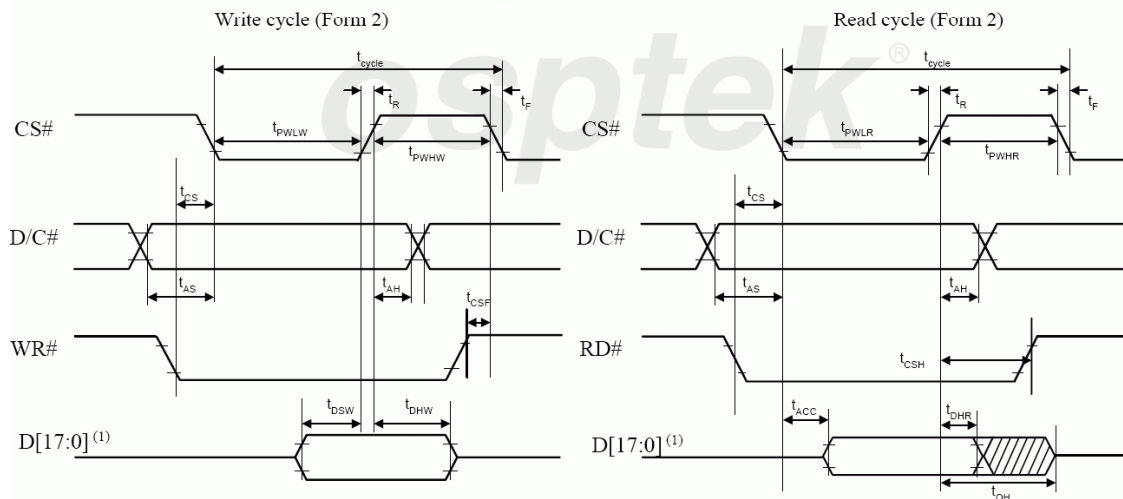
($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLr}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHr}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics (Form 1)



8080-series MCU parallel interface characteristics (Form 2)



Note

(1) when 8 bit used: D[7:0] instead; when 9 bit used: D[8:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

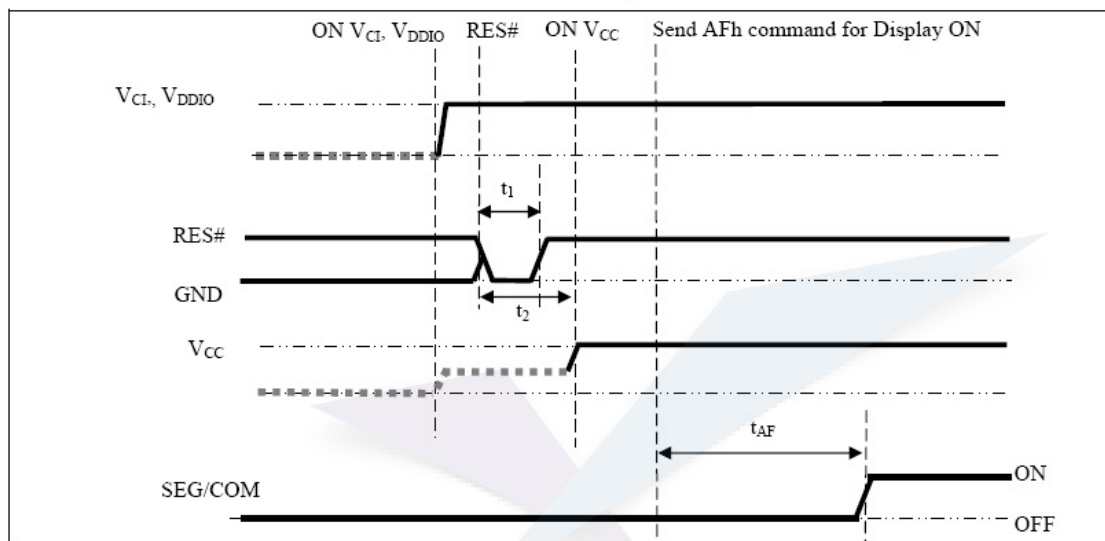
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

Power ON sequence:

1. Power ON V_{CI} , V_{DDIO} .
2. After V_{CI} , V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 100us (t_1) and then HIGH(logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON $V_{CC(1)}$
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

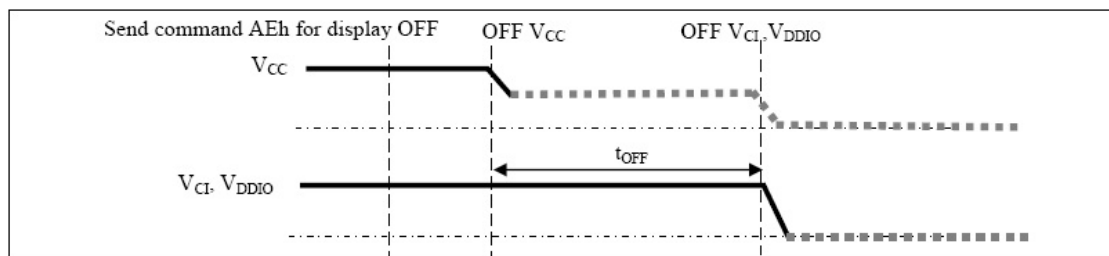
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC(1), (2)}$
3. Wait for t_{OFF} . Power OFF V_{CI} , V_{DDIO} .
(Where Minimum t_{OFF} =80ms, Typical t_{OFF} =100ms)

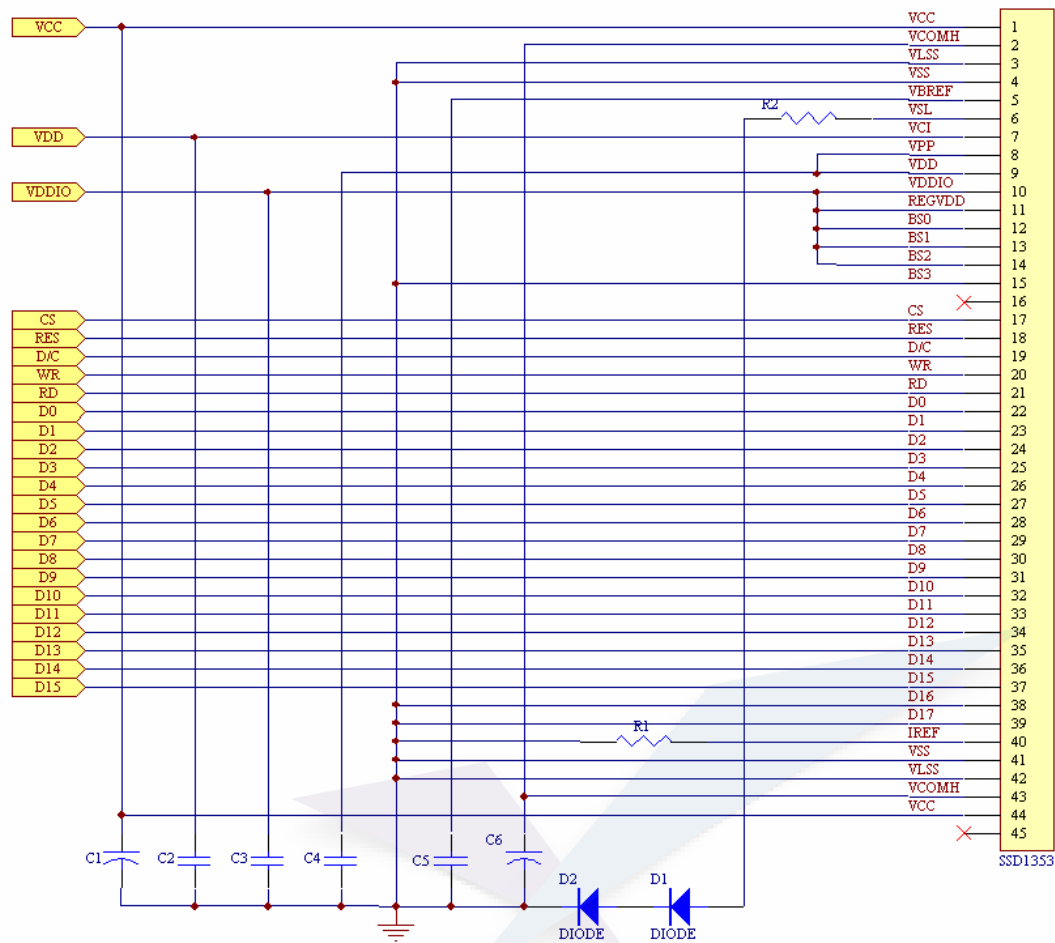
The Power OFF sequence



Note:

- (1) Since an ESD protection circuit is connected between V_{CI} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



Component:

C1, C6 : 4.7 μ F/35V (Tantalum type) or VISHAY (572D475X0025A2T)

C2, C3, C4 : 1 μ F/16V(0603)

C5 : 0.1 μ F/16V(0603)

R1: 1.2M ohm (0603) 1%

R2: 50ohm 1/4W

D1 and D2: RB480K (ROHM)

This circuit is for 8080 16bits interface.

8.3 COMMAND TABLE

Refer to IC Spec : SSD1353

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

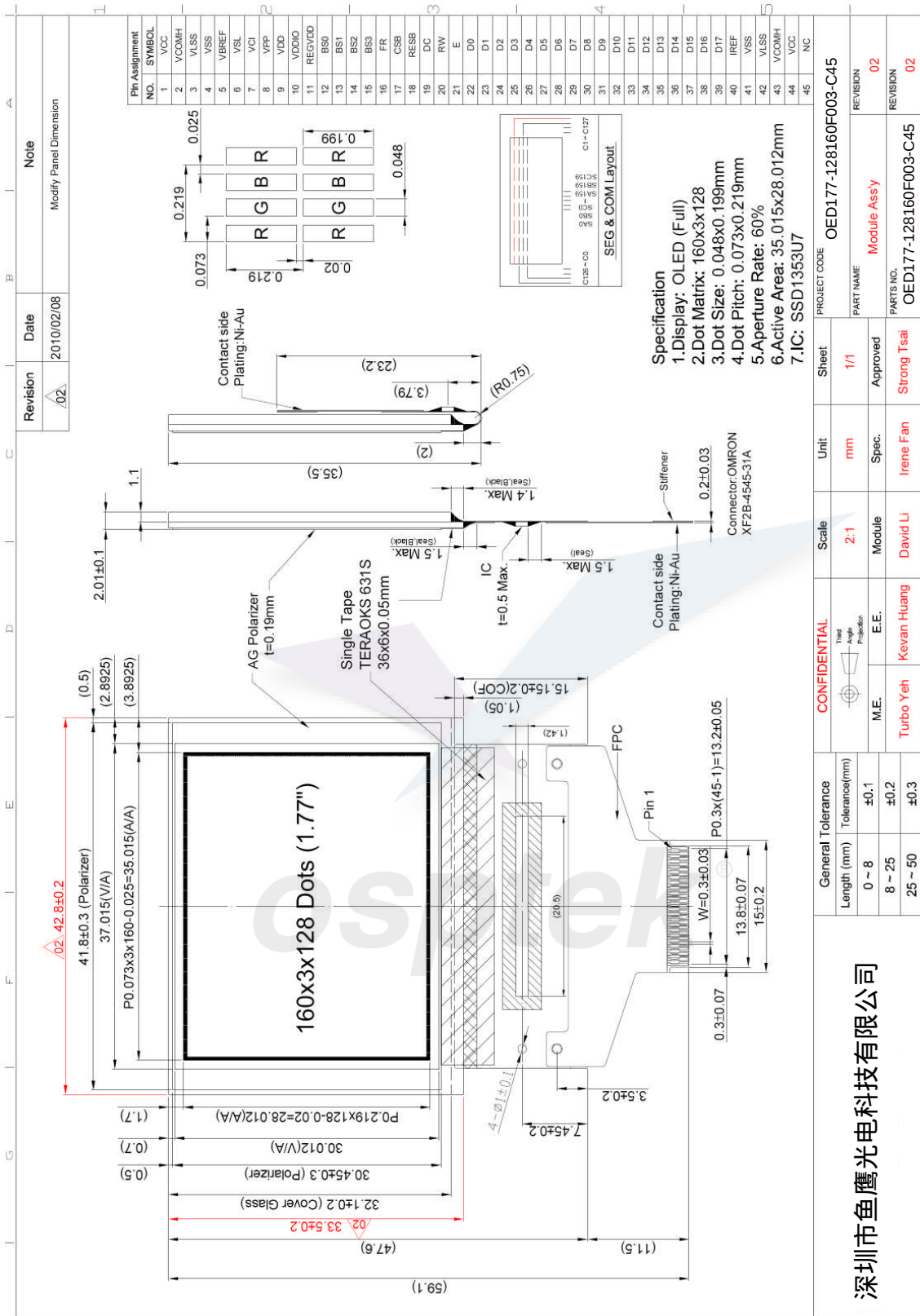
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

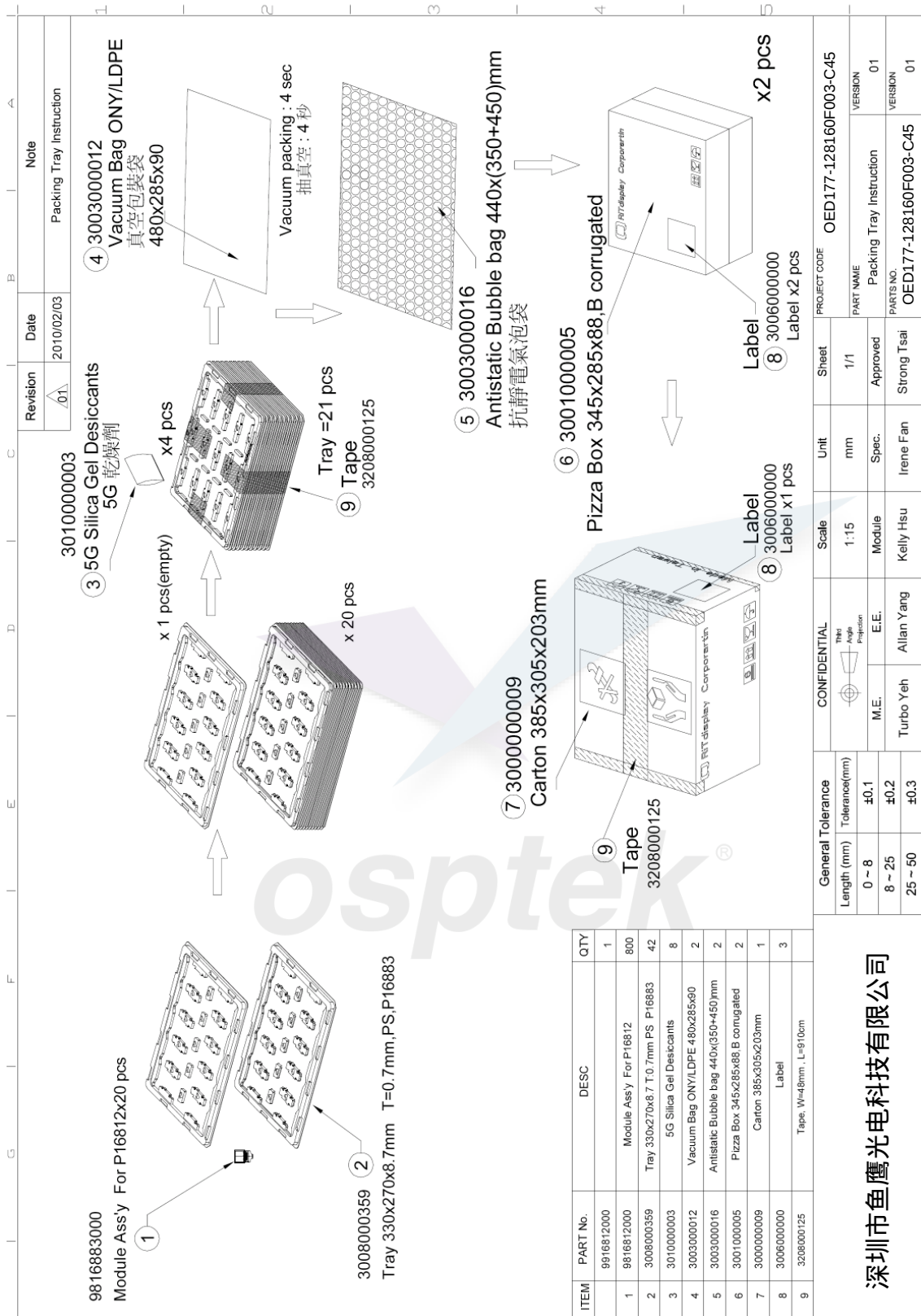
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm 50\%$ of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDICES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

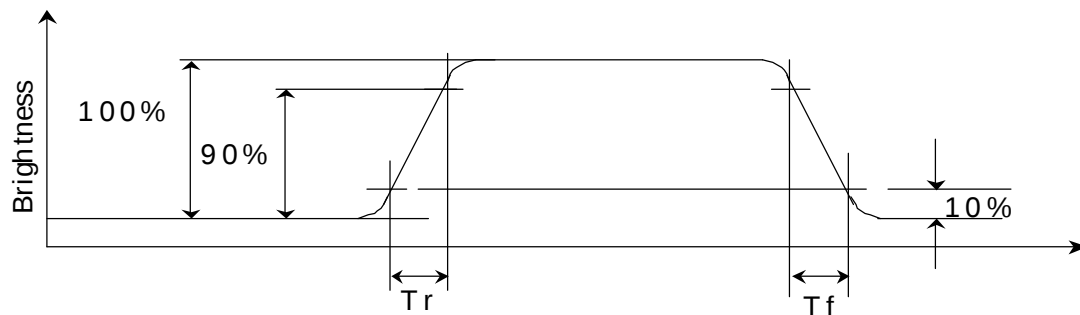


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

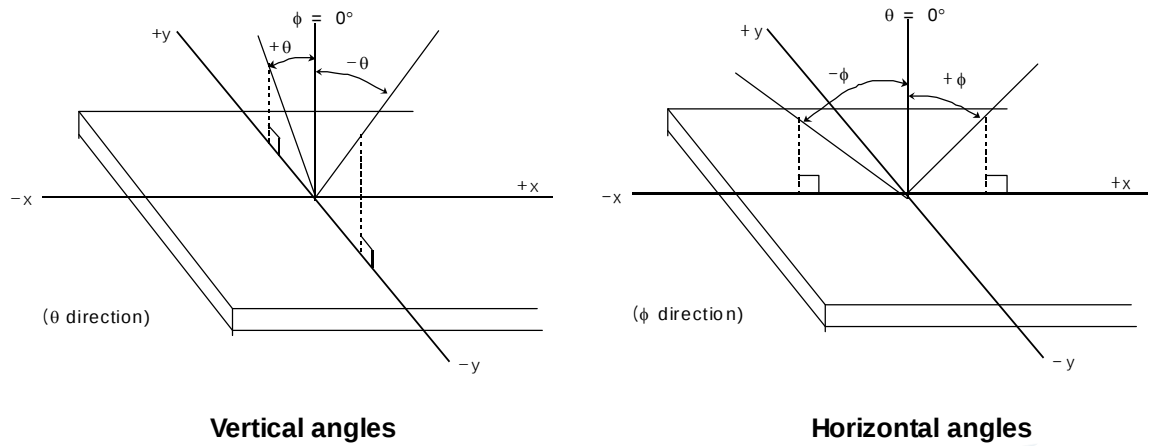


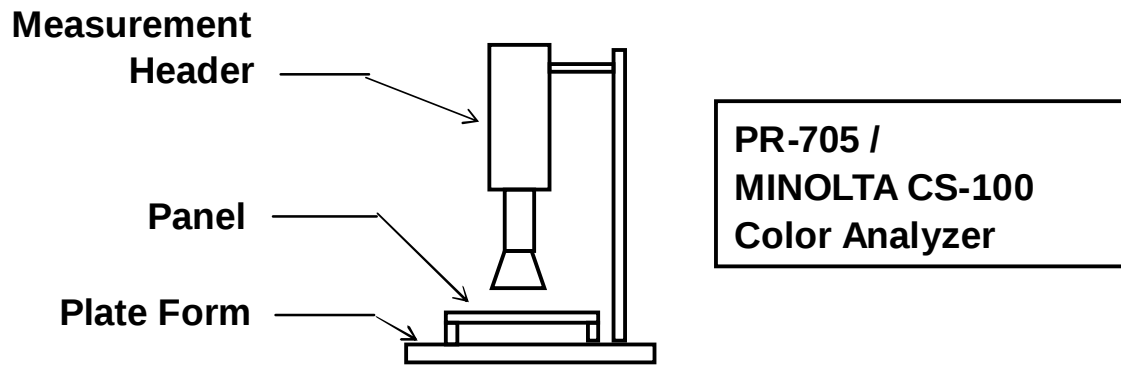
Figure 3 Viewing angle

osptek®

APPENDIX 2: MEASUREMENT APPARATUS

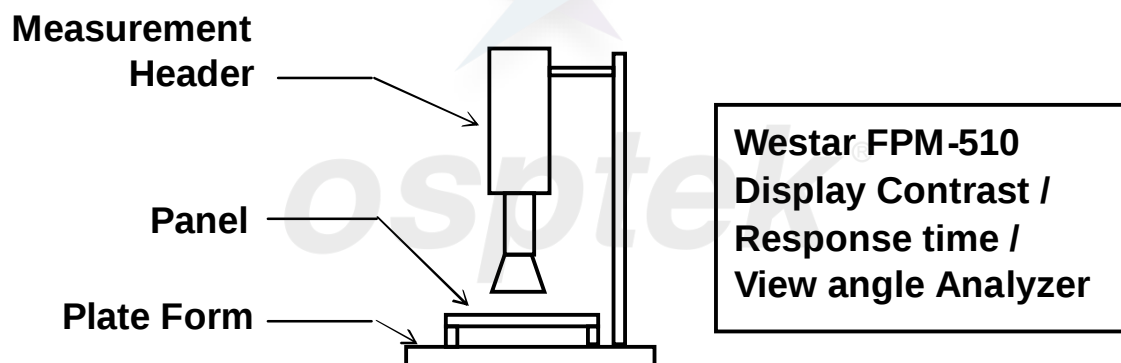
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

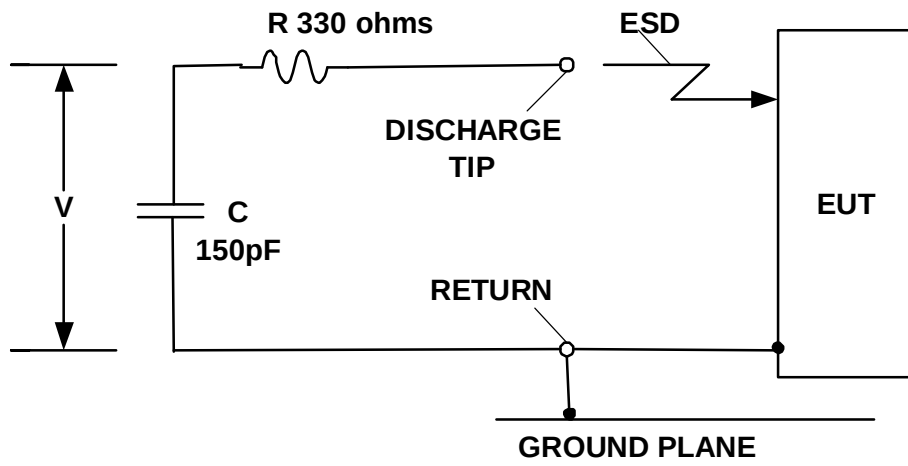


B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



osptek[®]

APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

