Osptek Display

OLED SPECIFICATION

Model No:

OED096-12864YB101-H30

CONTENTS

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RECORDS OF REVISION

DATE	REVISED NO.	REVISED DESCRIPTIONS	PREPARED	CHECKED	APPROVED
09.06.2017	VER1.0	FIRST ISSUE			

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3. GENERAL SPECIFICATIONS：

3-1 SCOPE:

This specification covers the delivery requirements for the organic light emitting diode display delivered by quality to Customer.

3-2 PRODUCTS:

Organic light emitting diode (OLED)

3-3 MODULE NAME:

OED096-12864YB101-H30

4. FEATURES：

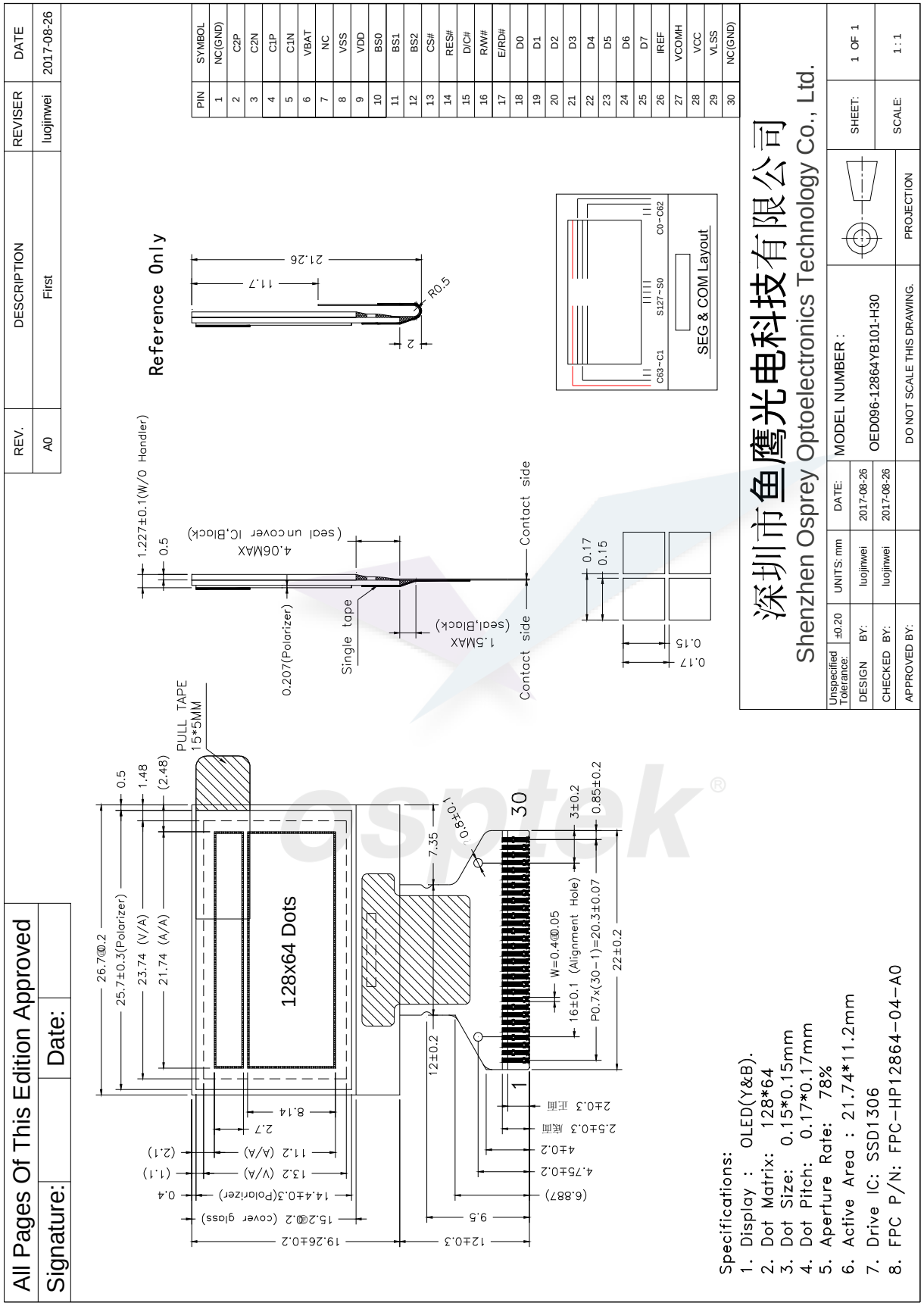
(1) Display Color: Y&B
(2) Dot Matrix: 128x64
(3) Drive IC: SSD1306BZ
(4) Viewing Angle: 160°
(5) Aperture rate: 78%
(6) Interface: 6800/8080 interface, 4 wire serial interface, I^2C

5. MACHANICAL SPECIFICATIONS：

ITEM	SPECIFICATIONS UNIT	
MODULE SIZE	26.7(W)x19.26(H)x1.227(D)	mm
VIEWING AREA	23.74 (W) x 13.2(H)	mm
ACTIVE AREA	21.74(W) x11.2 (H)	mm
DOT SIZE	0.15(W) x0.15(H)	mm
DOT PITCH	0.17(W) x0.17 (H)	mm
ASSY.TYPE	COG	---
WEIGHT	TBD	

NOTES:

OLED should be grounded during handling OLED.


REV. DESCRIPTION REVISER DATE
A0 First luojinwei 2017-08-26
PIN SYMBOL
1 NC(GND)
2 C2P
3 C2N
4 C1P
5 C1N
6 VBAT
7 NC
8 VSS
9 VDD
10 BS0
11 BS1
12 BS2
13 CS#
14 RES#
15 D/C#
16 R/W#
17 E/RD#
18 D0
19 D1
20 D2
21 D3
22 D4
23 D5
24 D6
25 D7
26 IREF
27 VCOMH
28 VCC
29 VLSS
30 NC(GND)
Reference Only
SEG & COM Layout
C63~C1
S127~S0
C0~C62
深圳市鱼鹰光电科技有限公司
Shenzhen Osprey Optoelectronics Technology Co., Ltd.
Unspecified Tolerance: ±0.20
UNITS: mm
DATE:
MODEL NUMBER :
OED096-12864YB101-H30
DESIGN BY: luojinwei 2017-08-26
CHECKED BY: luojinwei 2017-08-26
APPROVED BY:
DO NOT SCALE THIS DRAWING.
PROJECTION
SHEET: 1 OF 1
SCALE: 1 : 1
All Pages Of This Edition Approved
Signature: Date:
128x64 Dots
PULL TAPE 15*5MM
Contact side
Single tape
0.207(Polarizer)
1.227±0.1(W/O Handler)
4.06MAX (seal uncover IC,Black)
1.5MAX (seal,Black)
Specifications:
1. Display : OLED(Y&B).
2. Dot Matrix: 128*64
3. Dot Size: 0.15*0.15mm
4. Dot Pitch: 0.17*0.17mm
5. Aperture Rate: 78%
6. Active Area : 21.74*11.2mm
7. Drive IC: SSD1306
8. FPC P/N: FPC-HP12864-04-A0

7. INERFACE SPECIFICATIONS

7-1. PIN ASSIGNMENT

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>TYPE</th><th>FUNCTION DESCRIPTIONS</th></tr>
<tr><td>1</td><td>NC(GND)</td><td>P</td><td>It should be connected to external ground.</td></tr>
<tr><td>2</td><td>C2P</td><td rowspan="4">I</td><td rowspan="4">C1P/C1N-Pin for charge pump capacitor.
C2P/C2N-Pin for charge pump capacitor.
Connect to each other with a capacitor. They must be floated when the Charge pump not use.</td></tr>
<tr><td>3</td><td>C2N</td></tr>
<tr><td>4</td><td>C1P</td></tr>
<tr><td>5</td><td>C1N</td></tr>
<tr><td>6</td><td>VBAT</td><td>P</td><td>Power supply for charge pump regulator circuit.
It must be connected to external source when charge pump is used.
It must be float when charge pump is not used.</td></tr>
<tr><td>7</td><td>NC</td><td></td><td>NC</td></tr>
<tr><td>8</td><td>VSS</td><td>P</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>9</td><td>VDD</td><td>P</td><td>Power pin for logic circuit. It must be connected to external source.</td></tr>
<tr><td>10</td><td>BS0</td><td rowspan="3">I</td><td rowspan="3">Interface selection pins.
<table>
<tr><th></th><th>I²C</th><th>6800</th><th>8080</th><th>4SPI</th></tr>
<tr><td>BS0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>11</td><td>BS1</td></tr>
<tr><td>12</td><td>BS2</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>Chip Select input pin. Active “L”</td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>Hardware reset input pin. Active “L”.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>This is Data/Command control pin.
When the pin is pulled HIGH, the data at D[7:0] is data.
When the pin is pulled LOW, the data at D[7:0] is command.
In I2C mode, this pin acts as SA0 for slave address section.
When 3-wire serial interface is selected, this pin must be connected to VSS</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>This is read/write control input pin.
8080: data write enable; 6800: read/write select pin.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>17</td><td>E#</td><td>I</td><td>This is read/write control input pin.
8080: data read enable; 6800: read/write enable pin.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>18</td><td>D0</td><td rowspan="8">I/O</td><td rowspan="8">These are 8-bit bi-directional data bus to be connected to microprocessor’s Data bus.
When serial interface mode is selected, D2 should be kept NC, D1 will be the serial data input: SDIN, D0 will be the serial clock input: SCLK.
When I2C mode is selected, D2, D1 should be tied together and serve as SDA and D0 is the serial clock input, SCL.</td></tr>
<tr><td>19</td><td>D1</td></tr>
<tr><td>20</td><td>D2</td></tr>
<tr><td>21</td><td>D3</td></tr>
<tr><td>22</td><td>D4</td></tr>
<tr><td>23</td><td>D5</td></tr>
<tr><td>24</td><td>D6</td></tr>
<tr><td>25</td><td>D7</td></tr>
</table>

26	IREF	I	Current reference for brightness adjustment. This is segment output current reference pin. A resistor should be connected between this pin and VSS .Set the current at 12.5 uA maximum.
27	VCOMH	O	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
28	VCC	P	Power supply for OLED driving voltage. A capacitor should be connected between this pin and VSS, when charge pump is used. It must be connected to external source when charge pump is not used.
29	VLSS	P	This is an analog ground pin. It should be connected to VSS externally.
30	NC(GND)	P	It should be connected to external ground.

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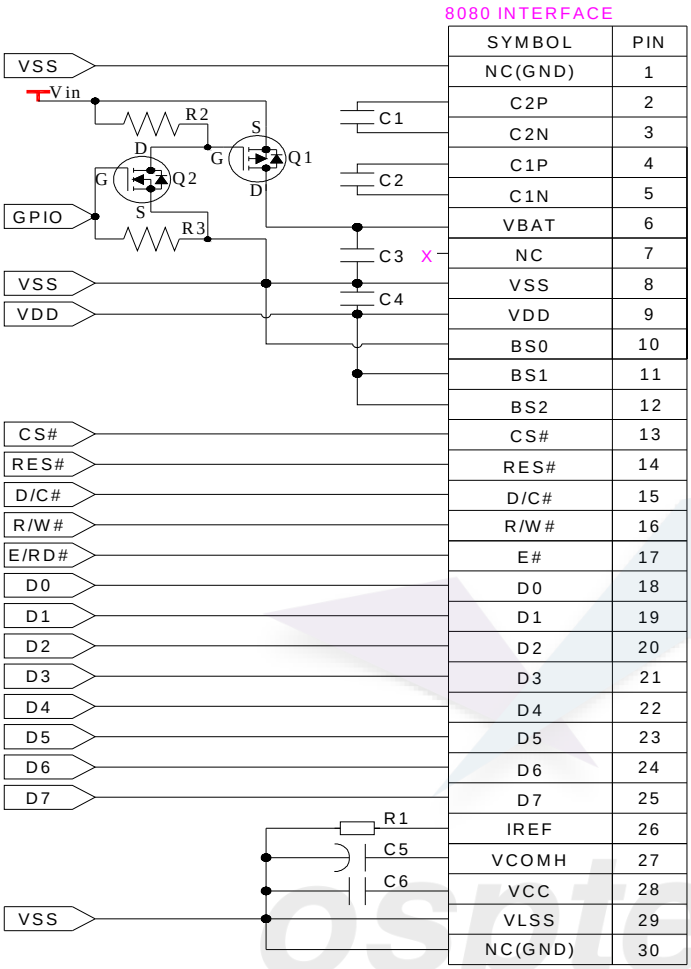
7-2 APPLICATION CIRCUIT

7-2-1 8080 Interface With Internal Charge Pump

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2: 1μF / 16V, X5R

C3, C4: 1μF / 16V, X5R

C5: 4.7μF / 25V(Tantalum type)

C6: 2.2μF / 25V,X7R

R1: 620kΩ, R1 = (Voltage at IREF - VSS) / IREF

R2, R3: 47kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

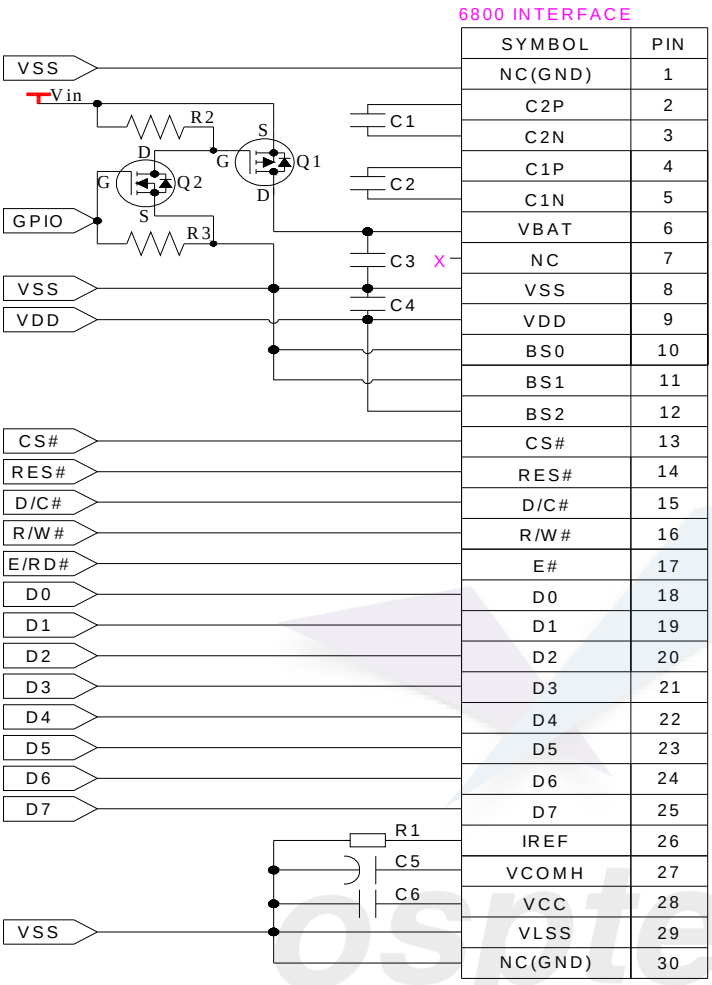
Vin: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (9V), R1 should be replaced as 620 **kΩ**.

7-2-2 6800 Interface With Internal Charge Pump

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2: 1μF / 16V, X5R

C3, C4: 1μF / 16V, X5R

C5: 4.7μF / 25V(Tantalum type)

C6: 2.2μF / 25V,X7R

R1: 620kΩ, R1 = (Voltage at IREF - VSS) / IREF

R2, R3: 47kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

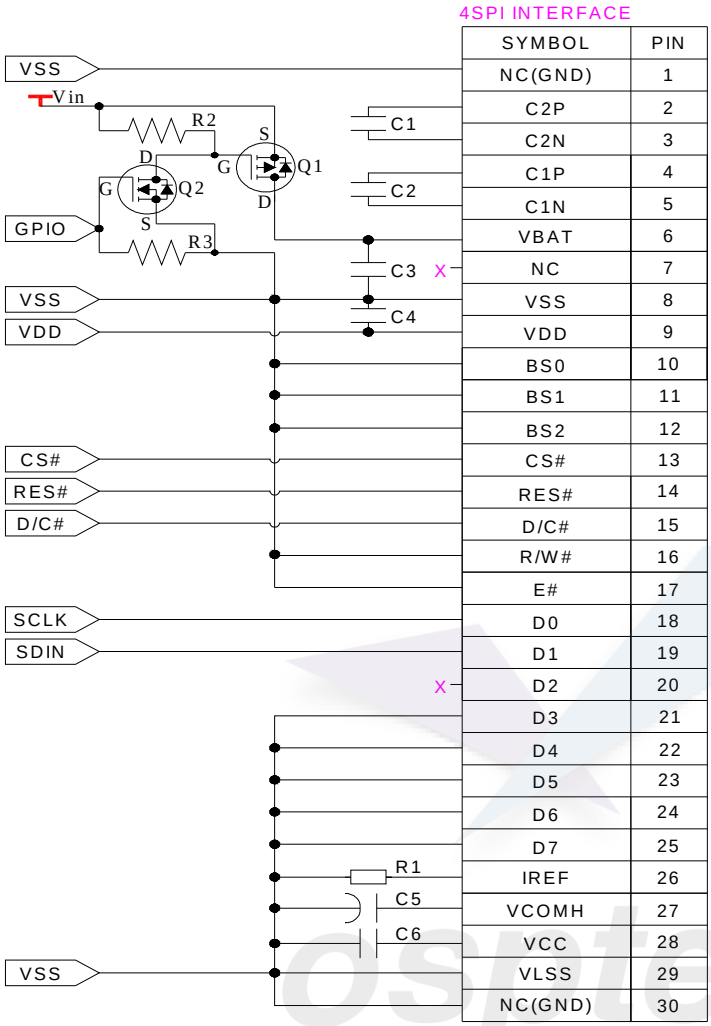
Vin: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (9V), R1 should be replaced as 620 **kΩ**.

7-2-3 4-Wire Serial Interface With Internal Charge Pump

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2: 1μF / 16V, X5R

C3, C4: 1μF / 16V, X5R

C5: 4.7μF / 25V(Tantalum type)

C6: 2.2μF / 25V,X7R

R1: 620kΩ, R1 = (Voltage at IREF - VSS) / IREF

R2, R3: 47kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

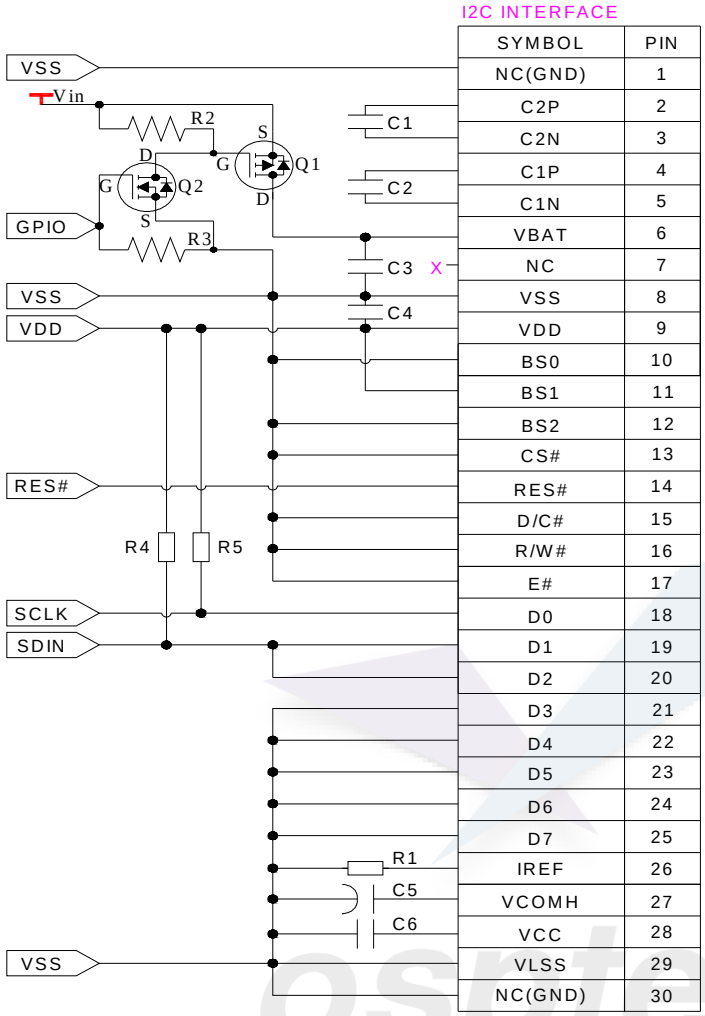
Vin: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (9V), R1 should be replaced as 620 **kΩ**.

7-2-4 I²C Interface With Internal Charge Pump

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2: 1μF / 16V, X5R

C3, C4: 1μF / 16V, X5R

C5: 4.7μF / 25V(Tantalum type)

C6: 2.2μF / 25V,X7R

R1: 620kΩ, R1 = (Voltage at IREF - VSS) / IREF

R2, R3: 47kΩ

R4, R5: 4.7kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

Vin: 3.5~4.2V

The I²C slave address is 0111100b

* VBAT will be connected to VDD when VCC be connected to external source (9V), R1 should be replaced as 620 **kΩ**.

8. ABSOLUTE MAXIMUM RATING

Characteristic	Symbol	Standard Value			Unit	Notes
		MIN	TYP	MAX		
Power Supply Voltage(1)	V_{DD}	-0.3	-	+4.0	V	1,2
Power Supply Voltage(2)	V_{BAT}	-0.3	-	4.5	V	1,2
Power Supply Voltage(3)	V_{CC}	0	-	15.0	V	1,2
Operating Temperature	T_{OPR}	-40	-	+70	^{0}C	
Storage Temperature	T_{STG}	-40	-	+85	^{0}C	3
Life Time (120 cd/m^2)		10000	-	-	hour	4
Life Time (80 cd/m^2)		30000	-	-	hour	4
Life Time (60 cd/m^2)		50000	-	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 9-1 "DC ELECTRICAL CHARACTERISTICS". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 9.0V, T_a = 25°C, 50% Checkerboard.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

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9.ELECTRICAL CHARACTERISTICS

9-1 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test condition	Standard Value			Unit
			MIN	TYP	MAX	
V_{DD}	Logic Supply Voltage	-	1.65	2.8	3.3	V
V_{BAT}	Charge Pump Regulator Supply Voltage	Internal Charge Pump Enable	3.5	-	4.2	V
V_{CC}	Operating Voltage for OLED (Generated by charge pump)	Internal Charge Pump Enable	7.0	7.5		V
V_{CC}	Operating Voltage for OLED (Supplied Externally)	Internal Charge Pump Disable	8.5	9.0	9.5	V
V_{IH}	High Logic Input Level		0.8*V_{DD}	-	-	V
V_{IL}	Low Logic Input Level		-	-	0.2*V_{DD}	V
V_{OH}	High Logic Output Level	I_{OUT} = 100μA, 3.3MHz	0.9*V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100μA, 3.3MHz	-	-	0.1*V_{DD}	V
$I_{DD, SLEEP}$	I_{DD}, Sleep Mode Current		-	-	10	uA
$I_{BAT, SLEEP}$	I_{BAT}, Sleep Mode Current		-	-	10	uA
$I_{CC, SLEEP}$	I_{CC}, Sleep Mode Current		-	-	10	uA
I_{DD}	V_{DD} Supply Current		-	50	150	uA
I_{CC}	V_{CC} Supply Current (V_{CC} Supplied Externally)	V_{DD} = 2.8V, V_{CC} = 9V, 100% Display Area Turn on	-	9.0	15.0	mA
I_{BAT}	I_{BAT} Supply Current (V_{CC} Generated by charge pump)	V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on	-	25.6	32.0	mA

9-2 ELECTRO-OPTICAL CHARACTERISTICS

Symbol	Parameter	condition	Standard Value			Unit
			MIN	TYP	MAX	
L_{br}	Brightness (V_{CC} Supplied Externally)		120	-	-	cd/m^2
L_{br}	Brightness (V_{CC} Generated by charge pump)		80	120	-	cd/m^2
(x)	C.I.E. (White)	C.I.E. 1931	0.25	0.29	0.33	
(y)			0.27	0.31	0.35	
CR	Dark Room Contrast		-	2000:1	-	
	Viewing Angle		-	160	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 9V & *7.25V*.

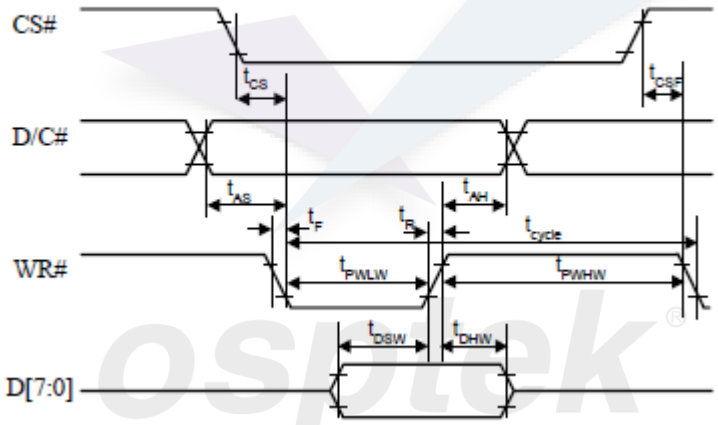
9-3 AC ELECTRICAL CHARACTERISTICS

9-3-1 8080 Interface Timing Characteristics

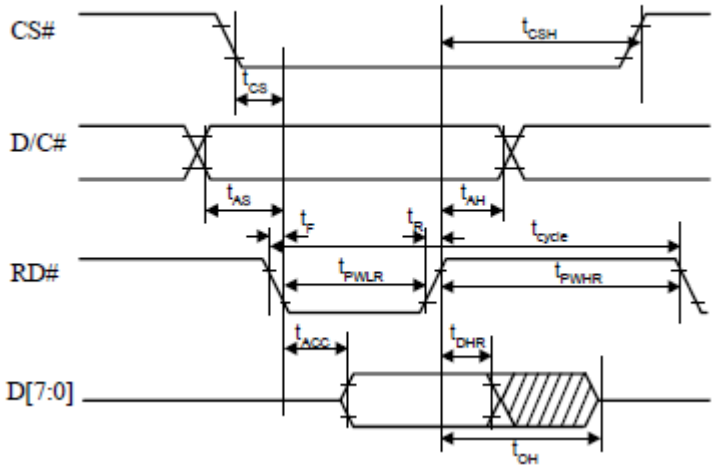
(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Write Cycle



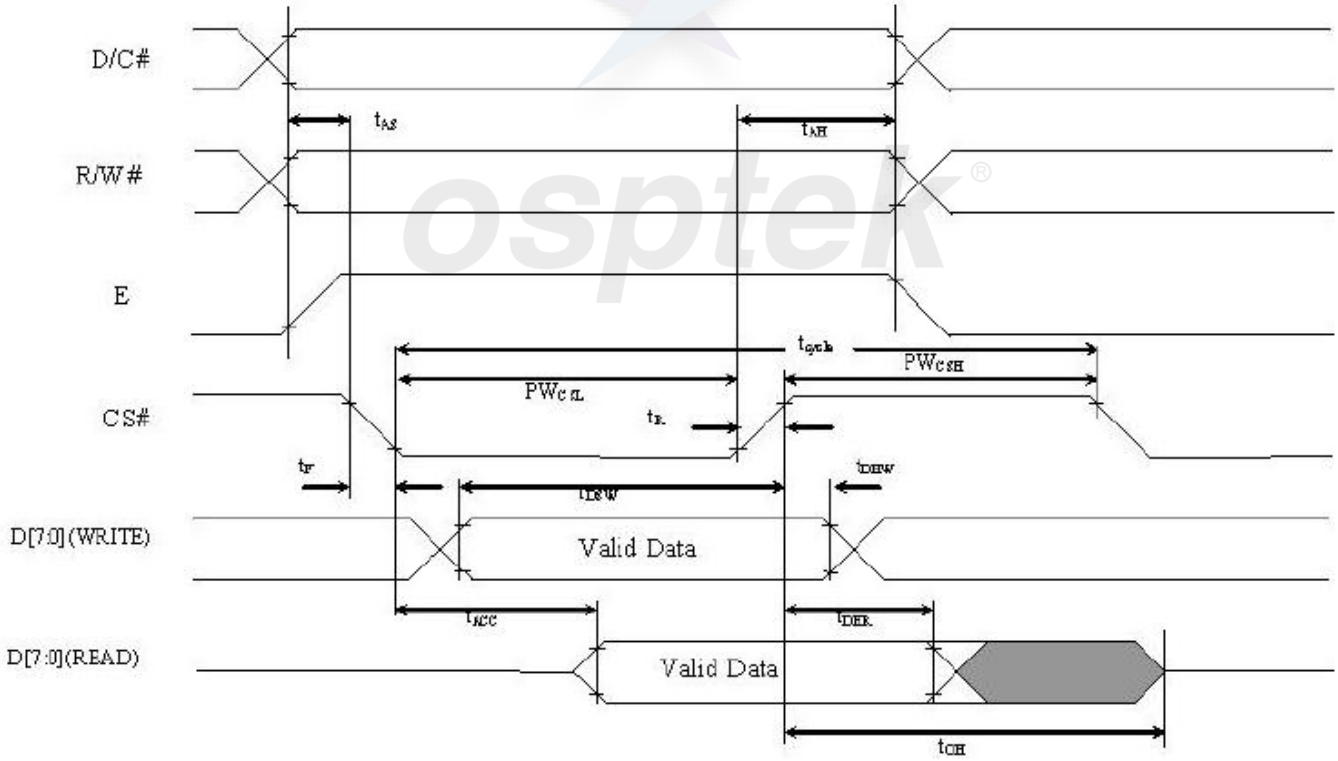
Read cycle



9-3-2 6800 Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



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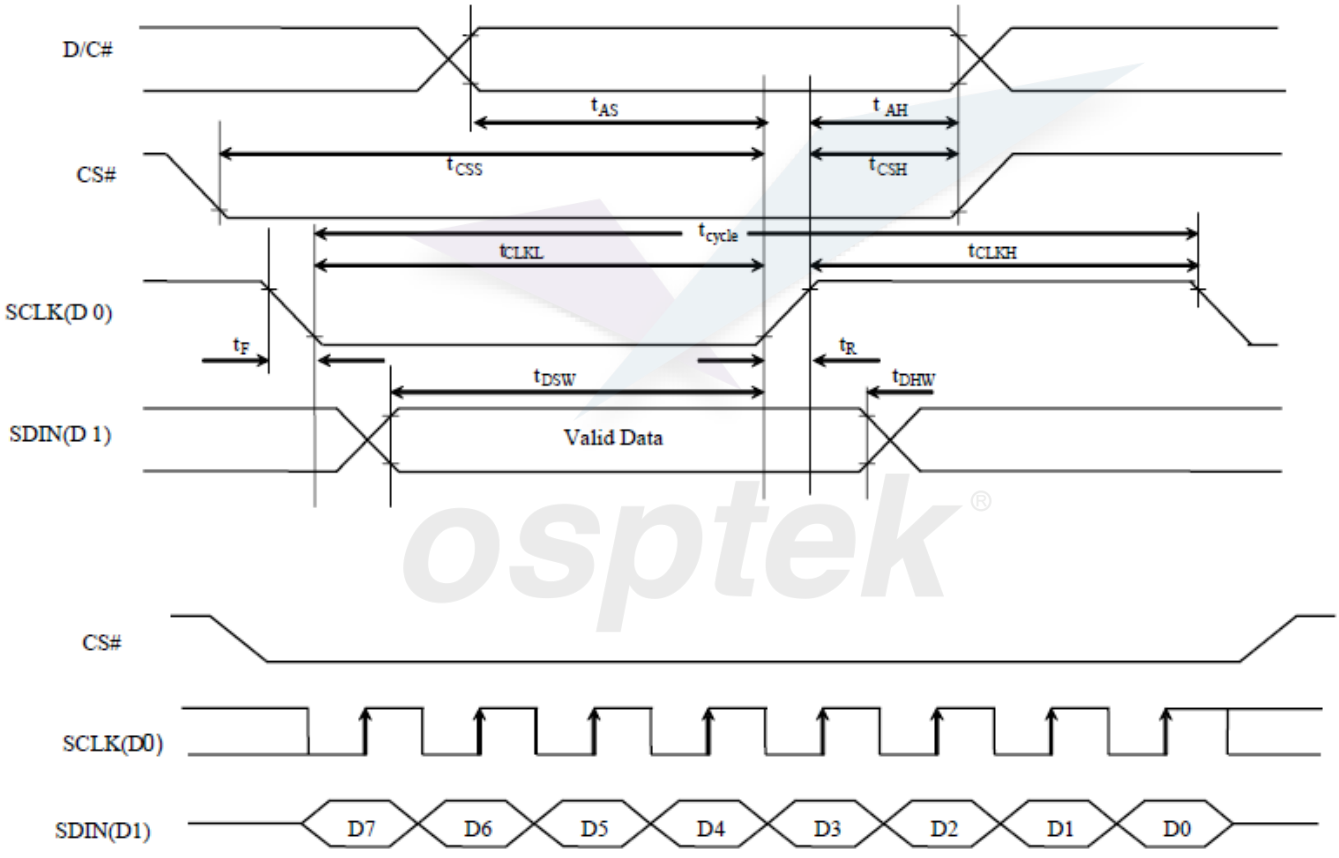
9-3-3 4-Wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



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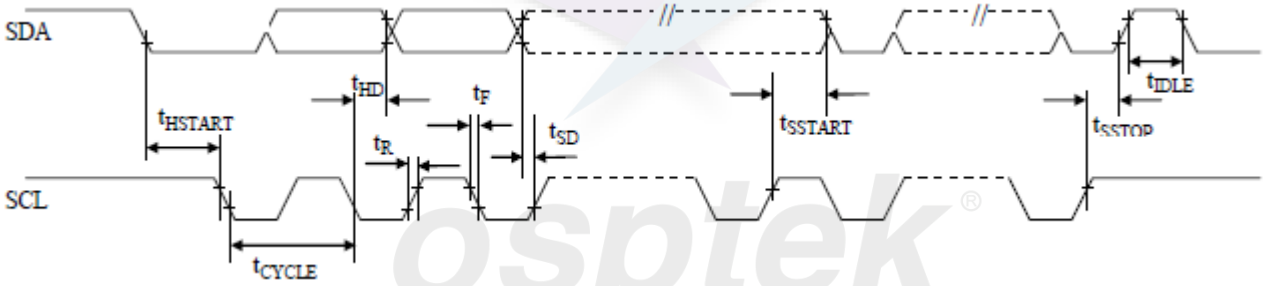
9-3-4 I^2C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



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10. FUNCTIONNAL SPECIFICATIONS

10-1 COMMANDS

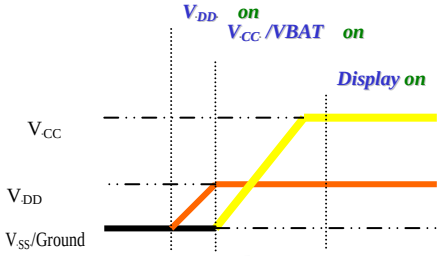
Refer to the SSD1306 IC Spec.

10-2 POWER UP AND POWER DOWN SEQUENCE

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

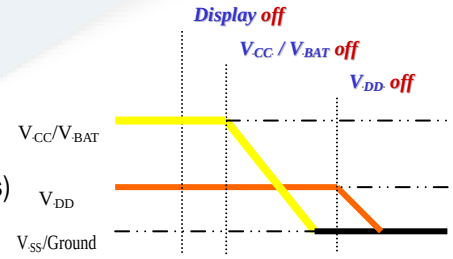
10-2-1 Power up Sequence:

1. Power up V_{DD} / V_{BAT}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



10-2-2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{BAT}
3. Delay 100ms
   (When V_{CC} / V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{BAT} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{BAT}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{BAT} power down.

10-3 Reset Circuit

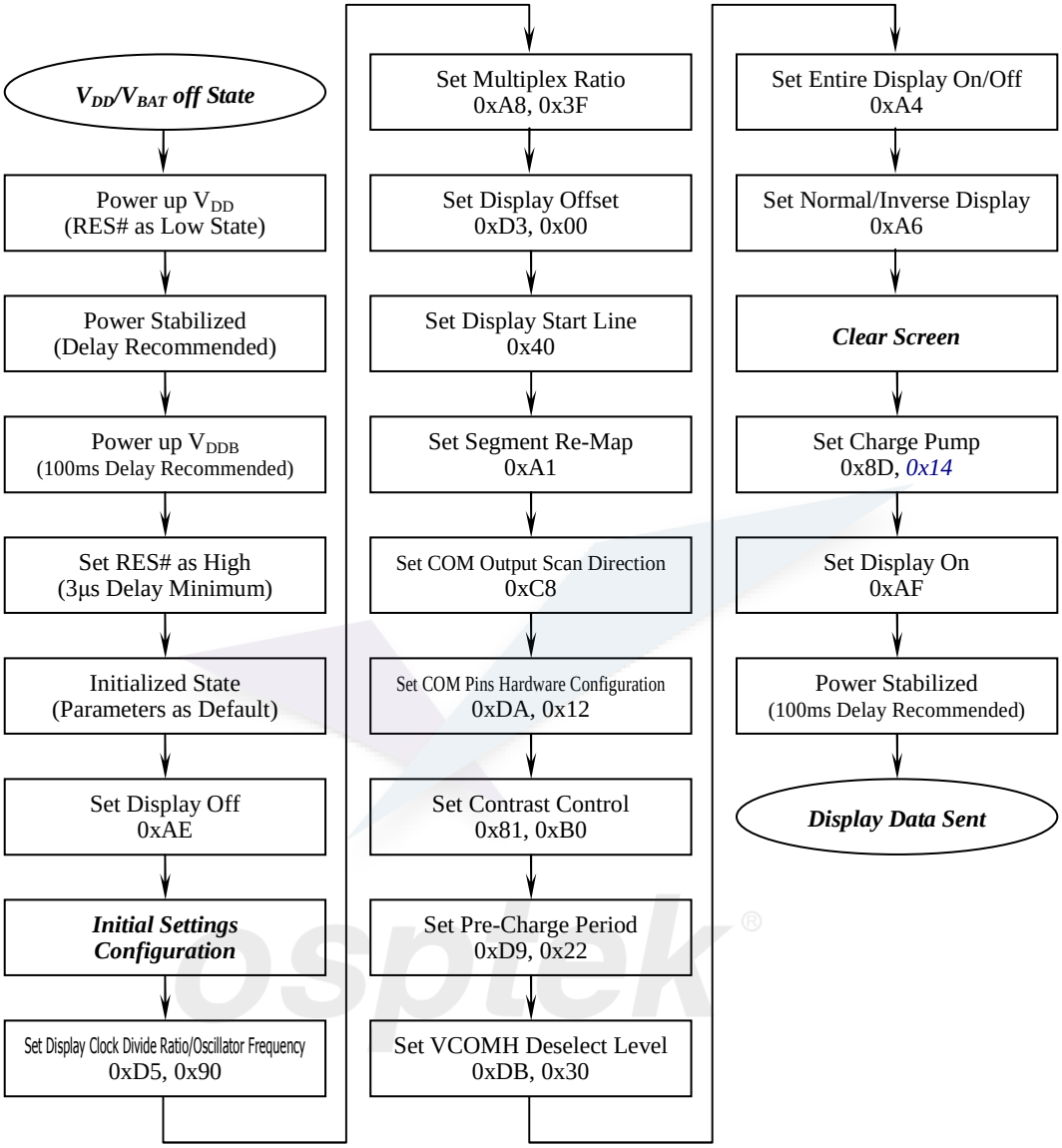
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

10-4 Actual Application Example

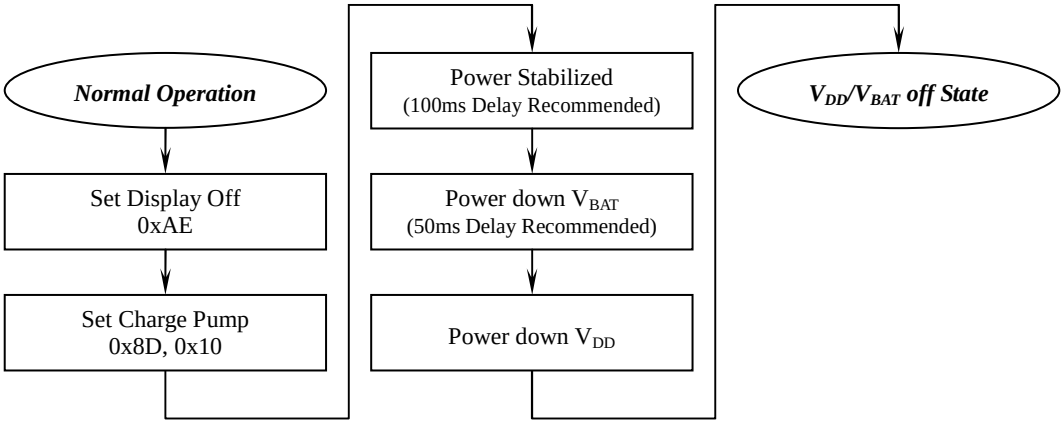
Command usage and explanation of an actual example . VCC generated by charge pump.

<Power up Sequence>

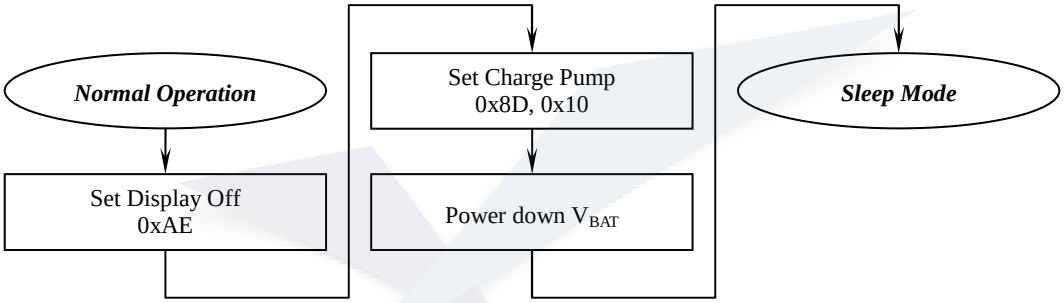


*If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

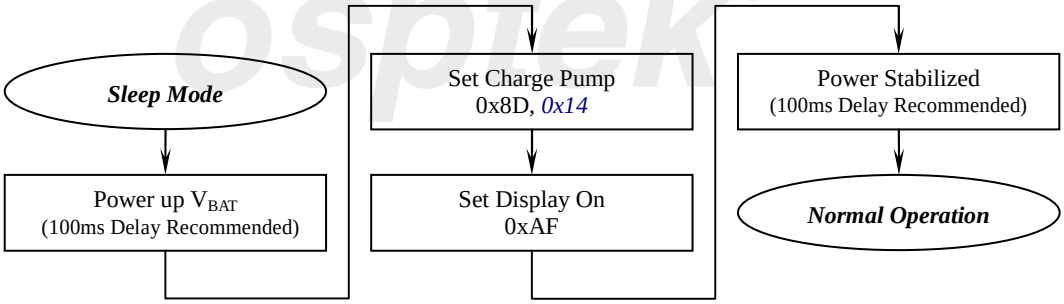
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



```
void Init_Lcd(void)
{
    RST=1;
    Delay_1ms(100);
    RST=0;
    Delay_1ms(100);
    RST=1;
    Delay_1ms(100);

    Write_Command(0xAE);//set display display ON/OFF,AFH/AEH

    Write_Command(0x40);//set display start line:COM0

    Write_Command(0x81);//set contrast control
    Write_Command(0xCF);

    Write_Command(0x20);//set memory addressing mode
    Write_Command(0x02);//page addressing mode

    Write_Command(0xA0);//set segment re-map

    Write_Command(0xA4);//entire display on: A4H:OFF/A5H:ON

    Write_Command(0xA6);//set normal/inverse display: A6H:normal/A7H:inverse

    Write_Command(0xA8);//set multiplex ratio
    Write_Command(0x3F);//1/64duty

    Write_Command(0xC0);//set com output scan direction

    Write_Command(0xD3);//set display    offset
    Write_Command(0x00);//

    Write_Command(0xD5);//set display    clock divide ratio/oscillator frequency
    Write_Command(0x80);//105Hz

    Write_Command(0xD9);//set pre-charge period
    Write_Command(0xF1);//

    Write_Command(0xDA);//set com pins hardware configuration
    Write_Command(0x12);//

    Write_Command(0xDB);//set vcomh deselect level
    Write_Command(0x30);//0.83*VCC
```

```
        Write_Command(0x8D);//charge pump setting
        Write_Command(0x14);//enable charge pump,VCC=7.5V

        Write_Command(0xAF);//set display display ON/OFF,AEH/AFH

}
void Write_Command (Uchar Command)
{
        int i;
        CS=0;
        A0=0;
        for(i=0;i<8;i++)
         {
           SCLK=0;
           if((Command&0x80)==0)
              SDA=0;
           else
              SDA=1;
           SCLK=1;
           Command=Command<<1;
         }
        CS=1;
  }
void Write_Data (Uchar Data)
{
        int i;
        CS=0;
        A0=1;
        for(i=0;i<8;i++)
         {
           SCLK=0;
           if((Data&0x80)==0)
              SDA=0;
           else
              SDA=1;
           SCLK=1;
           Data=Data<<1;
         }
        CS=1;
}
```

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11. RELIABILITY

ITEM	CONDITIONS	CRITERION
OPERATING TEMPERATURE	HIGH TEMPERTURE +70℃ 240HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -40℃ 240HRS	
STORAGE TEMPERATURE	HIGH TEMPERTURE +85℃ 240HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE - 40℃ 240HRS	
HUMIDITY	60℃ 90%RH 120HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
VIBRATION	• Operating Time: thirty minutes exposure for each direction (X,Y,Z) • Sweep Frequency: 10～55Hz (1 min) • Amplitude: 1.5mm	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
THERMAL SHOCK	-40℃(60mins) ←→+85℃(60mins), 24 cycles	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

*NOTE: TEST CONDITION

(1)TEMPERATURE AND HUMIDITY: IF NO SPECIFICATION, TEMP. SET AT 25±2℃, HUMIDITY SET AT 60±5%RH

(2) OPERATING STATE: SAMPLES SUBJECT TO THE TESTS SHALL BE IN " OPERATING" CONDITION

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12. Outgoing Quality Control Specifications

12.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

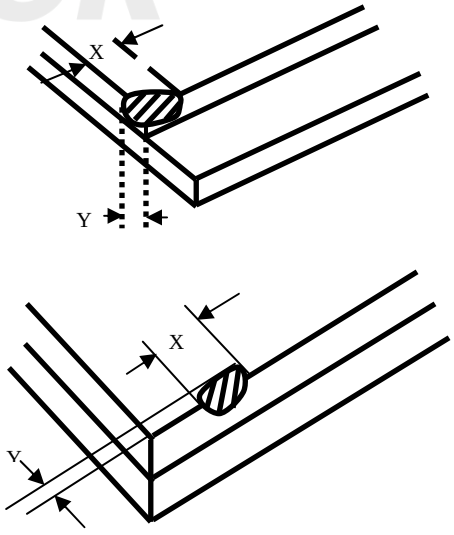
12.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

12.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

12.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

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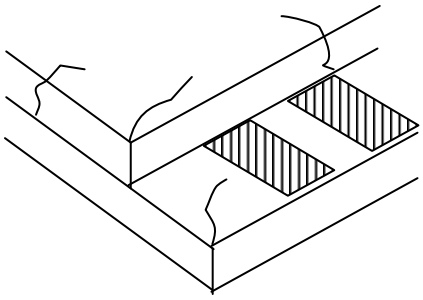
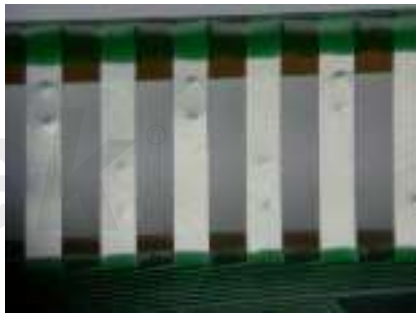
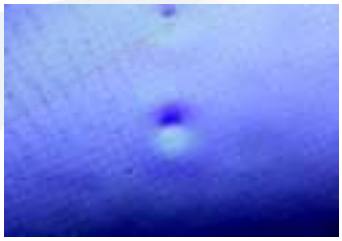
12.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

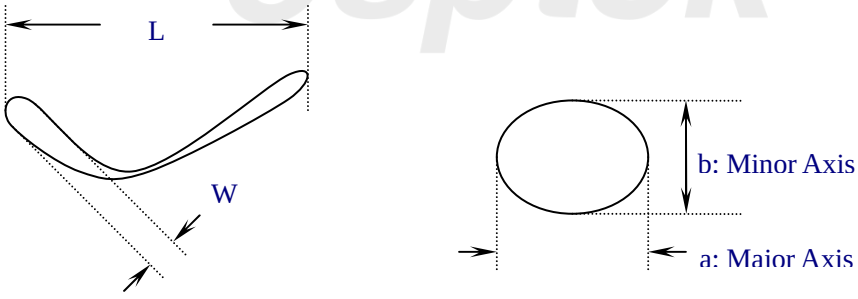
12.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



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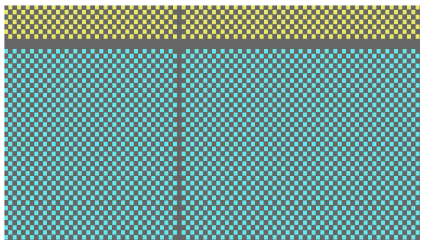
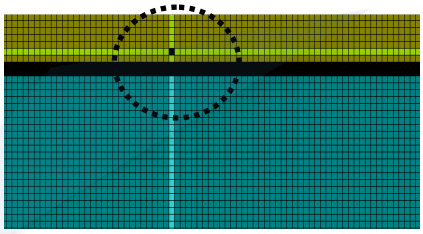
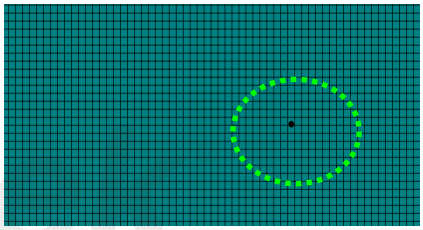
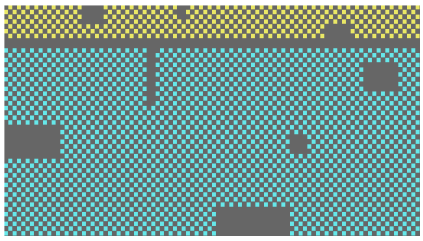
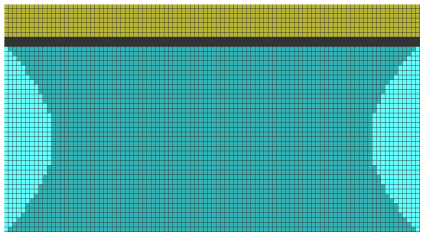
12.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

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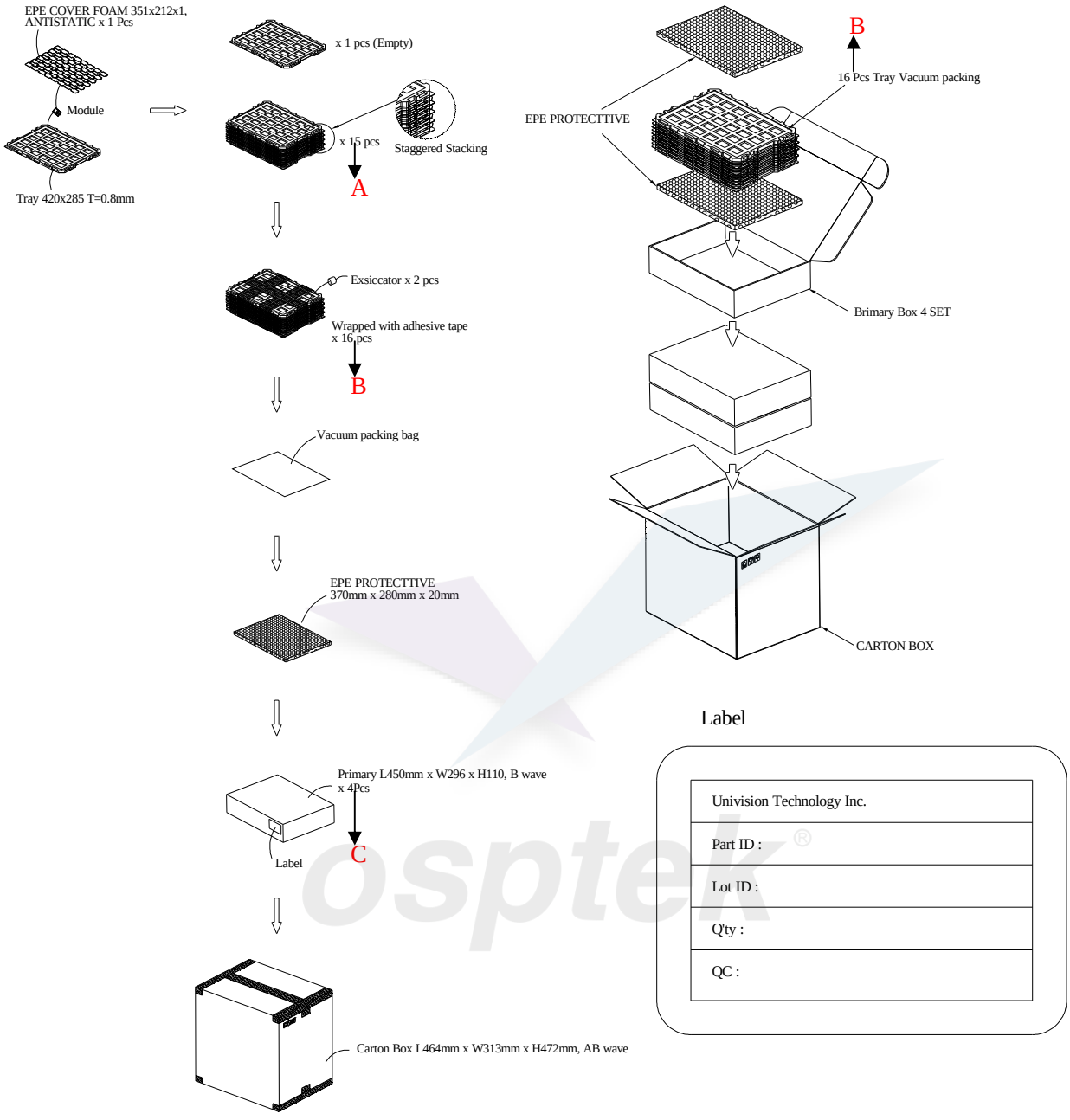
13. Package Specifications



Item		Quantity	
Module		**810**	**per Primary Box**
Holding Trays	**(A)**	**15**	**per Primary Box**
Total Trays	**(B)**	**16**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

14. Precautions When Using These OEL Display Modules

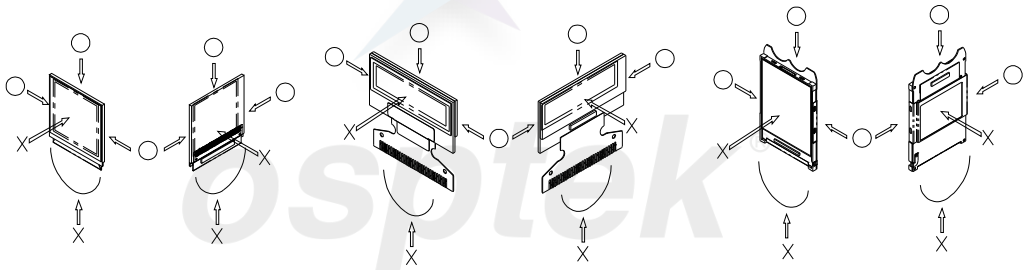
14.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:

   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue

adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

14.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Osptek technology Inc.)

   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

14.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1315

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

14.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

14.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements

change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.

* Design the product and installation method so that the OEL driver may be shielded from light in actual usage.

* Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.

4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

Warranty:

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. **Osptek technology Inc.** shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

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