Osptek Display

LCD Module SPECIFICATION

Model No:

LCM12864Z-4-Y

RECORDS OF REVISION

Date	Rev.	Description	Page	Design by
2011/06/26	0	New Sample.	-	-
			-	-

Contents

1. SPECIFICATIONS

1.1 Features

Item	Standard Value
Display Type	128X64 DOTS
LCD Type	STN (Y-G)，TRANSFLECTIVE
Driver Condition	LCD Module : 1/32Duty , 1/5Bias
Viewing Direction	6 O'clock
Backlight Type	Y-G SIDE Light
Interface	8BIT or Serial bus MPU interface
Driver IC	AIP31020 or eqv

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	93(L) *70(W) * Max 12.5 (T)	mm
Viewing Area	72(L) * 40(W)	mm
Dot Size (W*H)	0.48*0.48mm	
Dot Pitch (W*H)	0.52*0.52 mm	

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDD	-	-0.3	5.5	V
LCD Driver Supply Voltage	$VOUT_{IN}$	-	4.8	5.0	V
Input Voltage	V_{IN}	-	-0.3	VDD + 0.2	V
Operating Temperature	T_{OP}	-	-20	70	°C
Storage Temperature	T_{ST}	-	-30	80	°C
Storage Humidity	H_D	Ta < 40 °C	20	80	%RH

1.4 Backlight Characteristics

LCD Module without LED Backlight

Electrical / Optical Characteristics

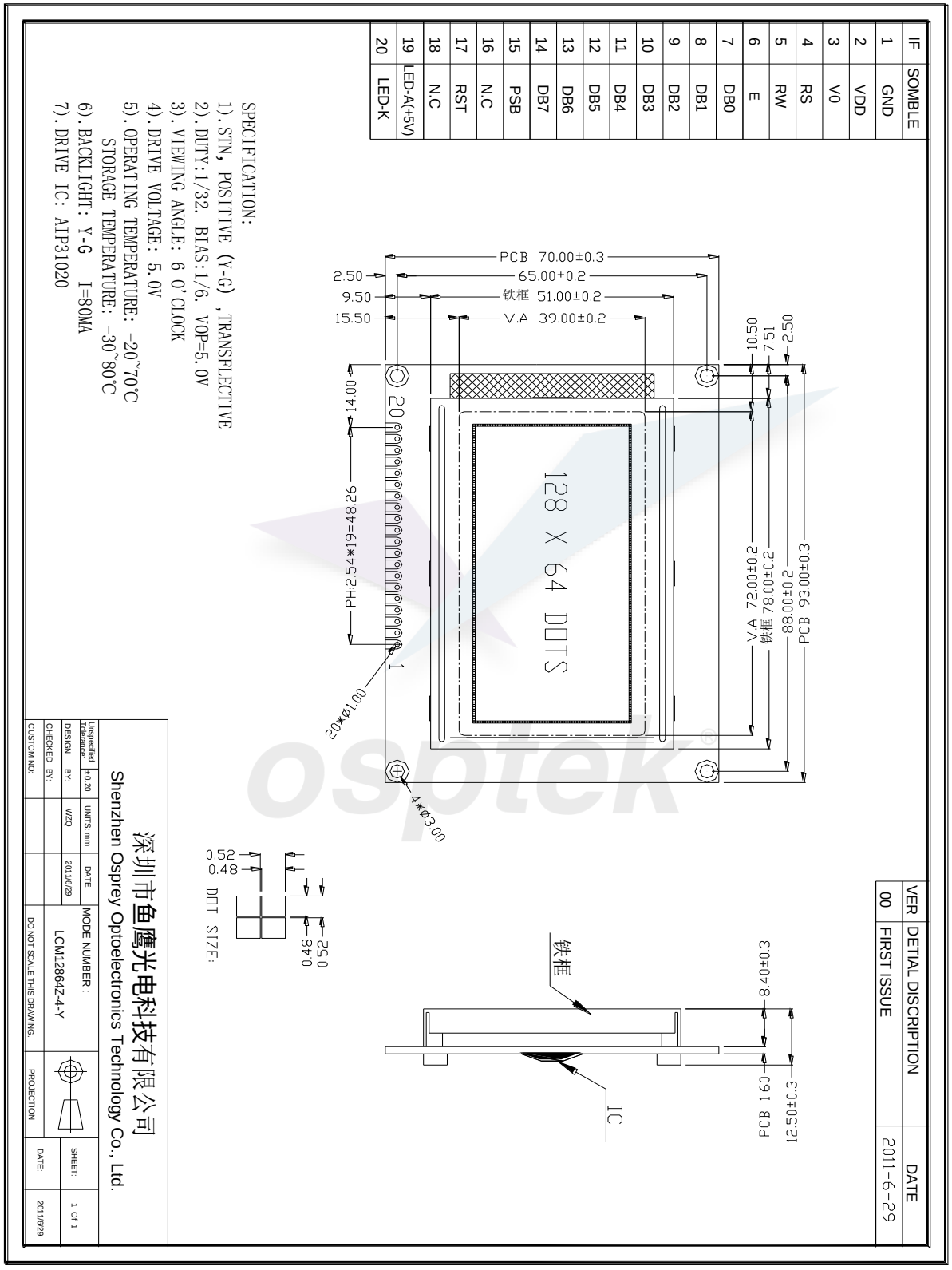
Ta =25℃

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	Vf	If=80mA	3.0	3.1	3.2	V
Reverse Current	Ir	If=8v			--	uA
Average Brightness	IV	If=80mA				cd/m^2
Wavelength (Without LCD)	λ d	If=80mA	--	--	--	nm
Luminous Intensity (without LCD)	Lv Sub	If=80mA				cd/m^2
Uniformity	Δ%	IvMin / IvMax *100%	--	-	-	%
Color	WHITE					

2. MODULE STRUCTURE

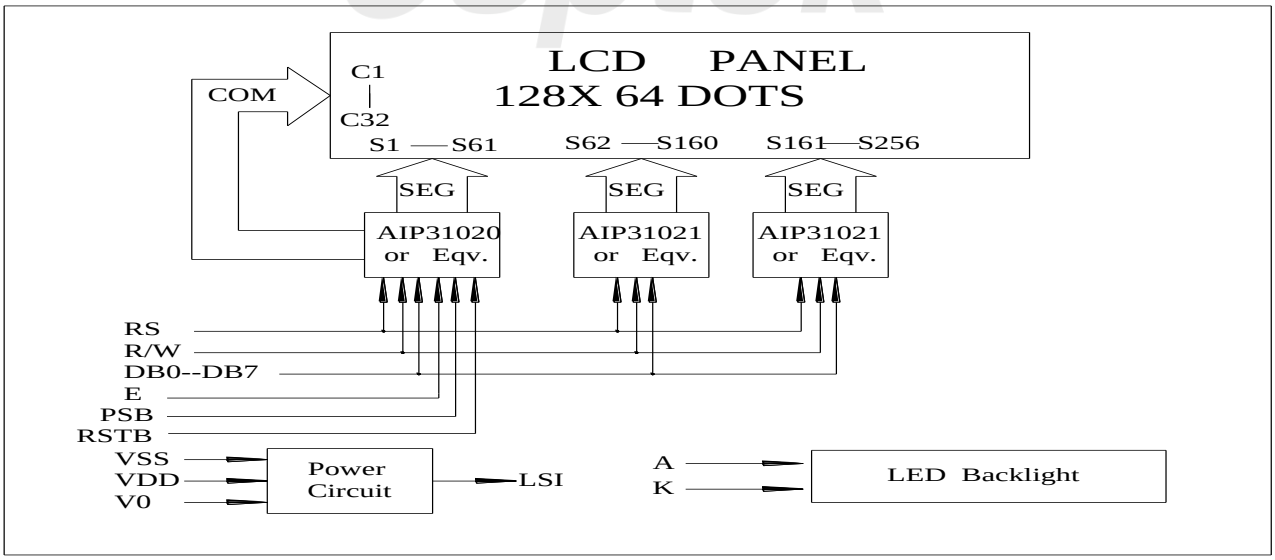
2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram



2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VSS	Ground (0V)
2	VDD	Power supply input for driver IC (+5V)
3	VO	LCD driver supply voltages
4	RS(CS)	Register select input pin - RS = "H": D0 to D7 are display data - RS = "L": D0 to D7 are control data Serial mode: CS=1 :chip enable CS=0 :chip enable
5	RW(SID)	Read write control 0:write 1:read (serial data input)
6	E(SCLK)	Enable trigger (serial clock)
7-10	DB0~DB3	Lower nibble data bus for 8 bit interface
11-14	DB4~DB7	Higher nibble data bus for 8 bit interface and data bus for 4 bit interface
15	PSB	Interface selection:0:serial mode 1:8/4-bits parallel bus mode
16	NC	No used
17	RST	Reset signal
18	NC	No used
19	LED+	BACKLIGHT+ （5V）
20	LED-	BACKLIGHT- （0V）



2.3 Timing Characteristics

AC Characteristics ($T_A = 25^oC$, $V_{DD} = 4.5V$) Parallel Mode Interface

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
OSC Frequency	fosc	R = 33KΩ	480	540	600	KHz
External Clock Operation						
External Frequency	fEX	-	480	540	600	KHz
Duty Cycle		-	45	50	55	%
Rise/Fall Time	TR,TF	-	-	-	0.2	μs
Write Mode (Writing data from MPU to AIP31020)						
Enable Cycle Time	TC	Pin E	1200	-	-	ns
Enable Pulse Width	TPW	Pin E	140	-	-	ns
Enable Rise/Fall Time	TR,TF	Pin E	-	-	25	ns
Address Setup Time	TAS	Pins: RS,RW,E	10	-	-	ns
Address Hold Time	TAH	Pins: RS,RW,E	20	-	-	ns
Data Setup Time	TDSW	Pins: DB0 - DB7	40	-	-	ns
Data Hold Time	TH	Pins: DB0 - DB7	20	-	-	ns
Read Mode (Reading Data from AIP31020 to MPU)						
Enable Cycle Time	TC	Pin E	1200	-	-	ns
Enable Pulse Width	TPW	Pin E	140	-	-	ns
Enable Rise/Fall Time	TR,TF	Pin E	-	-	25	ns
Address Setup Time	TAS	Pins: RS,RW,E	10	-	-	ns
Address Hold Time	TAH	Pins: RS,RW,E	20	-	-	ns
Data Delay Time	TDDR	Pins: DB0 - DB7	-	-	100	ns
Data Hold Time	TH	Pins: DB0 - DB7	20	-	-	ns
Interface Mode with LCD Driver(AIP31021)						
Clock Pulse with High	TCWH	Pins: CL1, CL2	800	-	-	ns
Clock Pulse with Low	TCWL	Pins: CL1, CL2	800	-	-	ns
Clock Setup Time	TCST	Pins: CL1, CL2	500	-	-	ns
Data Setup Time	TSU	Pin: D	300	-	-	ns
Data Hold Time	TDH	Pin: D	300	-	-	ns
M Delay Time	TDM	Pin: M	-1000	-	1000	ns

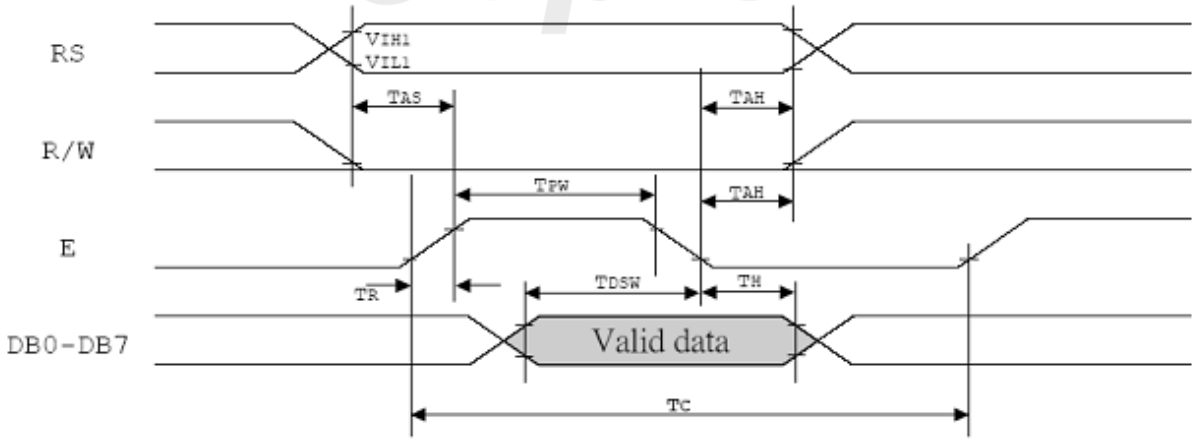
DC Characteristics ($T_A = 25^oC$, $V_{DD} = 4.5\ V - 5.5\ V$)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	-	4.5	-	5.5	V
LCD Voltage	VLCD	V0-VSS	3.0	-	7	V
Power Supply Current	ICC	fOSC= 540KHz, VDD=5V Rf=33KΩ	-	0.45	0.75	mA
Input High Voltage (Except OSC1)	VIH1	-	0.7VDD	-	VDD	V
Input Low Voltage (Except OSC1)	VIL1	-	-0.3	-	0.6	V
Input High Voltage (OSC1)	VIH2	-	VDD-1	-	VDD	V
Input Low Voltage (OSC1)	VIL2	-	-	-	1.0	V
Output High Voltage (DB0 - DB7)	VOH1	IOH= -0.1mA	0.8VDD	-	VDD	V
Output Low Voltage (DB0 - DB7)	VOL1	IOL = 0.1mA	-	-	0.4	V
Output High Voltage (Except DB0 - DB7)	VOH2	IOH = -0.04mA	0.8VDD	-	VDD	V
Output Low Voltage (Except DB0 - DB7)	VOL2	IOL= 0.04mA	-	-	0.1VDD	V
Input Leakage Current	ILEAK	VIN= 0V to VDD	-1	-	1	μA
Pull Up MOS Current	IPUP	VDD= 5V	75	80	85	μA

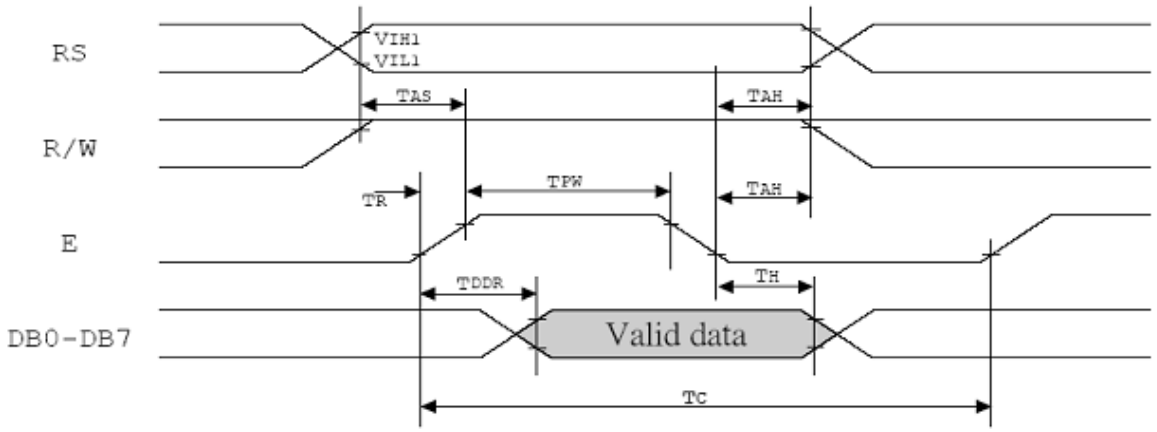
◆

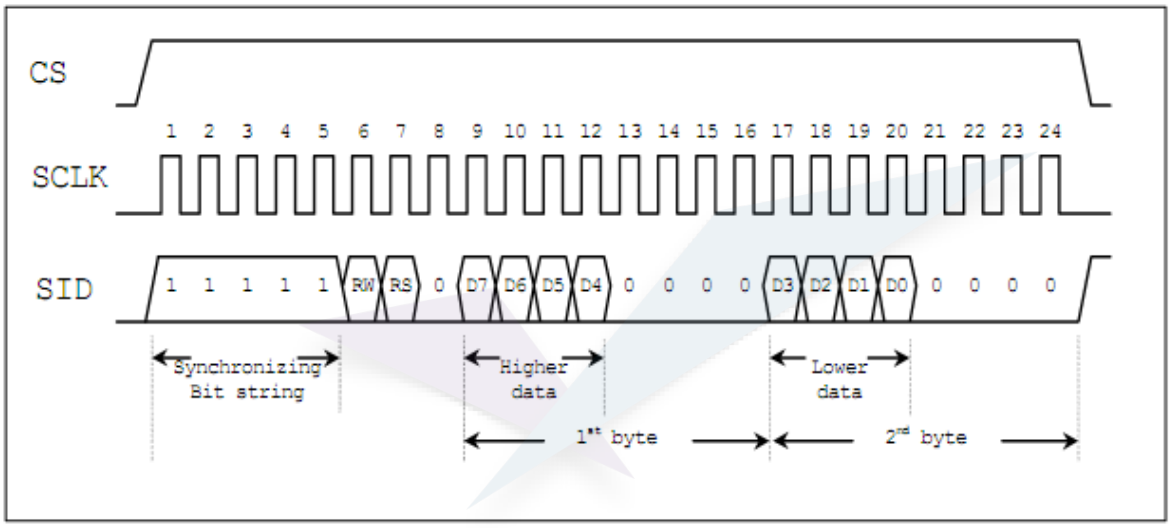
8 bit interface timing diagram

- **MPU write data to AIP31020**



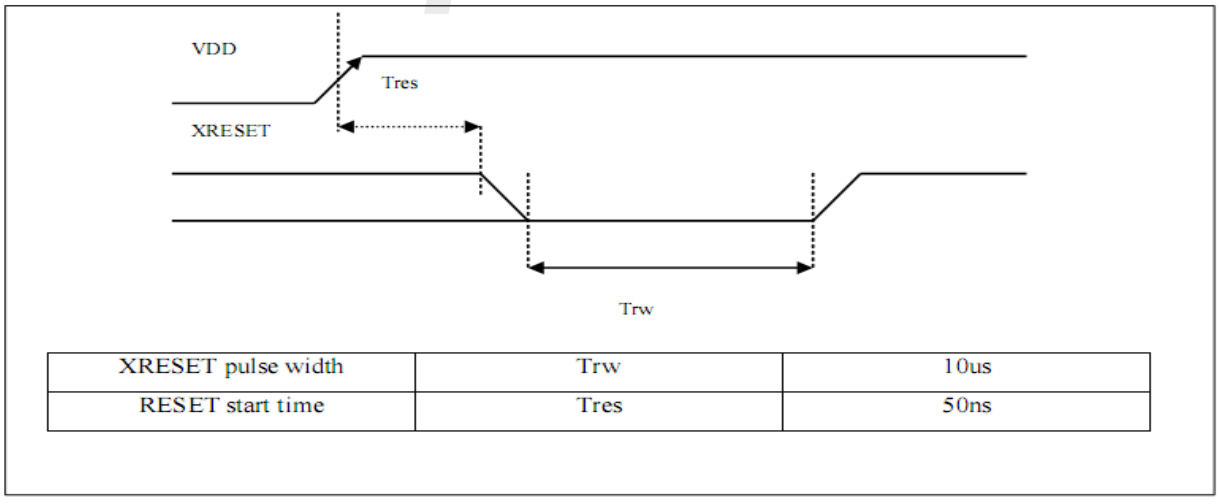
- **MPU read data from AIP31020**





Timing Diagram of Serial Mode Data Transfer

External reset timing



XRESET pulse width	Trw	10us
RESET start time	Tres	50ns

2.4 Instruction Table

Instruction set 1: (RE=0: basic instruction)

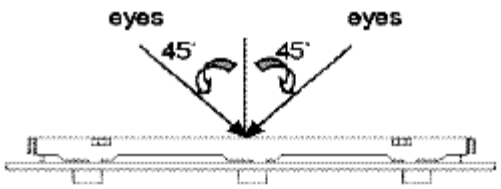
Ins	code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CLEAR	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H", and set DDRAM address counter （AC）to "00H"	1.6 ms
HOME	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter（AC）to "00H", and put cursor to origin ；the content of DDRAM are not changed	72us
ENTRY MODE	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation	72us
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1: display ON C=1: cursor ON B=1: blink ON	72 us
CURSOR DISPLAY CONTROL	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control ；the content of DDRAM are not changed	72 us
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1: extended instruction** **RE=0: basic instruction**	72 us
SET CGRAM ADDR.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter（AC） **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
SET DDRAM ADDR.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter（AC） AC6 is fixed to 0	72 us
READ BUSY FLAG（BF）& ADDR.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag（BF）for completion of internal operation, also Read out the value of address counter（AC）	0 us
WRITE RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/IRAM/GDRAM)	72 us
READ RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/IRAM/GDRAM)	72 us

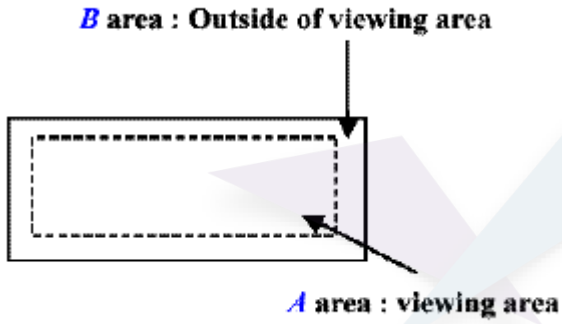
Instruction set 2: (RE=1: extended instruction)

Inst.	code										description	Exec. time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
STAND BY	0	0	0	0	0	0	0	0	0	1	Enter stand by mode, any other instruction can terminate (Com1..32 halted, only Com33 ICON can display)	72 us
SCROLL or RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	SR=1: enable vertical scroll position SR=0: enable IRAM address **(extended instruction)** SR=0: enable CGRAM address**(basic instruction)**	72 us
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction **R1,R0 initial value is 00**	72 us
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1: extended instruction set** **RE=0: basic instruction set** G=1 :graphic display ON G=0 :graphic display OFF	72 us
SET IRAM or SCROLL ADDR	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5~AC0 the address of vertical scroll SR=0: AC3~AC0 the address of ICON RAM	72 us
SET GRAPHIC RAM ADDR.	0	0	1	0 0	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set GDRAM address to address counter（AC） First set vertical address and the horizontal address by consecutive writing Vertical address range AC5...AC0 Horizontal address range AC3... AC0	72 us

2.5 Inspection Specification

◆Inspection Standard : MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ .
◆Equipment : Gauge、MIL-STD、Powertip Tester、Sample
◆Defect Level : Major Defect AQL 0.4; Minor Defect AQL 1.5 .
◆OUT Going Defect Level : Sampling .
◆Manner of appearance test :
(1). The test be under 40W×2 fluorescent light ' and distance of view must be at 30 cm.
(2). The test direction is base on about around 45° of vertical line. (Fig. 1)
(3). Definition of area . (Fig. 2)

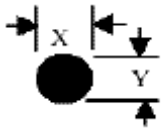
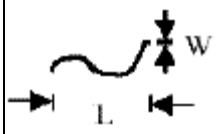




◆ Specification:

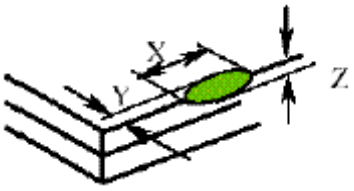
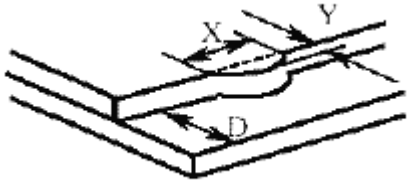
NO	Item	Criterion	level
01	Product condition	1.1 The part number is inconsistent with work order of Production.	Major
		1.2 Mixed production types.	Major
		1.3 Assembled in inverse direction.	Major
02	Quantity	2.1 The quantity is inconsistent with work order of production.	Major
03	Outline dimension	3.1 Product dimension and structure must conform to Structure diagram.	Major
04	Electrical Testing	4.1 Missing line character、dot and icon.	Major
		4.2 No function or no display.	Major
		4.3 Output data is error.	Major
		4.4 LCD viewing angle defect.	Major
		4.5 Current consumption exceeds product specifications.	Major
05	Black or white dot、scratch、contamination Round type	5.1 Round type: 5.1.1 display only : · White and black spots on display ≦ 0.25mm, no more than Four white or black spots present. · Densely spaced : NO more than two spots or lines within 3mm	Minor

◆Specification :

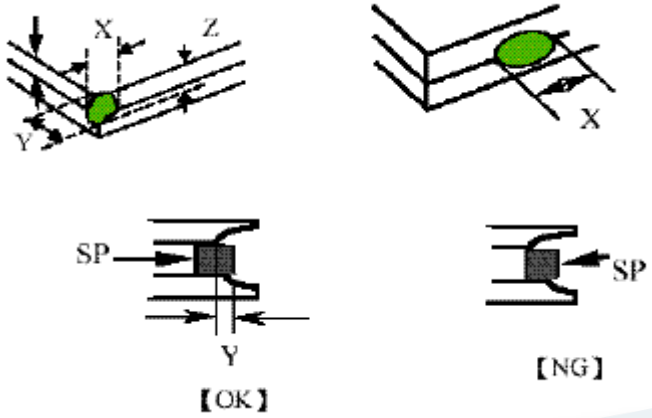
NO	Item	Criterion	level
05	Black or white dot、scratch、contamination Round type  Φ=(x+y)/2  	5.1.2 Nom-display : Dimension (diameter : Φ) Acceptance(Q'ty) Φ≦0.10mm Accept no dense 0.10mm＜Φ≦0.20mm 3 0.20mm＜Φ≦0.25mm 2 Total 4 5.1.3 Line type: Dimension (diameter : Φ) Acceptance (Q'ty) Length width A area B area --- w≦0.03mm Accept no dense Don't count L≦3.0mm 0.03mm＜Φ≦0.05mm 4 Don't count L≦2.5mm 0.05mm＜Φ≦0.075mm Don't count --- w＞0.075mm As round type	Minor

06	Polarizer Bubble	Dimension (diameter : Φ) Acceptance(Q'ty) A area B area Φ ≦0.20mm Accept no dense Don't count 0.20mm＜ Φ ≦0.50mm 3 Don't count 0.50mm＜ Φ ≦1.00mm 2 Don't count Φ ＞1.00mm 0 Don't count Total quantity 4 Don't count	Minor
07	The crack of glass	● Glass Crack: 7.1 Crack on the circuit of electrode terminal :  X Y Z Front X≦1/5 a Y≦ 1/2 D Z≦ t Back Neglect	Minor

◆Specification :

NO	Item	Criterion	Level
07	The crack of glass X: The length of Crack Y: The width of crack Z: The thickness of crack D: terminal length T: The thickness of glass A : The length of glass	● Glass Crack: 7.2 General glass crack and corner edge: 7.2.1  X Y Z Neglect Out A area Neglect 7.2.2  X Y Z Neglect Out A area Neglect	Minor
		7.3 Glass remain:  X Y Neglect ≦ 1/3 d	Minor

◆Specification :

NO	Item	Criterion	Level
07	The crack of glass X: The length of Crack Y: The width of crack Z: The thickness of crack D: terminal length T: The thickness of glass A : The length of glass	7.4 Corner crack and medial crack:  X Y Z ≦1/5a Crack can't enter viewing area ≦1/2t ≦1/5a Crack can't exceed the half of width of SP width of SP 1/2t<Z≦2t	Minor
08	Backlight elements	8.1 Backlight can't work normally.	Major
		8.2 Backlight doesn't light or color is wrong.	Major
		8.3 Illumination source flickers when lit.	Major
09	General appearance	9.1 pin type must match type in specification sheet	Major
		9.2 No short circuits in components on PCB or FPC	Major
		9.3Product packaging must the same as specified on packaging specification sheet.	Major
		9.4 The folding and peeled off in polarizer are not acceptable	Major
		9.5 The PCB or FPC between B/L assembled distance (PCB or FPC) is ≦1.5mm	Major