GC9702C

a-Si TFT LCD Single-Chip Driver
720(RGB)x1440 Resolution,
16.7M-color Without internal GRAM

Datasheet

V1.0

2021-11-16

Ordering Information

◆ **GC9702C**

(a-Si TFT LCD Single Chip Driver)

(720(RGB)x1440 Resolution, 16.7M-color Without internal GRAM)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2021-11-16	Document Release	Xin

Galaxycore Incorporation

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Table of Content

1. DESCRIPTION

The GC9702C device is a 16.7M single-chip (SOC) driver. It is comprised of a 2160-channel source driver (S1~S1080, S1321~S2400 and S_RA,S_LB), a gate-IC-less level shifter and a power supply circuit to drive a dot-matrix TFT LCD with 720 (RGB) x 1440 dots at maximum.

The GC9702C can configure functions via the MIPI[1] DSI[2] Interface; transmit video data via MIPI DSI Interface. The GC9702C supports three kinds of data types, i.e., 16-bit, 18-bit and 24-bit, for video image display in MIPI DSI interfaces. In the MIPI DSI high-speed mode, the GC9702C also provides three user-selectable hardware structures:

- Two data lanes supports up to 1 Gbps on the MIPI DSI link
- Three data lanes supports up to 860Mbps on the MIPI DSI link
- Four data lanes supports up to 600Mbps on the MIPI DSI link

The GC9702C can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The GC9702C supports Idle Mode (8-color low power mode) display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

2. FEATURES

Display resolution option
- 720RGB x (480+4*N)
- 640RGB x (480+4*N)
- 600RGB x (480+4*N)

Display mode (Color mode)
- Full color mode: 16.7M-colors
- Reduce color mode: 262K colors
- Reduce color mode: 65K colors
- Idle mode: 8 colors

Interface
- MIPI Display Serial Interface (DSI V1.02 and D-PHY V1.2)
  Supports 2 data lanes / maximum speed 1Gbps
  Supports 3 data lanes / maximum speed 860Mbps
  Supports 4 data lanes / maximum speed 600Mbps

Display features
- Supports 2160 source channel outputs (S1~S1080 , S1321~S2400 and S_R and S_LB)
- Supports gate control signals to gate driver in the panel
- Supports 1-dot , 2-dot , 3-dot , 4-dot , column , Zig-Zag inversion
- Gamma correction (1 preset Gamma curve)
- On module VCOM control

Power saving modes:
- Sleep mode
- Idle mode

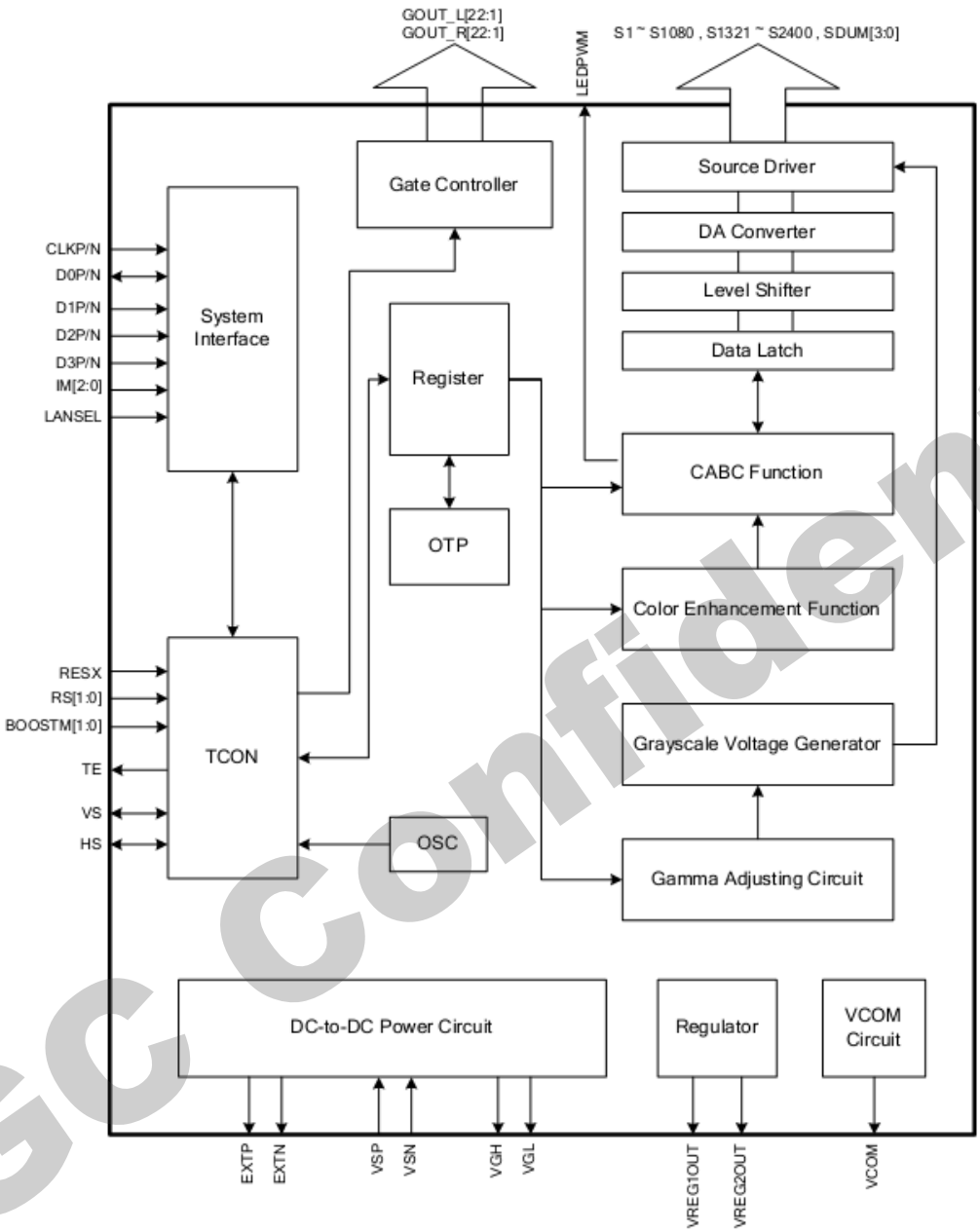
Other on-chip functions/Miscellaneous
- Software programmable color depth mode
- Oscillator for display clock generation
- DC VCOM voltage generator and adjustment
- CABC (Content Adaptive Brightness Control) function
- DGC (Digital Gamma Correction) function
- CE (Color Enhancement) function
- VGH/VGL voltage generator for gate control signal in panel
- Gate control signals to gate driver in panel (GIP)
- OTP (One-Time Programming) memory store initialization register settings
- Provide 3 times to store DC VCOM value setting and ID1 ~ ID3

Input power：

- External power IC and PFM：
  I/O and interface power supply (IOVCC)：1.65V to 3.3V
  Analog power supply (VCI)：2.5V to 3.3V
- Three-Power Mode：
  I/O and interface power supply (IOVCC)：1.65V to 3.3V
  Analog power supply (VSP)：4.5V to 6.0V
  Analog power supply (VSN)：-4.5V to -6.0V
- Output voltage：
  Positive source output voltage level: VSPR=3.3V to 5.6V
  Negative source output voltage level: VSNR=-5.6V to -3.3V
  Positive gate driver output voltage level: VGH=+10V to +20V
  Negative gate driver output voltage level: VGL=-7.5V to -15V
  VCOM=-3.5V to 0V

Operate temperature range: −40℃ to +80℃

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1. PIN DESCRIPTION

<table>
<tr><th colspan="3">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[2:0]</td><td>I</td><td>
-Select the interface mode
Interface type selection. The connections of IM[2:0] which not shown in table are invalid.
<table>
<tr><th colspan="4">External Pad Set</th><th>register</th><th colspan="5">Configuration of MIPI Lane</th></tr>
<tr><th>LANSEL</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Page0_reg_BA_bit0</th><th>CLKP/N</th><th>D0P/N</th><th>D1P/N</th><th>D2P/N</th><th>D3P/N</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>CLKP/N</td><td>D3P/N</td><td>D2P/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>CLKN/P</td><td>D3N/P</td><td>D2N/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>CLKP/N</td><td>D0P/N</td><td>D1P/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>CLKN/P</td><td>D0N/P</td><td>D1N/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>CLKP/N</td><td>D3P/N</td><td>D0P/N</td><td>D1P/N</td><td>D2P/N</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>CLKN/P</td><td>D3N/P</td><td>D0N/P</td><td>D1N/P</td><td>D2N/P</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>CLKP/N</td><td>D2P/N</td><td>D1P/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>CLKN/P</td><td>D2N/P</td><td>D1N/P</td><td>D0N/P</td><td>D3N/P</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CLKP/N</td><td></td><td>D2P/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>CLKN/P</td><td></td><td>D2N/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>CLKP/N</td><td>D0P/N</td><td>D1P/N</td><td>D2P/N</td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>CLKN/P</td><td>D0N/P</td><td>D1N/P</td><td>D2N/P</td><td></td></tr>
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<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>CLKP/N</td><td>D2P/N</td><td>D1P/N</td><td>D0P/N</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>CLKN/P</td><td>D2N/P</td><td>D1N/P</td><td>D0N/P</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CLKP/N</td><td></td><td></td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>CLKN/P</td><td></td><td></td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>CLKP/N</td><td>D0P/N</td><td>D1P/N</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>CLKN/P</td><td>D0N/P</td><td>D1N/P</td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>CLKP/N</td><td></td><td>D0P/N</td><td>D1P/N</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>CLKN/P</td><td></td><td>D0N/P</td><td>D1N/P</td><td></td></tr>
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<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>CLKN/P</td><td></td><td>D1N/P</td><td>D0N/P</td><td></td></tr>
<tr><td colspan="5">Others</td><td colspan="5">Reserved</td></tr>
</table>
</td></tr>
<tr><td>LANSEL</td><td>I</td><td>- MIPI DSI Lane number selection pin
LANSEL=”1”, MIPI DSI is 2 Lane mode
LANSEL=”0”, MIPI DSI is 3 or 4 Lane mode</td></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
Fix to VDDI level when not in use.</td></tr>
</table>

<table>
<tr><td>RS[1:0]</td><td>I</td><td>- Resolution selection pins
<table>
<tr><th>RS[1]</th><th>RS[0]</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>600RGB x (480+4*N)</td></tr>
<tr><td>0</td><td>1</td><td>640RGB x (480+4*N)</td></tr>
<tr><td>1</td><td>0</td><td>720RGB x (480+4*N)</td></tr>
</table></td></tr>
<tr><td>BOOSTM[1:0]</td><td>I</td><td>- Power type selection pins
<table>
<tr><th>BOOSTM[1]</th><th>BOOSTM[0]</th><th>Power mode</th></tr>
<tr><td>1</td><td>0</td><td>2 power
External VDDI and VCI Note 2</td></tr>
<tr><td>0</td><td>0</td><td rowspan="3">3 power
Extenal VDDI,VSP and VSN (VCI=VSP) Note 1</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td colspan="2">prohibited</td><td>-</td></tr>
</table>
Note 1: VCI and VSP pads must be connected by external metal path.
Note 2: Power voltage VCI VDDI is the requirement for power mode 3</td></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
Fix to VDDI level when not in use.</td></tr>
<tr><td>TE</td><td>I</td><td>- Tearing effect output pin.
Leave the pin open when not in use.</td></tr>
<tr><td>VS</td><td>I/O</td><td>- Touch synchronization signal (VSOUT).
Fix to VSS level when not in use.</td></tr>
<tr><td>HS</td><td>I/O</td><td>- Touch synchronization signal (HSOUT).
Fix to VSS level when not in use.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>- The PWM frequency output for LED driver control.
Leave the pin to open when not in use.</td></tr>
<tr><td>CLKP
CLKN</td><td>I</td><td>MIPI DSI differential clock pair (DSI-CLK+/-).
If MIPI are not used, they should be connected to DGND.</td></tr>
<tr><td>HS_D0P
HS_D0N</td><td>I/O</td><td>MIPI DSI differential data pair (DSI-D0+/-).
If MIPI are not used, they should be connected to DGND</td></tr>
<tr><td>HS_D1P
HS_D1N</td><td>I</td><td>MIPI DSI differential data pair (DSI-D1+/-).
If MIPI are not used, they should be connected to DGND</td></tr>
<tr><td>HS_D2P
HS_D2N</td><td>I</td><td>MIPI DSI differential data pair (DSI-D2+/-).
If MIPI are not used, they should be connected to DGND</td></tr>
<tr><td>HS_D3P
HS_D3N</td><td>I</td><td>MIPI DSI differential data pair (DSI-D3+/-).</td></tr>
</table>

		If MIPI are not used, they should be connected to DGND
Driver Output		
Pin Name	**I/O**	**Description**
GOUT_L[22:1]	O	- Gate control signals for panel in left side of IC. ***Leave the pin open when not in use.***
GOUT_R[22:1]	O	- Gate control signals for panel in right side of IC. ***Leave the pin open when not in use.***
S[1:1080] S[2400:1321] S_RA S_LB	O	- Source output voltage signals applied to a LCD panel. Source output mapping with different resolution Disaply resulation / Source channels 720 (RGB) / S1 ~ S1080, S1321 ~ S2400 640 (RGB) / S1 ~ S960, S1441 ~ S2400 600 (RGB) / S1 ~ S900, S1501 ~ S2400 Zigzag / S1 ~ S1080, S1321 ~ S2400, S_RA,S_LB
VCOM	O	-Regulator output for common voltage of panel **NoteVcom pad(IC pad number 25~27) must connect to another side of the Vcom pad(IC pad number 582~584) via the FPC.** You can connect a 2.2uF capacitor to keep stable.
Charge Pump Pin		
Pin Name	**I/O**	**Description**
AVDDR AVDDB	I	-Power supply for Analog system You can connect a 2.2uF capacitor to keep stable.
AVEER AVEEB	I	-Power supply for Analog system You can connect a 2.2uF capacitor to keep stable.
VGH	O	- Output positive voltage from step-up circuit for the liquid crystal panel
VGL	O	- Output negative voltage from step-up circuit for the liquid crystal panel.
EXTP	O	- Control signal output to generate VSP / VSN.
EXTN	O	- Control signal output to generate VSP / VSN.
Power Pin		
Pin Name	**I/O**	**Description**
VCI	I	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 3.3V You can connect a 2.2uF capacitor to keep stable.
VDDIB VDDIR	I	- Power supply for I/O pads. Connect to an external 3.3V power supply of 1.65V to 3.3V You can connect a 1uF capacitor to keep stable.

DVDD	O	- internal logic voltage output
VGMP/VGSP	O	- Output voltage generated from VSP. LDO output for positive gamma voltage generator.
VGMN/VGSN	O	- Output voltage generated from VSN. LDO output for negative gamma voltage generator.
VSSA	I	- System ground for analog circuit.
VSSAM	I	- System ground for MIPI circuit.
VSSR	I	- System ground for internal digital system.
VSSB	I	- System ground for DC/DC convertor.
DVSS	I	- System ground for Digital circuit.
VPP	I	- OTP programming power.

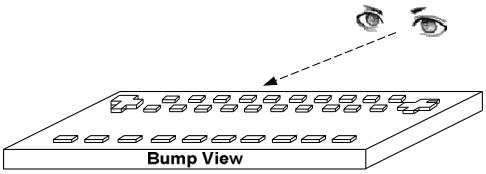
4.2. Output Bump Dimension

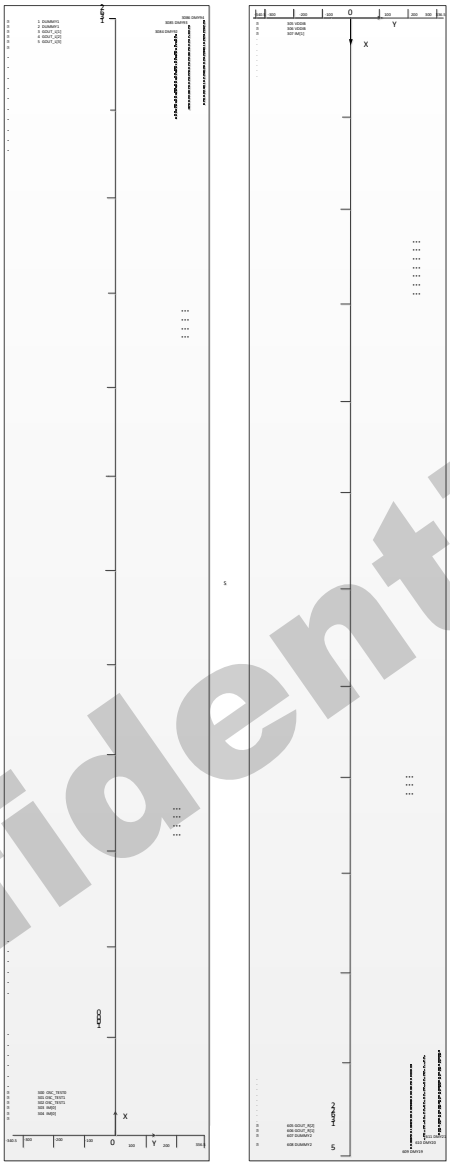
Au bump height： 9μm

Au bump size:

16μm x 65μm
Pad 609 to pad 3086

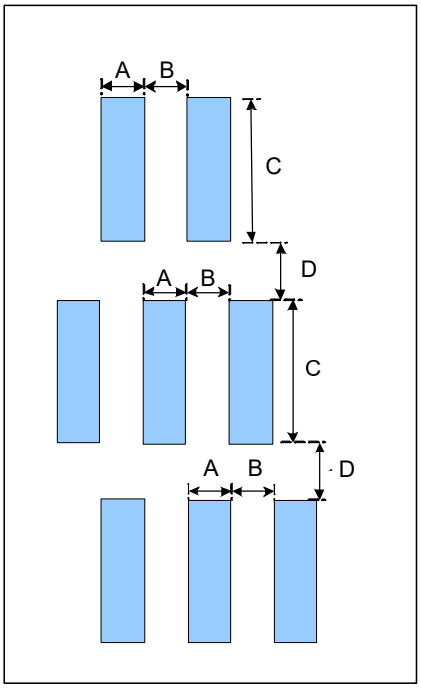
30μm x 43μm
Pad 1 to Pad 608





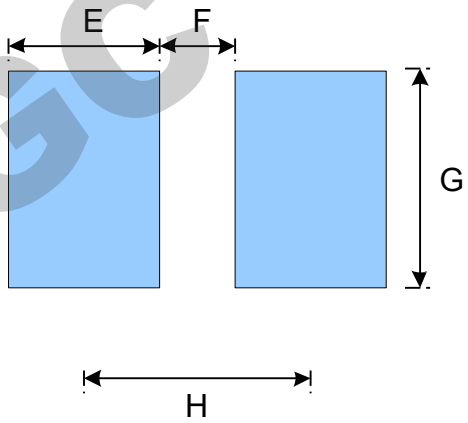
4.3. Input Bump Dimension

- **Output Pads**



Symbol	Item	Size
A	Bump Width	16 um
B	Bump Gap 1 (Horizontal)	17 um
C	Bump Height	65 um
D	Bump Gap 2 (Vertical)	27 um

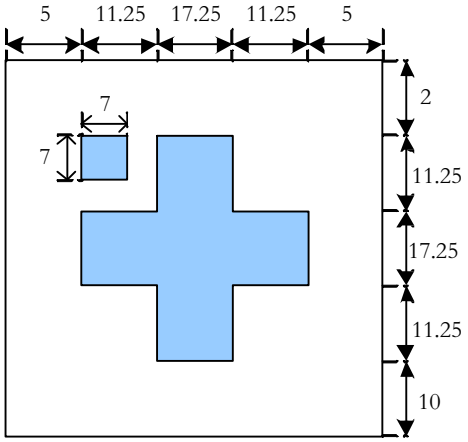
- **Input Pads**



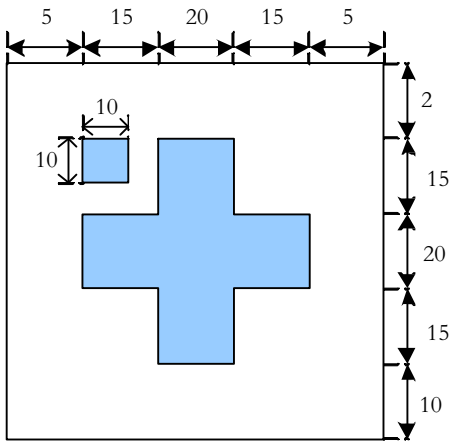
Symbol	Item	Size
E	Bump Width	30 um
F	Bump Gap	15um
G	Bump Height	43 um
H	Bump Pitch	45 um
	Bump thickness	9 um

4.4. Alignment Mark Dimension

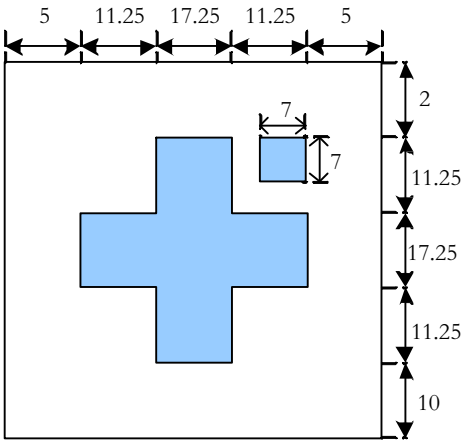
- **Alignment Mark ALIGN_L1 : (X,Y)=(-13706,346)**



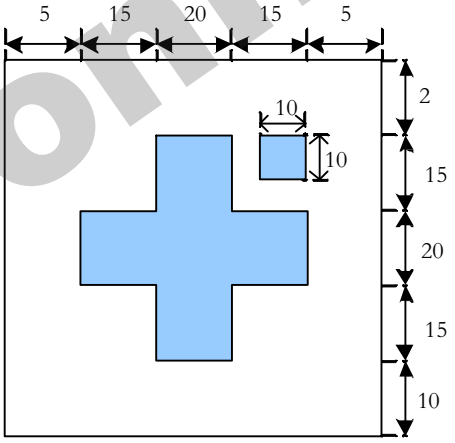
- **Alignment Mark ALIGN_L2 : (X,Y)=(-13706,259)**



- **Alignment Mark ALIGN_R1 : (X,Y)=(+13706,346)**



- **Alignment Mark ALIGN_R2 : (X,Y)=(+13706,259)**



4.5. Chip Information

Chip size	28060μm x830μm(include scribe line)
Chip thickness	200um
Pad Location	Pad center
Coordinate Origin	Chip center

4.6. Pad Coordination

No.	Name	X	Y
1	DUMMY1	-13622.5	-340.5
2	DUMMY1	-13622.5	-340.5
3	GOUT_L[1]	-13577.5	-340.5
4	GOUT_L[2]	-13532.5	-340.5
5	GOUT_L[3]	-13487.5	-340.5
6	GOUT_L[4]	-13442.5	-340.5
7	GOUT_L[5]	-13397.5	-340.5
8	GOUT_L[6]	-13352.5	-340.5
9	GOUT_L[7]	-13307.5	-340.5
10	GOUT_L[8]	-13262.5	-340.5
11	GOUT_L[9]	-13217.5	-340.5
12	GOUT_L[10]	-13172.5	-340.5
13	GOUT_L[11]	-13127.5	-340.5
14	GOUT_L[12]	-13082.5	-340.5
15	GOUT_L[13]	-13037.5	-340.5
16	GOUT_L[14]	-12992.5	-340.5
17	GOUT_L[15]	-12947.5	-340.5
18	GOUT_L[16]	-12902.5	-340.5
19	GOUT_L[17]	-12857.5	-340.5
20	GOUT_L[18]	-12812.5	-340.5
21	GOUT_L[19]	-12767.5	-340.5
22	GOUT_L[20]	-12722.5	-340.5
23	GOUT_L[21]	-12677.5	-340.5
24	GOUT_L[22]	-12632.5	-340.5
25	VCOM	-12587.5	-340.5
26	VCOM	-12542.5	-340.5
27	VCOM	-12497.5	-340.5
28	VSSB	-12442.5	-340.5
29	VSSB	-12397.5	-340.5
30	VSSB	-12352.5	-340.5
31	VSSB	-12307.5	-340.5
32	VSSB	-12262.5	-340.5
33	VSSB	-12217.5	-340.5
34	VSSB	-12172.5	-340.5
35	VSSB	-12127.5	-340.5
36	VSSB	-12082.5	-340.5
37	VSSB	-12037.5	-340.5
38	VDDMA	-11992.5	-340.5
39	VDDMA	-11947.5	-340.5
40	VSSAM	-11902.5	-340.5
41	D0N	-11857.5	-340.5
42	D0N	-11812.5	-340.5
43	D0N	-11767.5	-340.5
44	D0N	-11722.5	-340.5
45	D0N	-11677.5	-340.5
46	D0N	-11632.5	-340.5
47	D0P	-11587.5	-340.5
48	D0P	-11542.5	-340.5
49	D0P	-11497.5	-340.5
50	D0P	-11452.5	-340.5
51	D0P	-11407.5	-340.5
52	D0P	-11362.5	-340.5
53	VSSAM	-11317.5	-340.5
54	D1N	-11272.5	-340.5
55	D1N	-11227.5	-340.5
56	D1N	-11182.5	-340.5
57	D1N	-11137.5	-340.5
58	D1N	-11092.5	-340.5
59	D1N	-11047.5	-340.5
60	D1P	-11002.5	-340.5
61	D1P	-10957.5	-340.5
62	D1P	-10912.5	-340.5
63	D1P	-10867.5	-340.5
64	D1P	-10822.5	-340.5
65	D1P	-10777.5	-340.5
66	VSSAM	-10732.5	-340.5
67	CLKN	-10687.5	-340.5
68	CLKN	-10642.5	-340.5
69	CLKN	-10597.5	-340.5
70	CLKN	-10552.5	-340.5
71	CLKN	-10507.5	-340.5
72	CLKN	-10462.5	-340.5
73	CLKP	-10417.5	-340.5
74	CLKP	-10372.5	-340.5
75	CLKP	-10327.5	-340.5
76	CLKP	-10282.5	-340.5
77	CLKP	-10237.5	-340.5
78	CLKP	-10192.5	-340.5
79	VSSAM	-10147.5	-340.5
80	D2N	-10102.5	-340.5
81	D2N	-10057.5	-340.5
82	D2N	-10012.5	-340.5
83	D2N	-9967.5	-340.5
84	D2N	-9922.5	-340.5
85	D2N	-9877.5	-340.5
86	D2P	-9832.5	-340.5
87	D2P	-9787.5	-340.5
88	D2P	-9742.5	-340.5
89	D2P	-9697.5	-340.5
90	D2P	-9652.5	-340.5
91	D2P	-9607.5	-340.5
92	VSSAM	-9562.5	-340.5
93	D3N	-9517.5	-340.5
94	D3N	-9472.5	-340.5
95	D3N	-9427.5	-340.5
96	D3N	-9382.5	-340.5
97	D3N	-9337.5	-340.5
98	D3N	-9292.5	-340.5
99	D3P	-9247.5	-340.5
100	D3P	-9202.5	-340.5
101	D3P	-9157.5	-340.5
102	D3P	-9112.5	-340.5
103	D3P	-9067.5	-340.5
104	D3P	-9022.5	-340.5
105	VSSAM	-8977.5	-340.5
106	VSSAM	-8932.5	-340.5
107	VSSAM	-8887.5	-340.5
108	VSSAM	-8842.5	-340.5
109	VSSAM	-8797.5	-340.5
110	VSSAM	-8752.5	-340.5
111	VSSAM	-8707.5	-340.5
112	VSSAM	-8662.5	-340.5
113	VSSAM	-8617.5	-340.5
114	VSSAM	-8572.5	-340.5
115	VSSAM	-8527.5	-340.5
116	VSSAM	-8482.5	-340.5
117	AVEEB	-8437.5	-340.5
118	AVEEB	-8392.5	-340.5
119	AVEEB	-8347.5	-340.5
120	AVEEB	-8302.5	-340.5
121	AVEEB	-8257.5	-340.5
122	AVEEB	-8212.5	-340.5
123	AVEEB	-8167.5	-340.5
124	AVEEB	-8122.5	-340.5
125	AVEEB	-8077.5	-340.5
126	AVEEB	-8032.5	-340.5
127	AVEEB	-7987.5	-340.5
128	AVEEB	-7942.5	-340.5
129	AVDDB	-7897.5	-340.5
130	AVDDB	-7852.5	-340.5
131	AVDDB	-7807.5	-340.5
132	AVDDB	-7762.5	-340.5
133	AVDDB	-7717.5	-340.5
134	AVDDB	-7672.5	-340.5
135	AVDDB	-7627.5	-340.5
136	AVDDB	-7582.5	-340.5
137	AVDDB	-7537.5	-340.5
138	AVDDB	-7492.5	-340.5
139	AVDDB	-7447.5	-340.5
140	AVDDB	-7402.5	-340.5
141	VSSB	-7357.5	-340.5
142	VSSB	-7312.5	-340.5
143	VSSB	-7267.5	-340.5
144	VSSB	-7222.5	-340.5
145	VSSB	-7177.5	-340.5
146	VSSB	-7132.5	-340.5
147	VSSB	-7087.5	-340.5
148	VSSB	-7042.5	-340.5
149	VSSB	-6997.5	-340.5
150	VSSB	-6952.5	-340.5
151	VSSB	-6907.5	-340.5
152	VSSB	-6862.5	-340.5
153	VSSB	-6817.5	-340.5
154	VSSB	-6772.5	-340.5
155	VSSB	-6727.5	-340.5
156	DVSS	-6682.5	-340.5
157	DVSS	-6637.5	-340.5
158	DVSS	-6592.5	-340.5
159	DVSS	-6547.5	-340.5
160	DVSS	-6502.5	-340.5
161	DVSS	-6457.5	-340.5
162	DVSS	-6412.5	-340.5
163	DVSS	-6367.5	-340.5
164	DVSS	-6322.5	-340.5
165	DVSS	-6277.5	-340.5
166	DVSS	-6232.5	-340.5
167	DVSS	-6187.5	-340.5
168	DVSS	-6142.5	-340.5
169	DVSS	-6097.5	-340.5
170	DVSS	-6052.5	-340.5
171	VDDIB	-6007.5	-340.5
172	VDDIB	-5962.5	-340.5
173	VDDIB	-5917.5	-340.5
174	VDDIB	-5872.5	-340.5
175	VDDIB	-5827.5	-340.5
176	VDDIB	-5782.5	-340.5
177	VDDIB	-5737.5	-340.5
178	VDDIB	-5692.5	-340.5
179	VDDIB	-5647.5	-340.5
180	VDDIB	-5602.5	-340.5
181	VDDIB	-5557.5	-340.5
182	VDDIB	-5512.5	-340.5
183	VDDIB	-5467.5	-340.5
184	VDDIB	-5422.5	-340.5
185	VDDIB	-5377.5	-340.5
186	MVDDL	-5332.5	-340.5
187	MVDDL	-5287.5	-340.5
188	DUMMY	-5242.5	-340.5
189	DUMMY	-5197.5	-340.5
190	DUMMY	-5152.5	-340.5
191	DUMMY	-5107.5	-340.5
192	DUMMY	-5062.5	-340.5
193	DUMMY	-5017.5	-340.5
194	TESTN_L	-4972.5	-340.5
195	TESTN_L	-4927.5	-340.5
196	AVEEB	-4882.5	-340.5
197	AVEEB	-4837.5	-340.5
198	AVEEB	-4792.5	-340.5
199	AVEEB	-4747.5	-340.5
200	AVEEB	-4702.5	-340.5
201	DUMMY	-4657.5	-340.5
202	DUMMY	-4612.5	-340.5
203	DUMMY	-4567.5	-340.5
204	AVDDB	-4522.5	-340.5

No.	Name	X	Y
205	AVDDB	-4477.5	-340.5
206	AVDDB	-4432.5	-340.5
207	AVDDB	-4387.5	-340.5
208	AVDDB	-4342.5	-340.5
209	TESTP_L	-4297.5	-340.5
210	TESTP_L	-4252.5	-340.5
211	VSSR	-4207.5	-340.5
212	VSSR	-4162.5	-340.5
213	VSSR	-4117.5	-340.5
214	VSSR	-4072.5	-340.5
215	VSSR	-4027.5	-340.5
216	VSSR	-3982.5	-340.5
217	VSSR	-3937.5	-340.5
218	VSSR	-3892.5	-340.5
219	VSSR	-3847.5	-340.5
220	VSSR	-3802.5	-340.5
221	DUMMY	-3757.5	-340.5
222	DUMMY	-3712.5	-340.5
223	VDDIR	-3667.5	-340.5
224	VDDIR	-3622.5	-340.5
225	VDDIR	-3577.5	-340.5
226	VDDIR	-3532.5	-340.5
227	VDDIR	-3487.5	-340.5
228	VDDIR	-3442.5	-340.5
229	VSSB	-3397.5	-340.5
230	VSSB	-3352.5	-340.5
231	VSSB	-3307.5	-340.5
232	VSSB	-3262.5	-340.5
233	VSSB	-3217.5	-340.5
234	VSSB	-3172.5	-340.5
235	DUMMY	-3127.5	-340.5
236	DUMMY	-3082.5	-340.5
237	DUMMY	-3037.5	-340.5
238	DUMMY	-2992.5	-340.5
239	DUMMY	-2947.5	-340.5
240	DUMMY	-2902.5	-340.5
241	DUMMY	-2857.5	-340.5
242	DUMMY	-2812.5	-340.5
243	DUMMY	-2767.5	-340.5
244	DUMMY	-2722.5	-340.5
245	DUMMY	-2677.5	-340.5
246	DUMMY	-2632.5	-340.5
247	DUMMY	-2587.5	-340.5
248	DUMMY	-2542.5	-340.5
249	DUMMY	-2497.5	-340.5
250	DUMMY	-2452.5	-340.5
251	DUMMY	-2407.5	-340.5
252	DUMMY	-2362.5	-340.5
253	DUMMY	-2317.5	-340.5
254	DUMMY	-2272.5	-340.5
255	DUMMY	-2227.5	-340.5
256	DUMMY	-2182.5	-340.5
257	HS	-2137.5	-340.5
258	HS	-2092.5	-340.5
259	VS	-2047.5	-340.5
260	VS	-2002.5	-340.5
261	DUMMY	-1957.5	-340.5
262	DUMMY	-1912.5	-340.5
263	DUMMY	-1867.5	-340.5
264	DUMMY	-1822.5	-340.5
265	DUMMY	-1777.5	-340.5
266	DUMMY	-1732.5	-340.5
267	DUMMY	-1687.5	-340.5
268	DUMMY	-1642.5	-340.5
269	DUMMY	-1597.5	-340.5
270	DUMMY	-1552.5	-340.5
271	DUMMY	-1507.5	-340.5
272	DUMMY	-1462.5	-340.5

No.	Name	X	Y
273	DUMMY	-1417.5	-340.5
274	DUMMY	-1372.5	-340.5
275	LEDPWM	-1327.5	-340.5
276	LEDPWM	-1282.5	-340.5
277	LEDPWM	-1237.5	-340.5
278	LEDPWM	-1192.5	-340.5
279	TE	-1147.5	-340.5
280	TE	-1102.5	-340.5
281	TE	-1057.5	-340.5
282	TE	-1012.5	-340.5
283	TE	-967.5	-340.5
284	TE	-922.5	-340.5
285	TE1	-877.5	-340.5
286	TE1	-832.5	-340.5
287	TE1	-787.5	-340.5
288	TE1	-742.5	-340.5
289	TE1	-697.5	-340.5
290	TE1	-652.5	-340.5
291	RESX	-607.5	-340.5
292	RESX	-562.5	-340.5
293	RESX	-517.5	-340.5
294	RESX	-472.5	-340.5
295	DUMMY	-427.5	-340.5
296	DUMMY	-382.5	-340.5
297	DUMMY	-337.5	-340.5
298	DUMMY	-292.5	-340.5
299	OSC_TEST0	-247.5	-340.5
300	OSC_TEST0	-202.5	-340.5
301	OSC_TEST1	-157.5	-340.5
302	OSC_TEST1	-112.5	-340.5
303	IM[0]	-67.5	-340.5
304	IM[0]	-22.5	-340.5
305	VDDIB	22.5	-340.5
306	VDDIB	67.5	-340.5
307	IM[1]	112.5	-340.5
308	IM[1]	157.5	-340.5
309	IM[2]	202.5	-340.5
310	IM[2]	247.5	-340.5
311	RS[0]	292.5	-340.5
312	RS[0]	337.5	-340.5
313	VDDIB	382.5	-340.5
314	VDDIB	427.5	-340.5
315	RS[1]	472.5	-340.5
316	RS[1]	517.5	-340.5
317	VSSB	562.5	-340.5
318	VSSB	607.5	-340.5
319	LANSEL	652.5	-340.5
320	LANSEL	697.5	-340.5
321	VDDIB	742.5	-340.5
322	VDDIB	787.5	-340.5
323	BOOSTM[0]	832.5	-340.5
324	BOOSTM[0]	877.5	-340.5
325	DUMMY	922.5	-340.5
326	DUMMY	967.5	-340.5
327	BOOSTM[1]	1012.5	-340.5
328	BOOSTM[1]	1057.5	-340.5
329	VDDIB	1102.5	-340.5
330	VDDIB	1147.5	-340.5
331	VDDIB	1192.5	-340.5
332	VDDIB	1237.5	-340.5
333	VDDIB	1282.5	-340.5
334	VDDIB	1327.5	-340.5
335	VDDIB	1372.5	-340.5
336	VDDIB	1417.5	-340.5
337	VDDIB	1462.5	-340.5
338	VDDIB	1507.5	-340.5
339	VSSB	1552.5	-340.5
340	VSSB	1597.5	-340.5

No.	Name	X	Y
341	VSSB	1642.5	-340.5
342	VSSB	1687.5	-340.5
343	VSSB	1732.5	-340.5
344	VSSB	1777.5	-340.5
345	VSSB	1822.5	-340.5
346	VSSB	1867.5	-340.5
347	VSSB	1912.5	-340.5
348	VSSB	1957.5	-340.5
349	VSSB	2002.5	-340.5
350	VSSB	2047.5	-340.5
351	VSSB	2092.5	-340.5
352	VSSB	2137.5	-340.5
353	VSSB	2182.5	-340.5
354	VSSB	2227.5	-340.5
355	VSSB	2272.5	-340.5
356	VSSB	2317.5	-340.5
357	VSSB	2362.5	-340.5
358	VSSB	2407.5	-340.5
359	EXTN	2452.5	-340.5
360	EXTN	2497.5	-340.5
361	EXTN	2542.5	-340.5
362	EXTN	2587.5	-340.5
363	EXTN	2632.5	-340.5
364	EXTN	2677.5	-340.5
365	EXTN	2722.5	-340.5
366	EXTN	2767.5	-340.5
367	EXTP	2812.5	-340.5
368	EXTP	2857.5	-340.5
369	EXTP	2902.5	-340.5
370	EXTP	2947.5	-340.5
371	EXTP	2992.5	-340.5
372	EXTP	3037.5	-340.5
373	EXTP	3082.5	-340.5
374	EXTP	3127.5	-340.5
375	VCI	3172.5	-340.5
376	VCI	3217.5	-340.5
377	VCI	3262.5	-340.5
378	VCI	3307.5	-340.5
379	VCI	3352.5	-340.5
380	VCI	3397.5	-340.5
381	MTP_PWR	3442.5	-340.5
382	MTP_PWR	3487.5	-340.5
383	VSSB	3532.5	-340.5
384	VSSB	3577.5	-340.5
385	VSSB	3622.5	-340.5
386	VSSB	3667.5	-340.5
387	VSSB	3712.5	-340.5
388	VSSB	3757.5	-340.5
389	VSSB	3802.5	-340.5
390	VSSB	3847.5	-340.5
391	VSSB	3892.5	-340.5
392	VSSB	3937.5	-340.5
393	VSSB	3982.5	-340.5
394	VSSB	4027.5	-340.5
395	VSSB	4072.5	-340.5
396	VDDIB	4117.5	-340.5
397	VDDIB	4162.5	-340.5
398	VDDIB	4207.5	-340.5
399	VDDIB	4252.5	-340.5
400	VDDIB	4297.5	-340.5
401	VDDIB	4342.5	-340.5
402	VDDIB	4387.5	-340.5
403	VDDIB	4432.5	-340.5
404	VDDIB	4477.5	-340.5
405	VDDIB	4522.5	-340.5
406	VDDIB	4567.5	-340.5
407	TESTN_R	4612.5	-340.5
408	TESTN_R	4657.5	-340.5

No.	Name	X	Y
409	TESTN_R	4702.5	-340.5
410	VGMN	4747.5	-340.5
411	VGMN	4792.5	-340.5
412	VGMN	4837.5	-340.5
413	VGSN	4882.5	-340.5
414	VGSN	4927.5	-340.5
415	VGSN	4972.5	-340.5
416	VSSR	5017.5	-340.5
417	VSSR	5062.5	-340.5
418	VSSR	5107.5	-340.5
419	VSSR	5152.5	-340.5
420	VSSR	5197.5	-340.5
421	VGMP	5242.5	-340.5
422	VGMP	5287.5	-340.5
423	VGMP	5332.5	-340.5
424	VGMP	5377.5	-340.5
425	VGMP	5422.5	-340.5
426	VGMP	5467.5	-340.5
427	VGMP	5512.5	-340.5
428	VGMP	5557.5	-340.5
429	VSSB	5602.5	-340.5
430	VSSB	5647.5	-340.5
431	VSSB	5692.5	-340.5
432	VSSB	5737.5	-340.5
433	VSSB	5782.5	-340.5
434	DVSS	5827.5	-340.5
435	DVSS	5872.5	-340.5
436	DVSS	5917.5	-340.5
437	DVSS	5962.5	-340.5
438	DVSS	6007.5	-340.5
439	DVSS	6052.5	-340.5
440	DVSS	6097.5	-340.5
441	VDDIR	6142.5	-340.5
442	VDDIR	6187.5	-340.5
443	VDDIR	6232.5	-340.5
444	VDDIR	6277.5	-340.5
445	VDDIR	6322.5	-340.5
446	VDDIR	6367.5	-340.5
447	VDDIR	6412.5	-340.5
448	AVDDB	6457.5	-340.5
449	AVDDB	6502.5	-340.5
450	AVDDB	6547.5	-340.5
451	AVDDB	6592.5	-340.5
452	AVDDB	6637.5	-340.5
453	AVDDB	6682.5	-340.5
454	AVDDB	6727.5	-340.5
455	AVDDR	6772.5	-340.5
456	AVDDR	6817.5	-340.5
457	AVDDR	6862.5	-340.5
458	AVDDR	6907.5	-340.5
459	AVDDR	6952.5	-340.5
460	AVDDR	6997.5	-340.5
461	AVDDR	7042.5	-340.5
462	AVEEB	7087.5	-340.5
463	AVEEB	7132.5	-340.5
464	AVEEB	7177.5	-340.5
465	AVEEB	7222.5	-340.5
466	AVEEB	7267.5	-340.5
467	AVEEB	7312.5	-340.5
468	AVEEB	7357.5	-340.5
469	AVEER	7402.5	-340.5
470	AVEER	7447.5	-340.5
471	AVEER	7492.5	-340.5
472	AVEER	7537.5	-340.5
473	AVEER	7582.5	-340.5
474	AVEER	7627.5	-340.5
475	AVEER	7672.5	-340.5
476	VGSP	7717.5	-340.5
477	VGSP	7762.5	-340.5
478	VGSP	7807.5	-340.5
479	VGSP	7852.5	-340.5
480	VGSP	7897.5	-340.5
481	VGSP	7942.5	-340.5
482	VGSP	7987.5	-340.5
483	TESTP_R	8032.5	-340.5
484	TESTP_R	8077.5	-340.5
485	TESTP_R	8122.5	-340.5
486	TESTP_R	8167.5	-340.5
487	TESTP_R	8212.5	-340.5
488	TESTP_R	8257.5	-340.5
489	TESTP_R	8302.5	-340.5
490	DVDD	8347.5	-340.5
491	DVDD	8392.5	-340.5
492	DVDD	8437.5	-340.5
493	DVDD	8482.5	-340.5
494	DVDD	8527.5	-340.5
495	DVDD	8572.5	-340.5
496	DVDD	8617.5	-340.5
497	VDDGH	8662.5	-340.5
498	VDDGH	8707.5	-340.5
499	VDDGH	8752.5	-340.5
500	VDDGH	8797.5	-340.5
501	VDDGH	8842.5	-340.5
502	VDDGH	8887.5	-340.5
503	VDDGH	8932.5	-340.5
504	DUMMY	8977.5	-340.5
505	DUMMY	9022.5	-340.5
506	DUMMY	9067.5	-340.5
507	DUMMY	9112.5	-340.5
508	DUMMY	9157.5	-340.5
509	DUMMY	9202.5	-340.5
510	DUMMY	9247.5	-340.5
511	DUMMY	9292.5	-340.5
512	DUMMY	9337.5	-340.5
513	DUMMY	9382.5	-340.5
514	DUMMY	9427.5	-340.5
515	DUMMY	9472.5	-340.5
516	VSSB	9517.5	-340.5
517	VSSB	9562.5	-340.5
518	VSSB	9607.5	-340.5
519	VSSB	9652.5	-340.5
520	VSSB	9697.5	-340.5
521	VSSB	9742.5	-340.5
522	VSSB	9787.5	-340.5
523	VSSB	9832.5	-340.5
524	VGL	9877.5	-340.5
525	VGL	9922.5	-340.5
526	VGL	9967.5	-340.5
527	VGL	10012.5	-340.5
528	VGL	10057.5	-340.5
529	VGL	10102.5	-340.5
530	VGL	10147.5	-340.5
531	VGH	10192.5	-340.5
532	VGH	10237.5	-340.5
533	VGH	10282.5	-340.5
534	VGH	10327.5	-340.5
535	VGH	10372.5	-340.5
536	VGH	10417.5	-340.5
537	VGH	10462.5	-340.5
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1622	S<1414>	2480.5	336.5
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1640	S<1396>	2282.5	336.5
1641	S<1395>	2271.5	152.5
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1645	S<1391>	2227.5	244.5
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1649	S<1387>	2183.5	336.5
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1721	S<1315>	1391.5	336.5
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1840	DUMMY49	82.5	244.5
1841	DUMMY50	71.5	336.5
1842	DUMMY51	60.5	152.5
1843	DUMMY52	49.5	244.5
1844	DUMMY53	38.5	336.5
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2702	S<376>	-9399.5	336.5
2703	S<375>	-9410.5	152.5
2704	S<374>	-9421.5	244.5
2705	S<373>	-9432.5	336.5
2706	S<372>	-9443.5	152.5
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2708	S<370>	-9465.5	336.5
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2710	S<368>	-9487.5	244.5
2711	S<367>	-9498.5	336.5
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2713	S<365>	-9520.5	244.5
2714	S<364>	-9531.5	336.5
2715	S<363>	-9542.5	152.5
2716	S<362>	-9553.5	244.5
2717	S<361>	-9564.5	336.5
2718	S<360>	-9575.5	152.5
2719	S<359>	-9586.5	244.5
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2723	S<355>	-9630.5	336.5
2724	S<354>	-9641.5	152.5
2725	S<353>	-9652.5	244.5
2726	S<352>	-9663.5	336.5
2727	S<351>	-9674.5	152.5
2728	S<350>	-9685.5	244.5
2729	S<349>	-9696.5	336.5
2730	S<348>	-9707.5	152.5
2731	S<347>	-9718.5	244.5
2732	S<346>	-9729.5	336.5
2733	S<345>	-9740.5	152.5
2734	S<344>	-9751.5	244.5
2735	S<343>	-9762.5	336.5
2736	S<342>	-9773.5	152.5
2737	S<341>	-9784.5	244.5
2738	S<340>	-9795.5	336.5
2739	S<339>	-9806.5	152.5
2740	S<338>	-9817.5	244.5
2741	S<337>	-9828.5	336.5
2742	S<336>	-9839.5	152.5
2743	S<335>	-9850.5	244.5
2744	S<336.5>	-9861.5	336.5
2745	S<333>	-9872.5	152.5
2746	S<332>	-9883.5	244.5
2747	S<331>	-9894.5	336.5
2748	S<330>	-9905.5	152.5
2749	S<329>	-9916.5	244.5
2750	S<328>	-9927.5	336.5
2751	S<327>	-9938.5	152.5
2752	S<326>	-9949.5	244.5
2753	S<325>	-9960.5	336.5
2754	S<324>	-9971.5	152.5
2755	S<323>	-9982.5	244.5
2756	S<322>	-9993.5	336.5
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2759	S<319>	-10026.5	336.5
2760	S<318>	-10037.5	152.5
2761	S<317>	-10048.5	244.5
2762	S<316>	-10059.5	336.5
2763	S<315>	-10070.5	152.5
2764	S<314>	-10081.5	244.5
2765	S<313>	-10092.5	336.5
2766	S<312>	-10103.5	152.5
2767	S<311>	-10114.5	244.5
2768	S<310>	-10125.5	336.5
2769	S<309>	-10136.5	152.5
2770	S<308>	-10147.5	244.5
2771	S<307>	-10158.5	336.5
2772	S<306>	-10169.5	152.5
2773	S<305>	-10180.5	244.5
2774	S<304>	-10191.5	336.5
2775	S<303>	-10202.5	152.5
2776	S<302>	-10213.5	244.5
2777	S<301>	-10224.5	336.5
2778	S<300>	-10235.5	152.5
2779	S<299>	-10246.5	244.5
2780	S<298>	-10257.5	336.5
2781	S<297>	-10268.5	152.5
2782	S<296>	-10279.5	244.5
2783	S<295>	-10290.5	336.5
2784	S<294>	-10301.5	152.5
2785	S<293>	-10312.5	244.5
2786	S<292>	-10323.5	336.5
2787	S<291>	-10334.5	152.5
2788	S<290>	-10345.5	244.5

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2792	S<286>	-10389.5	336.5
2793	S<285>	-10400.5	152.5
2794	S<284>	-10411.5	244.5
2795	S<283>	-10422.5	336.5
2796	S<282>	-10433.5	152.5
2797	S<281>	-10444.5	244.5
2798	S<280>	-10455.5	336.5
2799	S<279>	-10466.5	152.5
2800	S<278>	-10477.5	244.5
2801	S<277>	-10488.5	336.5
2802	S<276>	-10499.5	152.5
2803	S<275>	-10510.5	244.5
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2806	S<272>	-10543.5	244.5
2807	S<271>	-10554.5	336.5
2808	S<270>	-10565.5	152.5
2809	S<269>	-10576.5	244.5
2810	S<268>	-10587.5	336.5
2811	S<267>	-10598.5	152.5
2812	S<266>	-10609.5	244.5
2813	S<265>	-10620.5	336.5
2814	S<264>	-10631.5	152.5
2815	S<263>	-10642.5	244.5
2816	S<262>	-10653.5	336.5
2817	S<261>	-10664.5	152.5
2818	S<260>	-10675.5	244.5
2819	S<259>	-10686.5	336.5
2820	S<258>	-10697.5	152.5
2821	S<257>	-10708.5	244.5
2822	S<256>	-10719.5	336.5
2823	S<255>	-10730.5	152.5
2824	S<254>	-10741.5	244.5
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2826	S<252>	-10763.5	152.5
2827	S<251>	-10774.5	244.5
2828	S<250>	-10785.5	336.5
2829	S<249>	-10796.5	152.5
2830	S<248>	-10807.5	244.5
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2832	S<246>	-10829.5	152.5
2833	S<245>	-10840.5	244.5
2834	S<244>	-10851.5	336.5
2835	S<243>	-10862.5	152.5
2836	S<244.5>	-10873.5	244.5
2837	S<241>	-10884.5	336.5
2838	S<240>	-10895.5	152.5
2839	S<239>	-10906.5	244.5
2840	S<238>	-10917.5	336.5
2841	S<237>	-10928.5	152.5
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2843	S<235>	-10950.5	336.5
2844	S<234>	-10961.5	152.5
2845	S<233>	-10972.5	244.5
2846	S<232>	-10983.5	336.5
2847	S<231>	-10994.5	152.5
2848	S<230>	-11005.5	244.5
2849	S<229>	-11016.5	336.5
2850	S<228>	-11027.5	152.5
2851	S<227>	-11038.5	244.5
2852	S<226>	-11049.5	336.5
2853	S<225>	-11060.5	152.5
2854	S<224>	-11071.5	244.5
2855	S<223>	-11082.5	336.5
2856	S<222>	-11093.5	152.5

No.	Name	X	Y
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2861	S<217>	-11148.5	336.5
2862	S<216>	-11159.5	152.5
2863	S<215>	-11170.5	244.5
2864	S<214>	-11181.5	336.5
2865	S<213>	-11192.5	152.5
2866	S<212>	-11203.5	244.5
2867	S<211>	-11214.5	336.5
2868	S<210>	-11225.5	152.5
2869	S<209>	-11236.5	244.5
2870	S<208>	-11247.5	336.5
2871	S<207>	-11258.5	152.5
2872	S<206>	-11269.5	244.5
2873	S<205>	-11280.5	336.5
2874	S<204>	-11291.5	152.5
2875	S<203>	-11302.5	244.5
2876	S<202>	-11313.5	336.5
2877	S<201>	-11324.5	152.5
2878	S<200>	-11335.5	244.5
2879	S<199>	-11346.5	336.5
2880	S<198>	-11357.5	152.5
2881	S<197>	-11368.5	244.5
2882	S<196>	-11379.5	336.5
2883	S<195>	-11390.5	152.5
2884	S<194>	-11401.5	244.5
2885	S<193>	-11412.5	336.5
2886	S<192>	-11423.5	152.5
2887	S<191>	-11434.5	244.5
2888	S<190>	-11445.5	336.5
2889	S<189>	-11456.5	152.5
2890	S<188>	-11467.5	244.5
2891	S<187>	-11478.5	336.5
2892	S<186>	-11489.5	152.5
2893	S<185>	-11500.5	244.5
2894	S<184>	-11511.5	336.5
2895	S<183>	-11522.5	152.5
2896	S<182>	-11533.5	244.5
2897	S<181>	-11544.5	336.5
2898	S<180>	-11555.5	152.5
2899	S<179>	-11566.5	244.5
2900	S<178>	-11577.5	336.5
2901	S<177>	-11588.5	152.5
2902	S<176>	-11599.5	244.5
2903	S<175>	-11610.5	336.5
2904	S<174>	-11621.5	152.5
2905	S<173>	-11632.5	244.5
2906	S<172>	-11643.5	336.5
2907	S<171>	-11654.5	152.5
2908	S<170>	-11665.5	244.5
2909	S<169>	-11676.5	336.5
2910	S<168>	-11687.5	152.5
2911	S<167>	-11698.5	244.5
2912	S<166>	-11709.5	336.5
2913	S<165>	-11720.5	152.5
2914	S<164>	-11731.5	244.5
2915	S<163>	-11742.5	336.5
2916	S<162>	-11753.5	152.5
2917	S<161>	-11764.5	244.5
2918	S<160>	-11775.5	336.5
2919	S<159>	-11786.5	152.5
2920	S<158>	-11797.5	244.5
2921	S<157>	-11808.5	336.5
2922	S<156>	-11819.5	152.5
2923	S<155>	-11830.5	244.5
2924	S<154>	-11841.5	336.5
2925	S<153>	-11852.5	152.5
2926	S<152>	-11863.5	244.5
2927	S<151>	-11874.5	336.5
2928	S<152.5>	-11885.5	152.5
2929	S<149>	-11896.5	244.5
2930	S<148>	-11907.5	336.5
2931	S<147>	-11918.5	152.5
2932	S<146>	-11929.5	244.5
2933	S<145>	-11940.5	336.5
2934	S<144>	-11951.5	152.5
2935	S<143>	-11962.5	244.5
2936	S<142>	-11973.5	336.5
2937	S<141>	-11984.5	152.5
2938	S<140>	-11995.5	244.5
2939	S<139>	-12006.5	336.5
2940	S<138>	-12017.5	152.5
2941	S<137>	-12028.5	244.5
2942	S<136>	-12039.5	336.5
2943	S<135>	-12050.5	152.5
2944	S<134>	-12061.5	244.5
2945	S<133>	-12072.5	336.5
2946	S<132>	-12083.5	152.5
2947	S<131>	-12094.5	244.5
2948	S<130>	-12105.5	336.5
2949	S<129>	-12116.5	152.5
2950	S<128>	-12127.5	244.5
2951	S<127>	-12138.5	336.5
2952	S<126>	-12149.5	152.5
2953	S<125>	-12160.5	244.5
2954	S<124>	-12171.5	336.5
2955	S<123>	-12182.5	152.5
2956	S<122>	-12193.5	244.5
2957	S<121>	-12204.5	336.5
2958	S<120>	-12215.5	152.5
2959	S<119>	-12226.5	244.5
2960	S<118>	-12237.5	336.5
2961	S<117>	-12248.5	152.5
2962	S<116>	-12259.5	244.5
2963	S<115>	-12270.5	336.5
2964	S<114>	-12281.5	152.5
2965	S<113>	-12292.5	244.5
2966	S<112>	-12303.5	336.5
2967	S<111>	-12314.5	152.5
2968	S<110>	-12325.5	244.5
2969	S<109>	-12336.5	336.5
2970	S<108>	-12347.5	152.5
2971	S<107>	-12358.5	244.5
2972	S<106>	-12369.5	336.5
2973	S<105>	-12380.5	152.5
2974	S<104>	-12391.5	244.5
2975	S<103>	-12402.5	336.5
2976	S<102>	-12413.5	152.5
2977	S<101>	-12424.5	244.5
2978	S<100>	-12435.5	336.5
2979	S<99>	-12446.5	152.5
2980	S<98>	-12457.5	244.5
2981	S<97>	-12468.5	336.5
2982	S<96>	-12479.5	152.5
2983	S<95>	-12490.5	244.5
2984	S<94>	-12501.5	336.5
2985	S<93>	-12512.5	152.5
2986	S<92>	-12523.5	244.5
2987	S<91>	-12534.5	336.5
2988	S<90>	-12545.5	152.5
2989	S<89>	-12556.5	244.5
2990	S<88>	-12567.5	336.5
2991	S<87>	-12578.5	152.5
2992	S<86>	-12589.5	244.5
2993	S<85>	-12600.5	336.5
2994	S<84>	-12611.5	152.5
2995	S<83>	-12622.5	244.5
2996	S<82>	-12633.5	336.5
2997	S<81>	-12644.5	152.5
2998	S<80>	-12655.5	244.5
2999	S<79>	-12666.5	336.5
3000	S<78>	-12677.5	152.5
3001	S<77>	-12688.5	244.5
3002	S<76>	-12699.5	336.5
3003	S<75>	-12710.5	152.5
3004	S<74>	-12721.5	244.5
3005	S<73>	-12732.5	336.5
3006	S<72>	-12743.5	152.5
3007	S<71>	-12754.5	244.5
3008	S<70>	-12765.5	336.5
3009	S<69>	-12776.5	152.5
3010	S<68>	-12787.5	244.5
3011	S<67>	-12798.5	336.5
3012	S<66>	-12809.5	152.5
3013	S<65>	-12820.5	244.5
3014	S<64>	-12831.5	336.5
3015	S<63>	-12842.5	152.5
3016	S<62>	-12853.5	244.5
3017	S<61>	-12864.5	336.5
3018	S<60>	-12875.5	152.5
3019	S<59>	-12886.5	244.5
3020	S<58>	-12897.5	336.5
3021	S<57>	-12908.5	152.5
3022	S<56>	-12919.5	244.5
3023	S<55>	-12930.5	336.5
3024	S<54>	-12941.5	152.5
3025	S<53>	-12952.5	244.5
3026	S<52>	-12963.5	336.5
3027	S<51>	-12974.5	152.5
3028	S<50>	-12985.5	244.5
3029	S<49>	-12996.5	336.5
3030	S<48>	-13007.5	152.5
3031	S<47>	-13018.5	244.5
3032	S<46>	-13029.5	336.5
3033	S<45>	-13040.5	152.5
3034	S<44>	-13051.5	244.5
3035	S<43>	-13062.5	336.5
3036	S<42>	-13073.5	152.5
3037	S<41>	-13084.5	244.5
3038	S<40>	-13095.5	336.5
3039	S<39>	-13106.5	152.5
3040	S<38>	-13117.5	244.5
3041	S<37>	-13128.5	336.5
3042	S<36>	-13139.5	152.5
3043	S<35>	-13150.5	244.5
3044	S<34>	-13161.5	336.5
3045	S<33>	-13172.5	152.5
3046	S<32>	-13183.5	244.5
3047	S<31>	-13194.5	336.5
3048	S<30>	-13205.5	152.5
3049	S<29>	-13216.5	244.5
3050	S<28>	-13227.5	336.5
3051	S<27>	-13238.5	152.5
3052	S<26>	-13249.5	244.5
3053	S<25>	-13260.5	336.5
3054	S<24>	-13271.5	152.5
3055	S<23>	-13282.5	244.5
3056	S<22>	-13293.5	336.5
3057	S<21>	-13304.5	152.5
3058	S<20>	-13315.5	244.5
3059	S<19>	-13326.5	336.5
3060	S<18>	-13337.5	152.5

No.	Name	X	Y
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3063	S<15>	-13370.5	152.5
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3066	S<12>	-13403.5	152.5
3067	S<11>	-13414.5	244.5
3068	S<10>	-13425.5	336.5
3069	S<9>	-13436.5	152.5
3070	S<8>	-13447.5	244.5
3071	S<7>	-13458.5	336.5
3072	S<6>	-13469.5	152.5
3073	S<5>	-13480.5	244.5
3074	S<4>	-13491.5	336.5
3075	S<3>	-13502.5	152.5
3076	S<2>	-13513.5	244.5
3077	S<1>	-13524.5	336.5
3078	S_LB	-13535.5	152.5
3079	DUMMY87	-13546.5	244.5
3080	DUMMY88	-13557.5	336.5
3081	DUMMY89	-13568.5	152.5
3082	DUMMY90	-13579.5	244.5
3083	DUMMY91	-13590.5	336.5
3084	DUMMY92	-13601.5	152.5
3085	DUMMY93	-13612.5	244.5
3086	DUMMY94	-13623.5	336.5
3087	Aligment mark L1	-13706	346
3088	Aligment mark L2	-13706	259
3089	Aligment mark R1	13706	346
3090	Aligment mark R2	13706	259

5. System Interface

5.1. Interface Type Selection

The selection of a given interfaces are done by setting LANSEL, IM2, IM1 ,IM0 pins and Page0_BA_bit0 as show in **Table 5.1.1**

Table 5.1.1 Interface Type Selection

External Pad Set				register	Configuration of				
LANSEL	**IM2**	**IM1**	**IM0**	**Page0_BA_bit0**	CLKP/N	D0P/N	D1P/N	D2P/N	D3P/N
0	0	0	0	1	CLKP/N	D3P/N	D2P/N	D1P/N	D0P/N
0	0	0	1	1	CLKN/P	D3N/P	D2N/P	D1N/P	D0N/P
0	0	1	0	1	CLKP/N	D0P/N	D1P/N	D2P/N	D3P/N
0	0	1	1	1	CLKN/P	D0N/P	D1N/P	D2N/P	D3N/P
0	1	0	0	1	CLKP/N	D3P/N	D0P/N	D1P/N	D2P/N
0	1	0	1	1	CLKN/P	D3N/P	D0N/P	D1N/P	D2N/P
0	1	1	0	1	CLKP/N	D2P/N	D1P/N	D0P/N	D3P/N
0	1	1	1	1	CLKN/P	D2N/P	D1N/P	D0N/P	D3N/P
0	0	0	0	0	CLKP/N		D2P/N	D1P/N	D0P/N
0	0	0	1	0	CLKN/P		D2N/P	D1N/P	D0N/P
0	0	1	0	0	CLKP/N	D0P/N	D1P/N	D2P/N	
0	0	1	1	0	CLKN/P	D0N/P	D1N/P	D2N/P	
0	1	0	0	0	CLKP/N		D0P/N	D1P/N	D2P/N
0	1	0	1	0	CLKN/P		D0N/P	D1N/P	D2N/P
0	1	1	0	0	CLKP/N	D2P/N	D1P/N	D0P/N	
0	1	1	1	0	CLKN/P	D2N/P	D1N/P	D0N/P	
1	0	0	0	0	CLKP/N			D1P/N	D0P/N
1	0	0	1	0	CLKN/P			D1N/P	D0N/P
1	0	1	0	0	CLKP/N	D0P/N	D1P/N		
1	0	1	1	0	CLKN/P	D0N/P	D1N/P		
1	1	0	0	0	CLKP/N		D0P/N	D1P/N	
1	1	0	1	0	CLKN/P		D0N/P	D1N/P	
1	1	1	0	0	CLKP/N		D1P/N	D0P/N	
1	1	1	1	0	CLKN/P		D1N/P	D0N/P	
Others					Reserved				

5.2. DSI system interface

5.2.1. General Description

The MIPI DSI is enabled or disabled by external IM[2:0] and LANSEL pin.

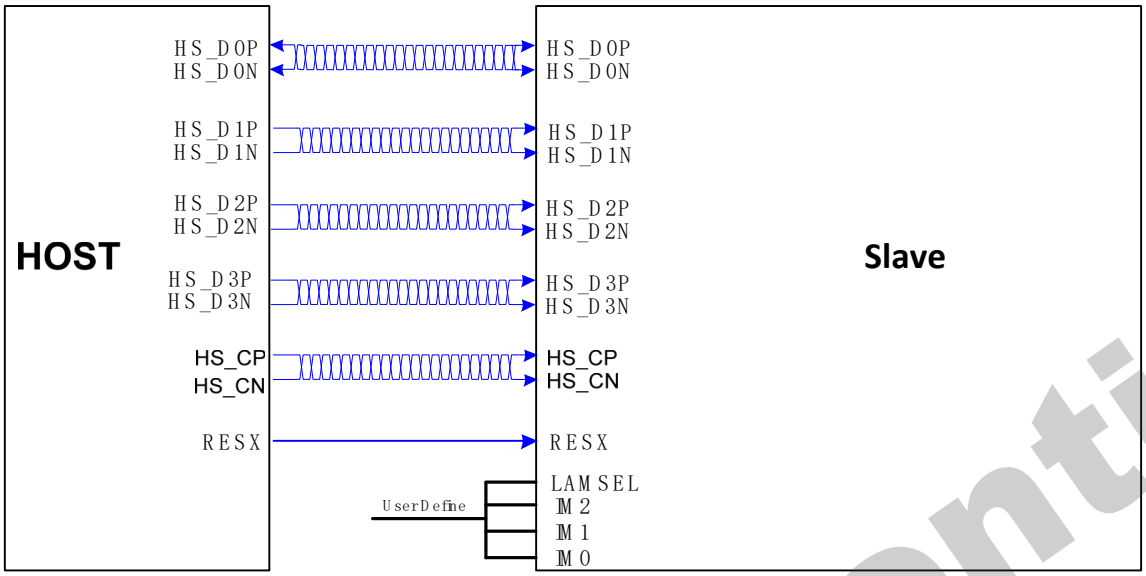


Figure 13 DSI system interface diagram

5.2.2. Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 10 High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage		High Speed	Low Power	
	DATA_P	DATA_N	Burst Mode	Control	Escape
HS-0	Low	High	Differential – 0	Note 1	Note 1
HS-1	High	Low	Differential – 1	Note 1	Note 1
LP-00	Low	Low	Not Defined	Bridge	Space
LP-01	Low	High	Not Defined	HS – Request	Mark - 0
LP-10	High	Low	Not Defined	LP - Request	Mark - 1
LP-11	High	High	Not Defined	Stop	Note 2

Note 1 *Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.*

Note 2 *If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.*

Note 3 *n = 0 and 1 (D1+/- lanes only for HS-0 and HS-1)*

5.2.3.DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

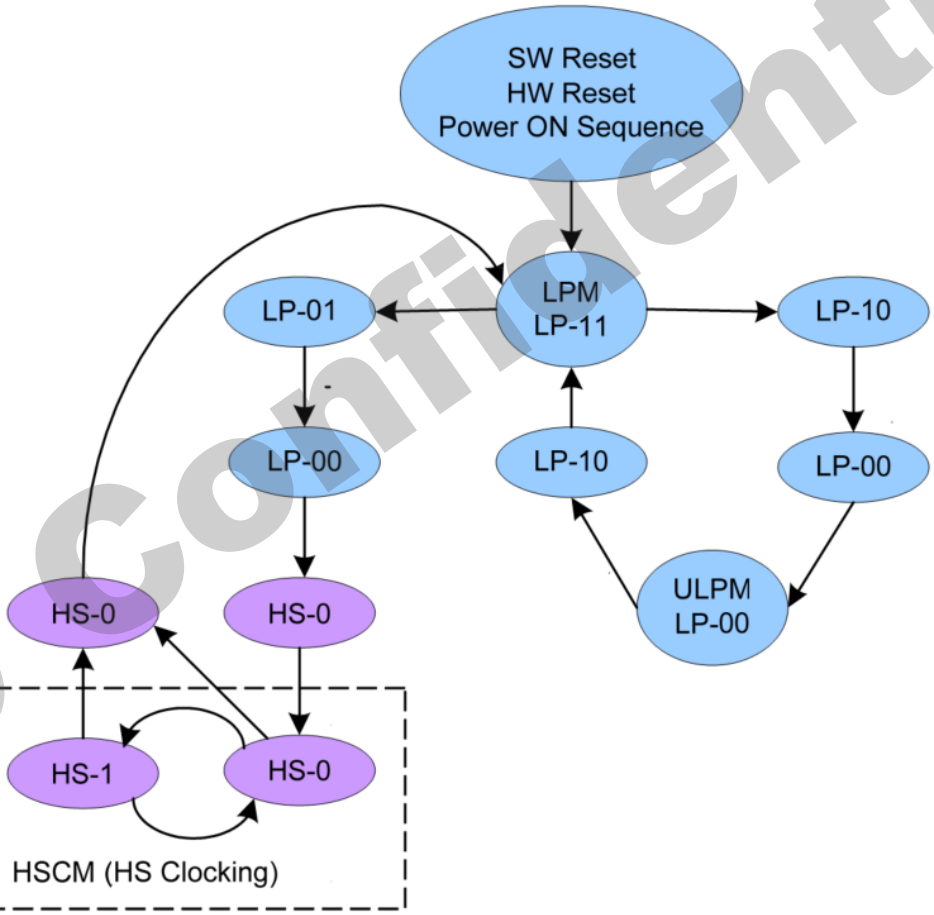


Figure 14 Clock Lanes Power Modes

5.2.4.Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

After SW Reset, HW Reset or Power On Sequence =>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM).

This sequence is illustrated below.

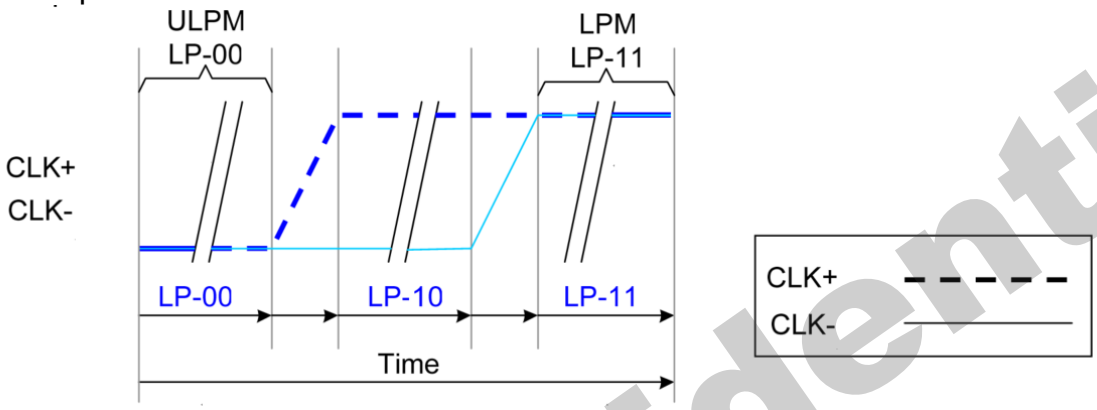


Figure 15 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.

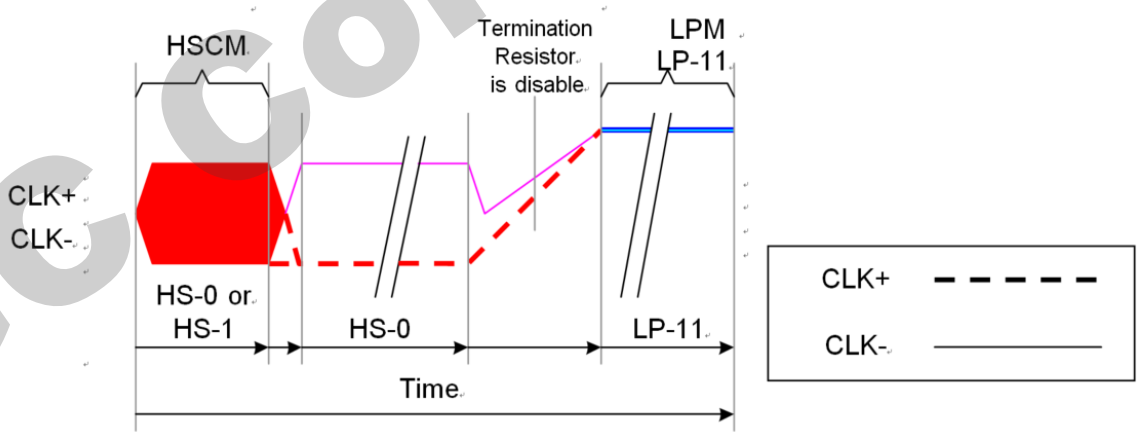


Figure 16 From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below

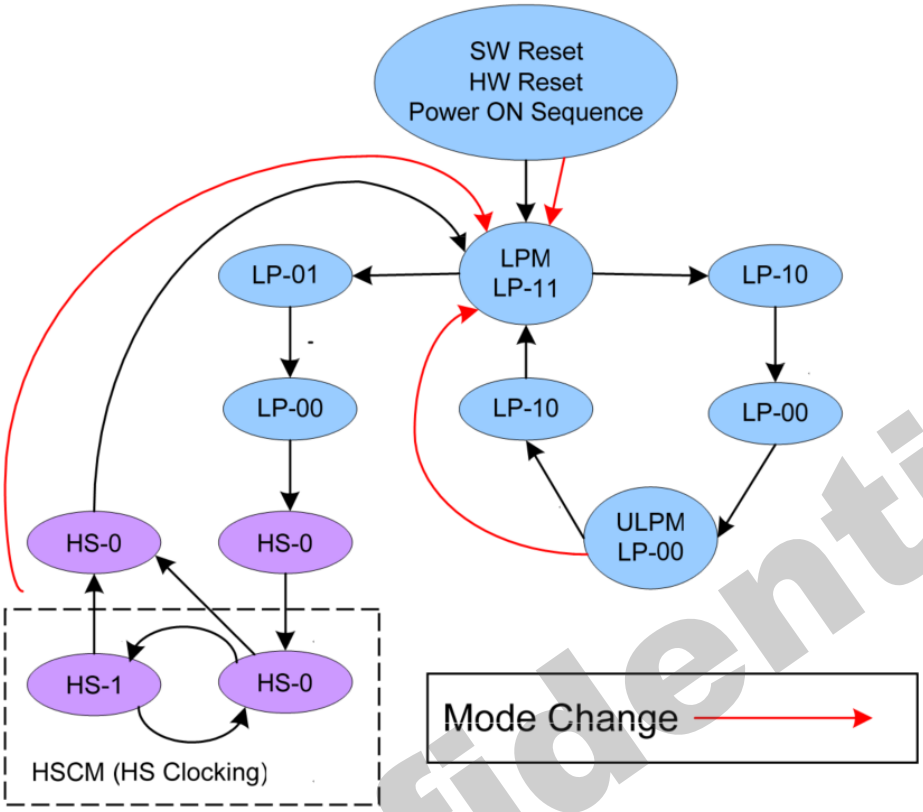


Figure 17 All Three Mode Changes to LPM on the Flow Chart

5.2.5. Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10

=>LP-00 (ULPM).

This sequence is illustrated below.

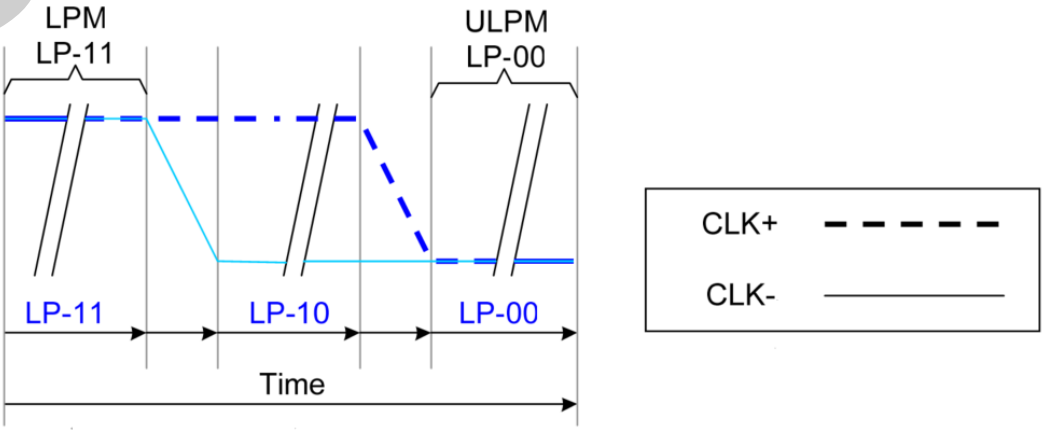


Figure 18 From LPM to ULPM

The mode change is also illustrated below.

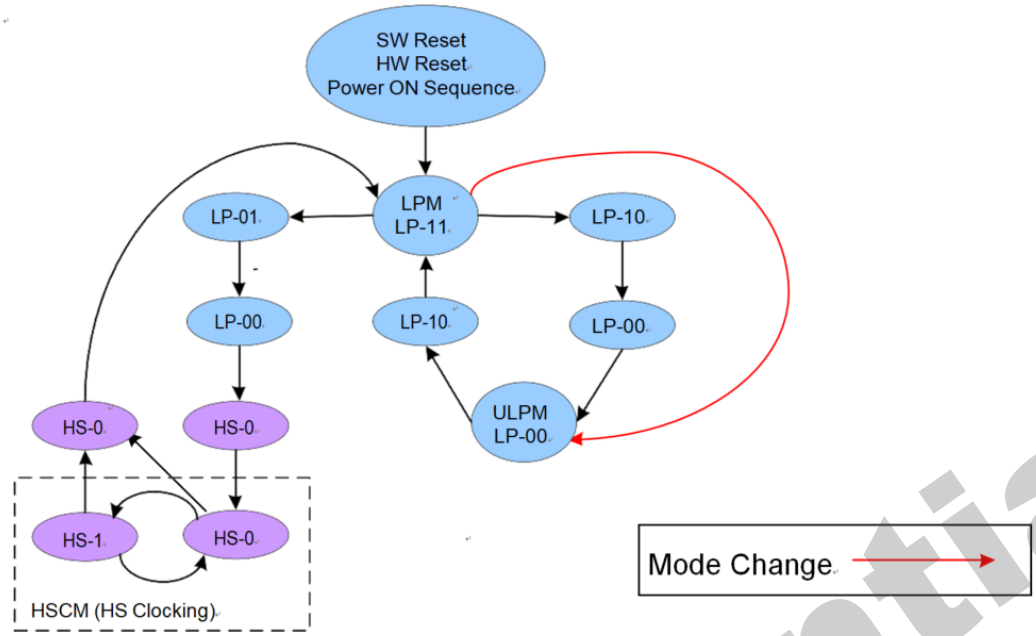


Figure 19 Mode Change from LPM to ULPM on the Flow Chart

5.2.6.High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00

=>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

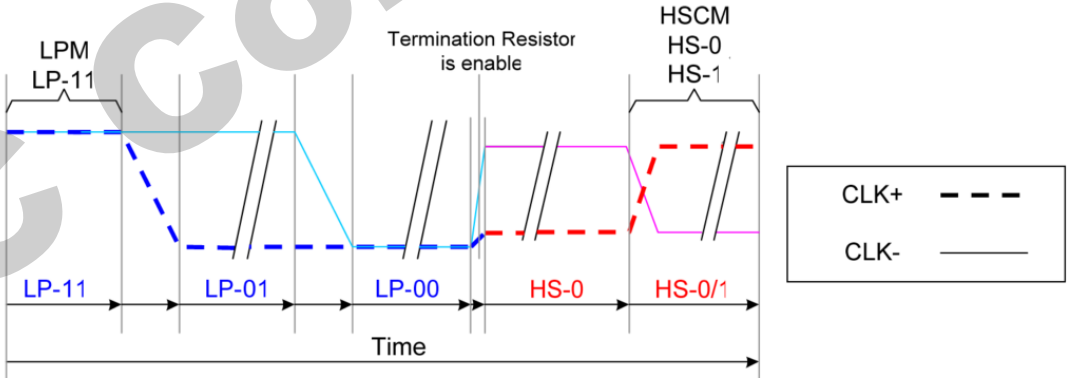


Figure 20 From LPM to HSCM

The mode change is also illustrated below.

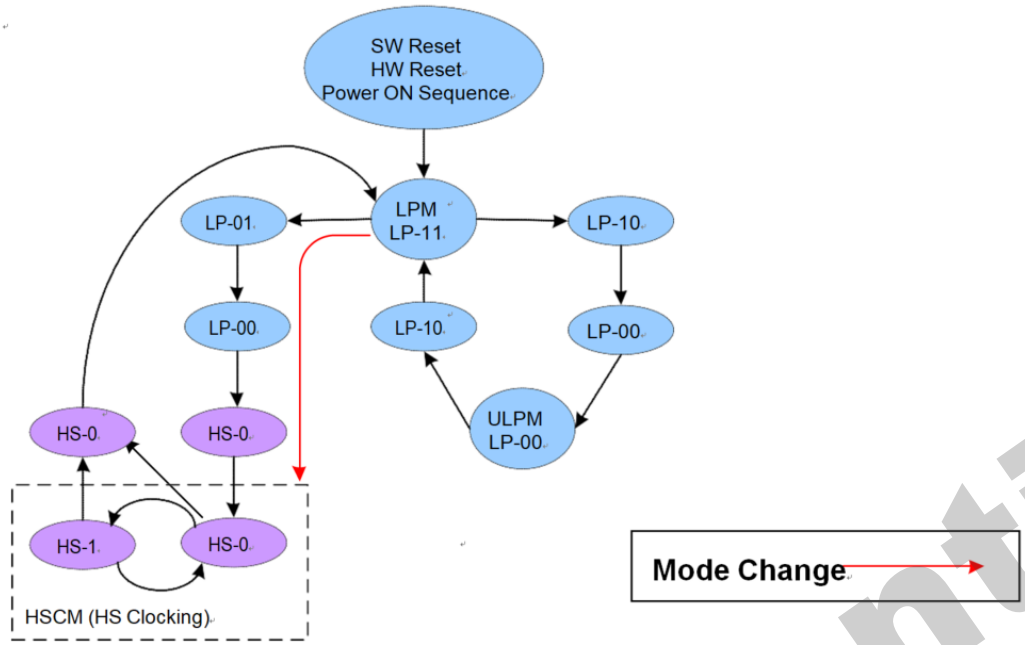


Figure 21 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

Even number of transitions

Start state is HS-0

End state is HS-0

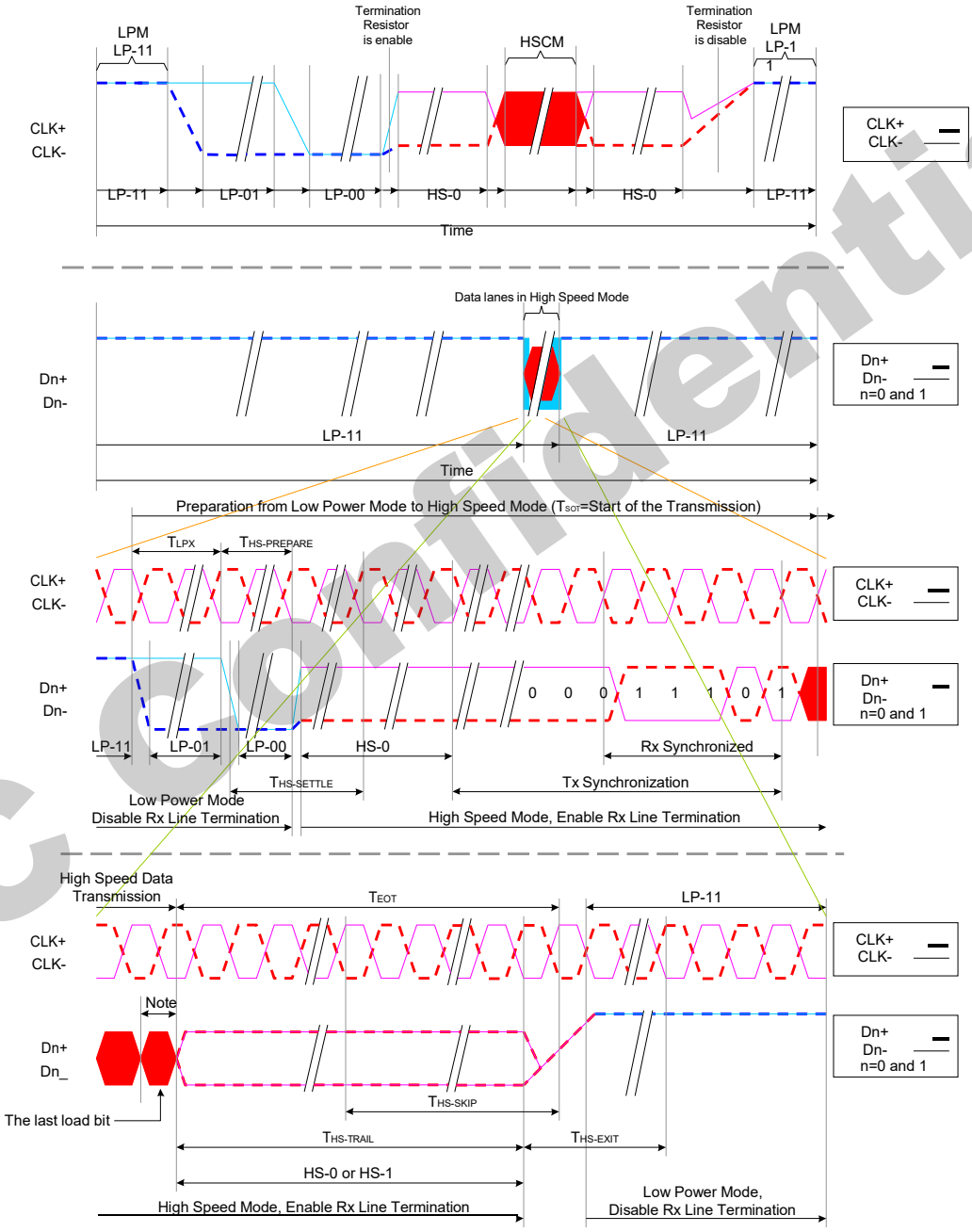


Figure 22 High Speed Clock Burst[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.2.7.DSI-D1 and DSI-D0 Data Lanes

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven in different modes which are:

Escape Mode (Only DSI-D0+/- data lanes are used)

High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 11 Entering and Leaving Sequences[Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 -+ LP-10 -+ LP-00 -+ LP-01 -+ LP-00	LP-00 -+ LP-10 -+ LP-11
High-Speed Data	LP-11 -+ LP-01 -+ LP-00 -+ HS-0	(HS-0 or HS-1) -+ LP-11
Bus Turnaround Request	LP-11 -+ LP-10 -+ LP-00 -+ LP-10 -+ LP-00	Hi-Z

Note 1. DSI-D1+/- and DSI-D0+/- data lanes are used.
2. More information on chapter “Bus Turnaround ”.

5.2.8. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

Send “Low-Power Data Transmission” (LPDT) e.g. from the MPU to the display module,

Drive data lanes to “Ultra-Low Power State” (ULPS),

Indicate “Remote Application Reset” (RAR), which is resetting the display module,

Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follow

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0-= 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

A load if it is needed

Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

End: LP-11

This basic construction is illustrated below:

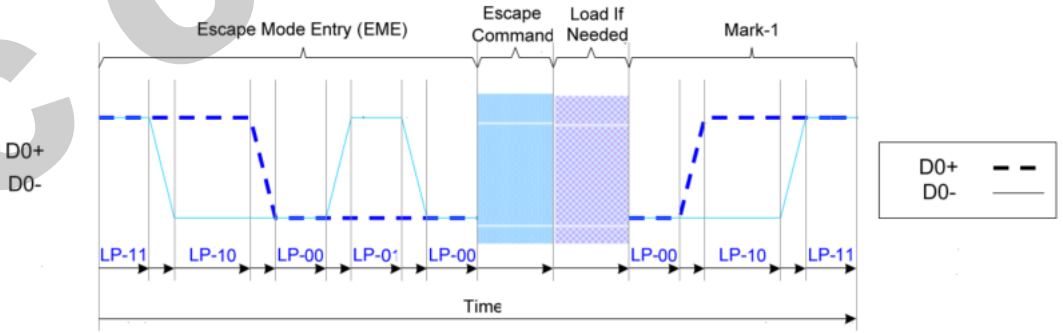


Figure 23 General Escape Mode Sequence

There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers, see Table 12: Escape Commands.

An example of a Mode type Escape Command is ‘Ultra-Low Power Mode’ where the MPU instructs the display module to enter it’s Ultra-Low Power Mode.

Escape commands are defined on the next table.

Table 12 Escape Commands[Note]

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Bit -+ Last Bit Transmitted)	Dn	
Low-Power Data	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, Note 1	Mo	1001 1111 b	-	-
Undefined-2, Note 1	Mo	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, Note 1	Trigger	1010 0000 b	-	-

Note 1. This Escape command support has not been implemented on the display module.
n = 1
x = Supported
- = Not Supported

5.2.9. Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MPU.

The Low Power Data Transmission (LPDT) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

Load (Data):

One or more bytes (8 bit)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

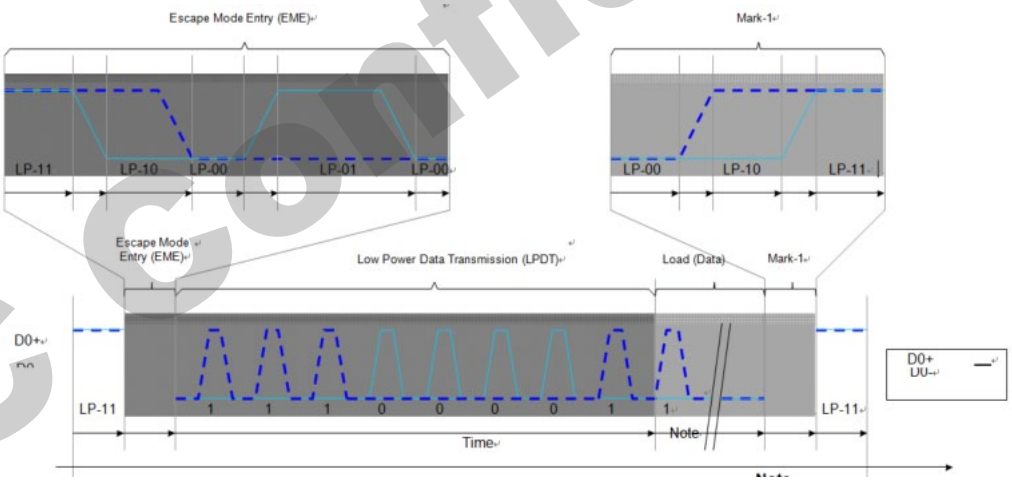


Figure 24 Low-Power Data Transmission (LPDT)[Note]

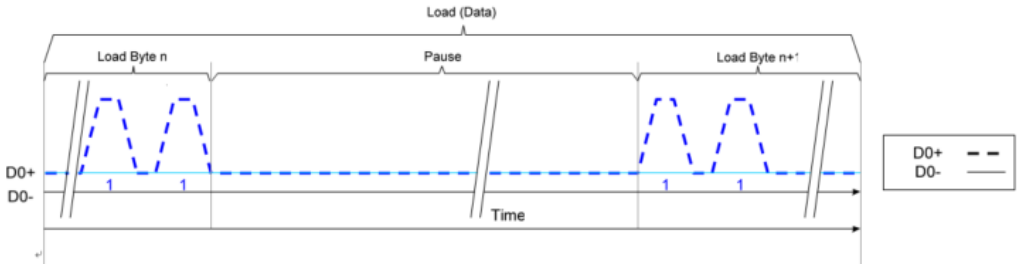


Figure 25 Pause (Example)

Note Load (Data) is presenting that the first bit is logical '1' in this example.

5.2.10. Ultra-Low Power State (ULPS)

The MPU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

Ultra-Low Power State (ULPS) when the MPU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

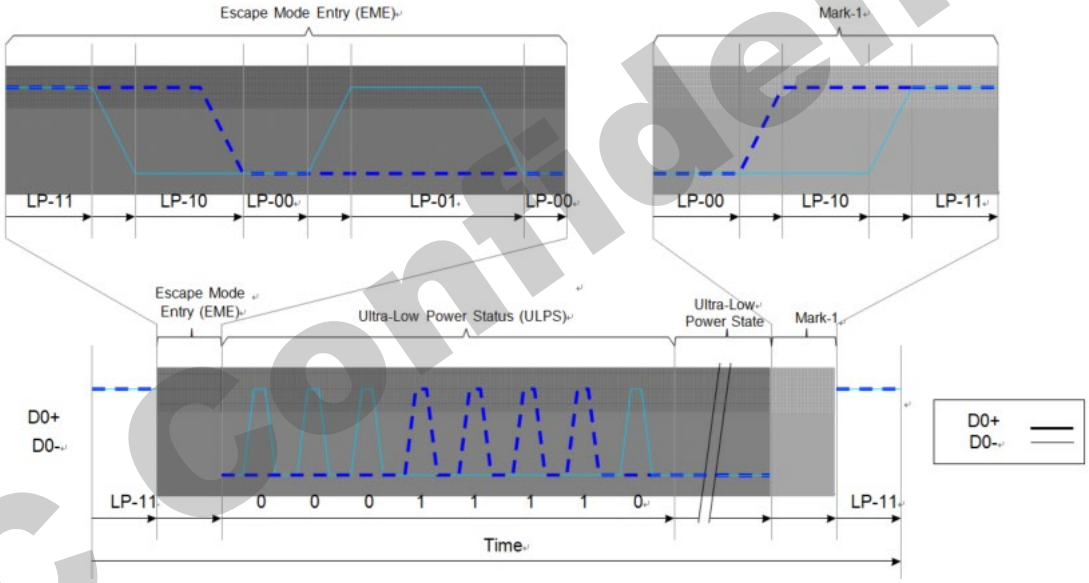


Figure 26 Ultra-Low Power State (ULPS)

5.2.11. Acknowledge (ACK)

The display module can inform to the MPU when an error has not recognized on it by Acknowledge (ACK). The display module is sending the Acknowledge (ACK) what is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

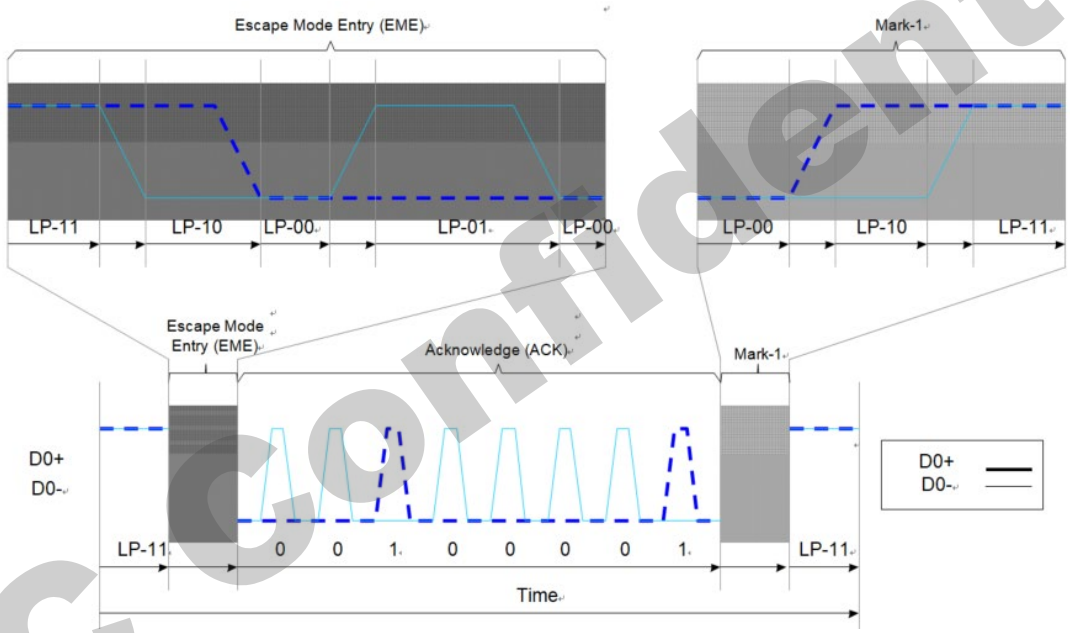


Figure 28 Acknowledge (ACK)

5.2.12. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MPU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

Start: LP-11

HS-Request: LP-01

HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)

End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

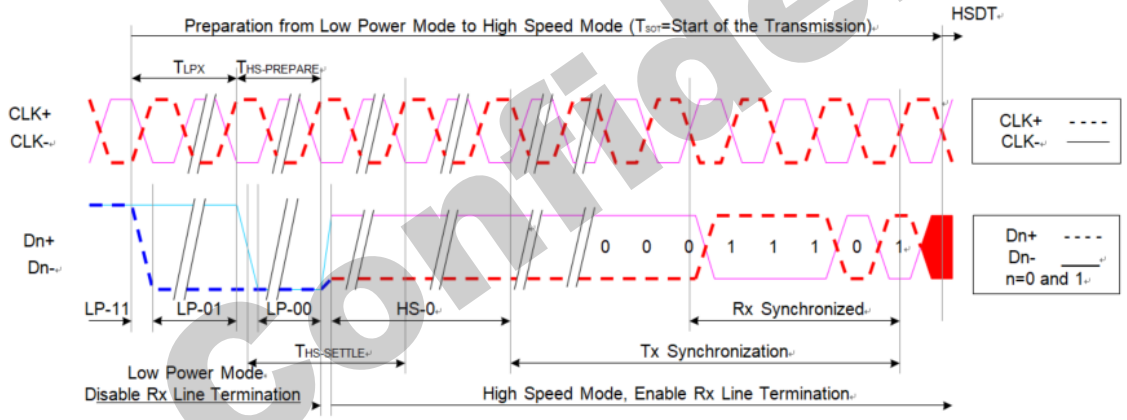


Figure 29 Entering High-Speed Data Transmission (T_{SOT} of HSDT)

5.2.13. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MPU and this HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

Start: High-Speed Data Transmission (HSDT)

Stops High-Speed Data Transmission

o MPU changes to HS-1, if the last load bit is HS-0 o MPU changes to HS-0, if the last load bit is HS-1

End: LP-11 (Rx: Lane Termination Disable)

his same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

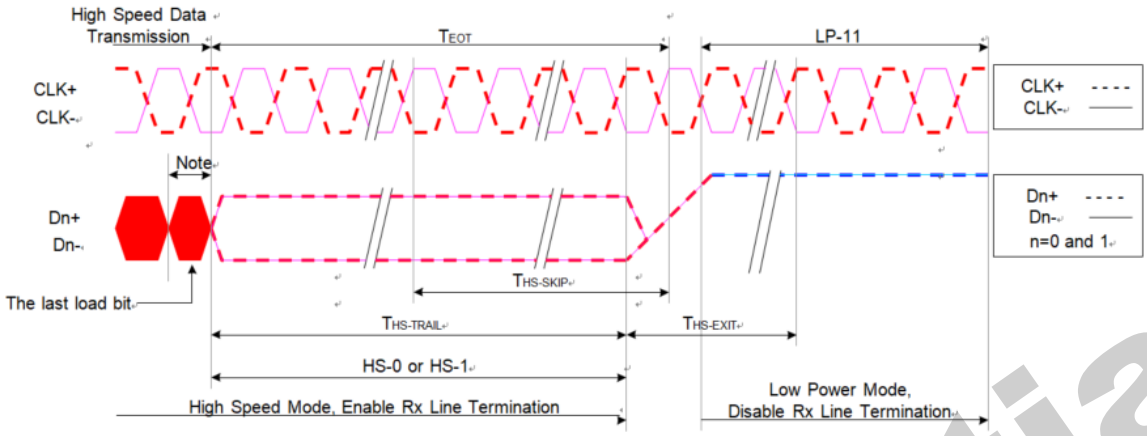


Figure 30 Leaving High-Speed Data Transmission (T_{EOT} of HSDT) Note

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.2.14. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

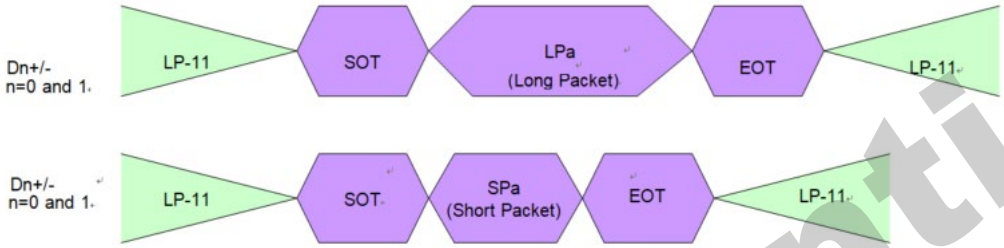


Figure 31 Single Packet in Low-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:

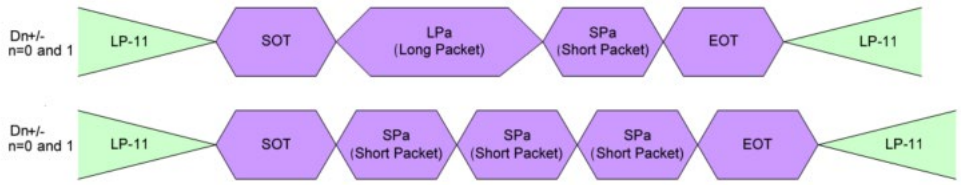


Figure 32 Multiple Packets in High-Speed Data Transmission – Examples

Table 13 Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

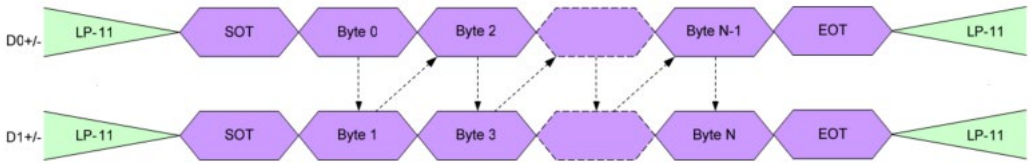


Figure 33 Single Packet in HSDT – Even Number of Bytes

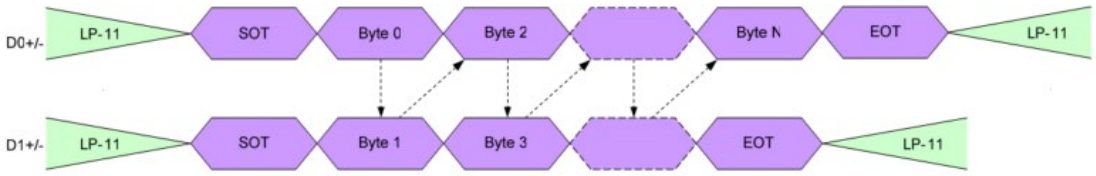


Figure 34 Single Packet in HSDT – Odd Number of Byte

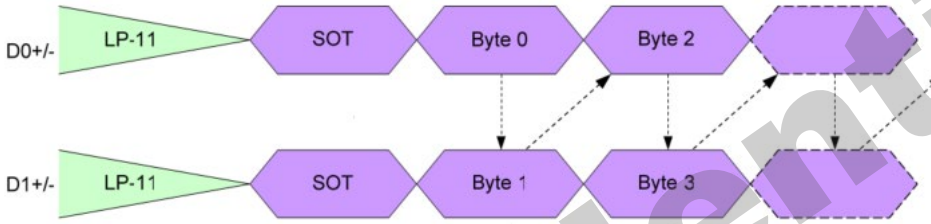


Figure 35 Start of Transmission (SoT) in HSDT for Multiple Packets

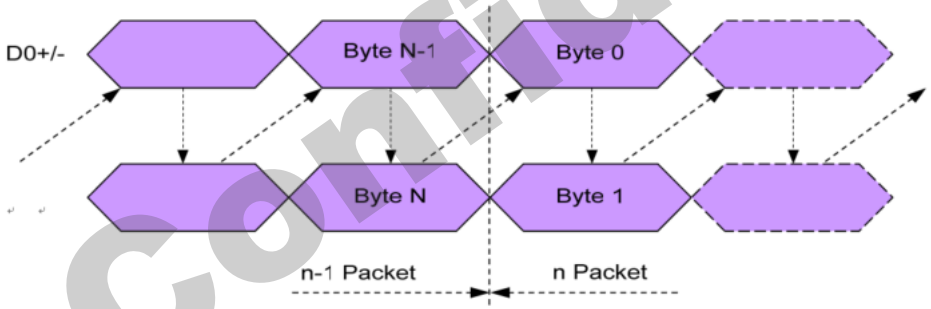


Figure 36 Continue Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

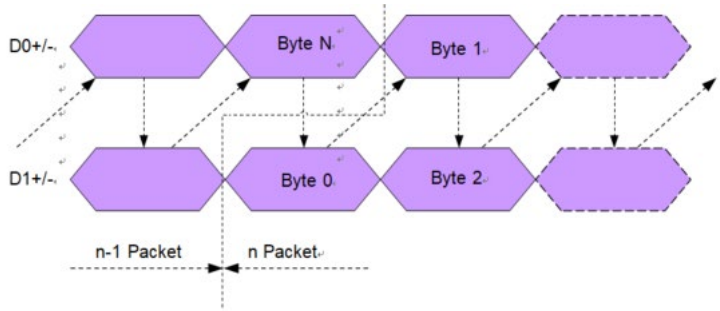


Figure 37 Continue Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

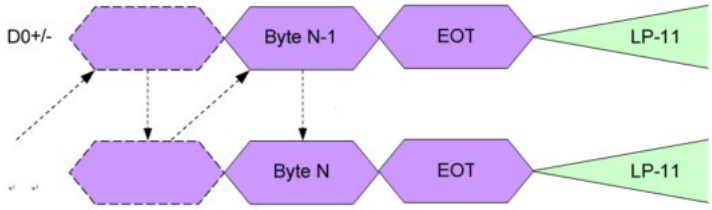


Figure 38 End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

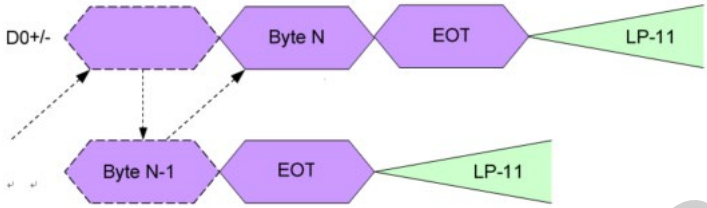


Figure 39 End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at cthe End of the Packet

5.2.15. Bus Turnaround (BTA)

The MPU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MPU or display module.

The MPU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MPU wants to do the bus turnaround procedure to the display module, as follows.

Start (MPU): LP-11

Turnaround Request (MPU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00

The MPU waits until the display module is starting to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)

The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MPU to the display module) is illustrated below

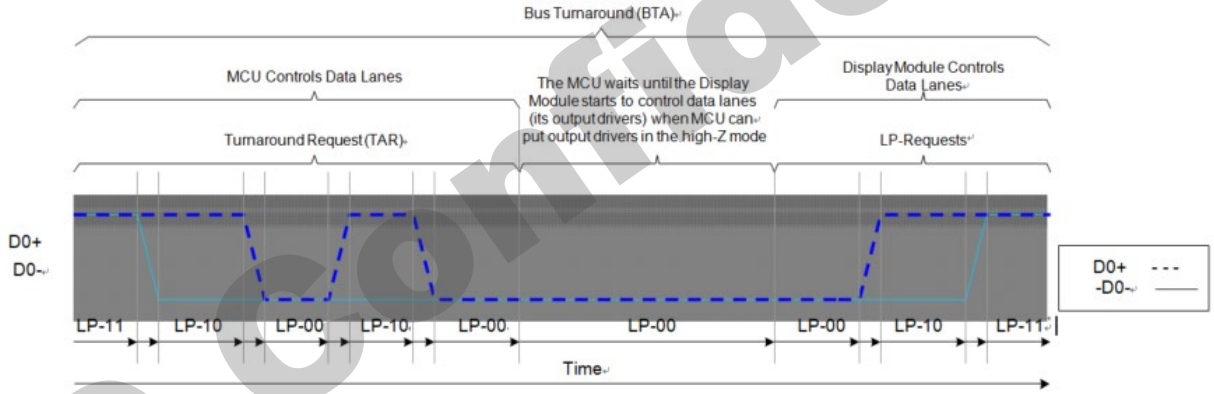


Figure 40 Bus Turnaround Procedure

MPU and display module terms are switched on the Figure 40, if the Bus Turnaround (BTA) is from the display module to the MPU.

5.2.16. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes[Note].The lengths of the packets are

Short Packet (SPa): 4 bytes

Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

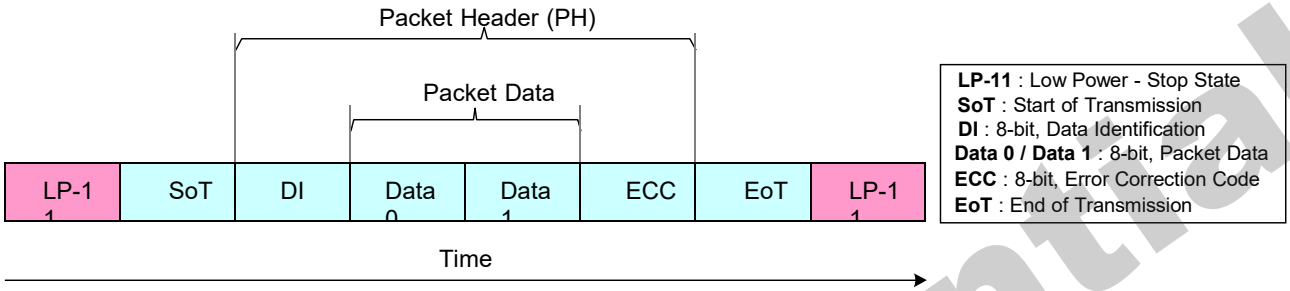


Figure 41 Short Packet (SPa) Structure

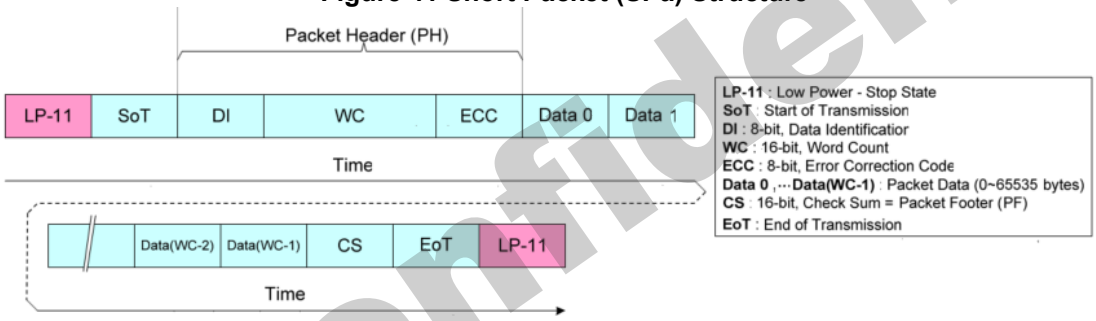


Figure 42 Long Packet (LPa) Structure

Note Short Packet (SPa) and Long Packet (LPa) are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.
LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.2.17. Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last. This same order is illustrated for reference purposes below.

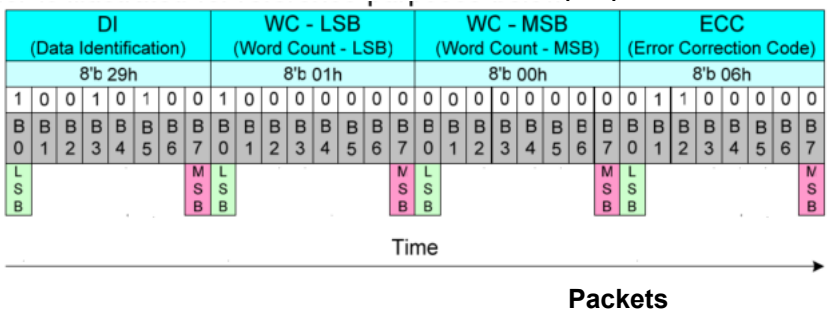


Figure 43 Bit Order of the Byte on Packets

5.2.18. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last

e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

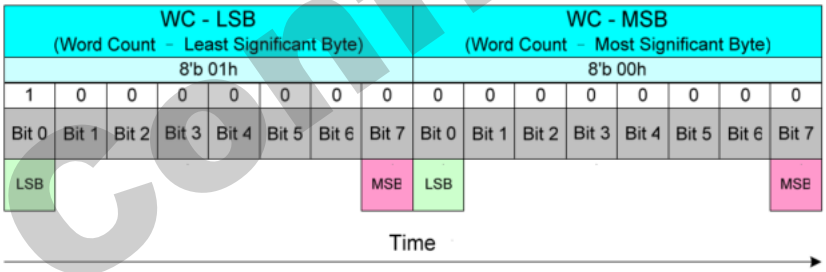


Figure 44 Byte Order of the Multiple Byte Information on Packets

5.2.19. Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

4th byte: Error Correction Code (ECC)

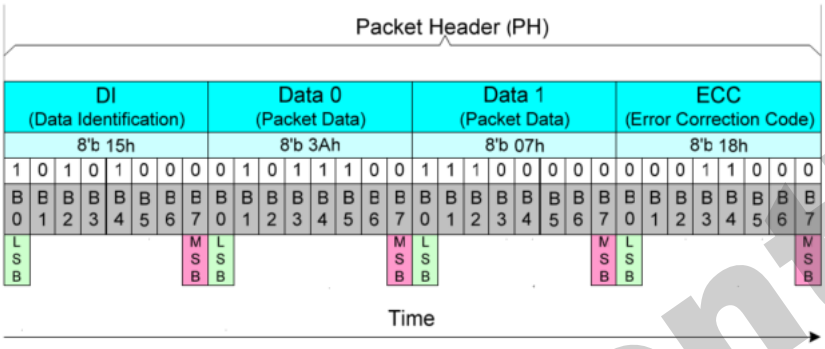


Figure 45 Packet Header (PH) on Short Packet (SPa)

Short Packet (LPa):

1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

2nd and 3rd bytes: Word Count (WC)

4th byte: Error Correction Code (ECC)

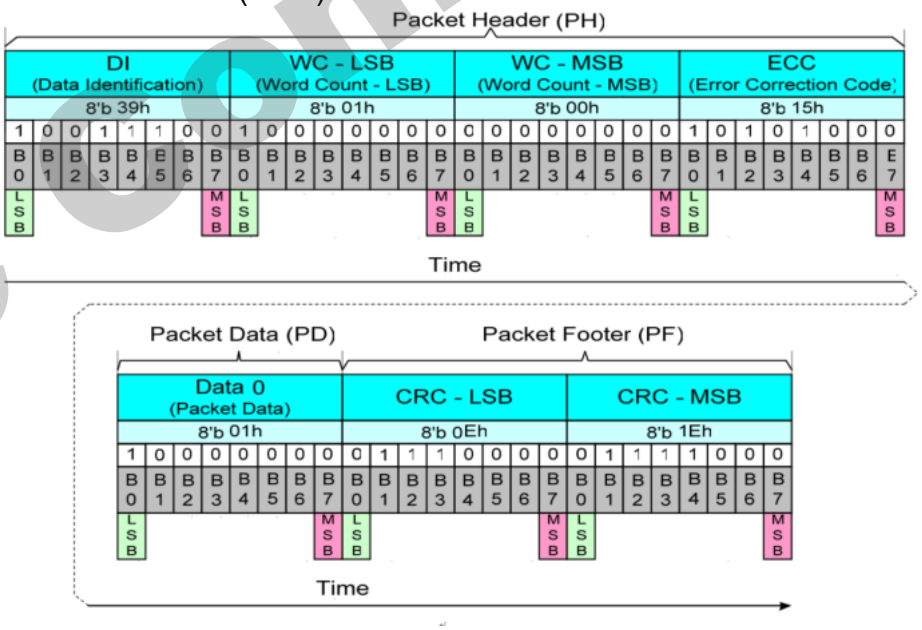


Figure 46 Packet Header (PH) on Long Packet (LPa)

5.2.20. Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

Virtual Channel (VC), 2 bits, DI[7...6]

Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated, see figure below.

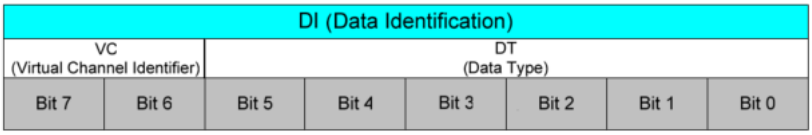


Figure 47 Data Identification (DI) Structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

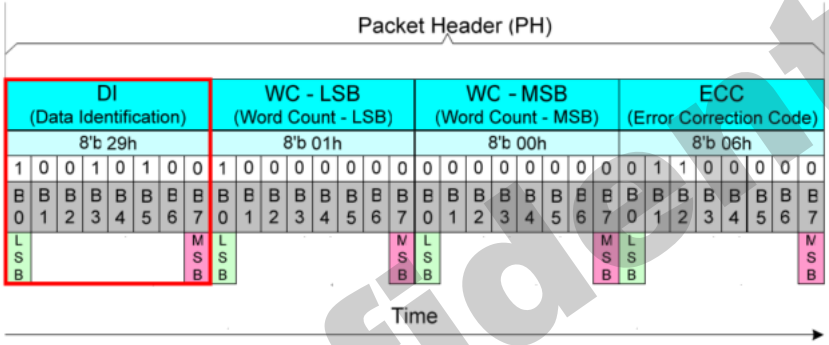


Figure 48 Data Identification (DI) on the Packet Header (PH)

5.2.21. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MPU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

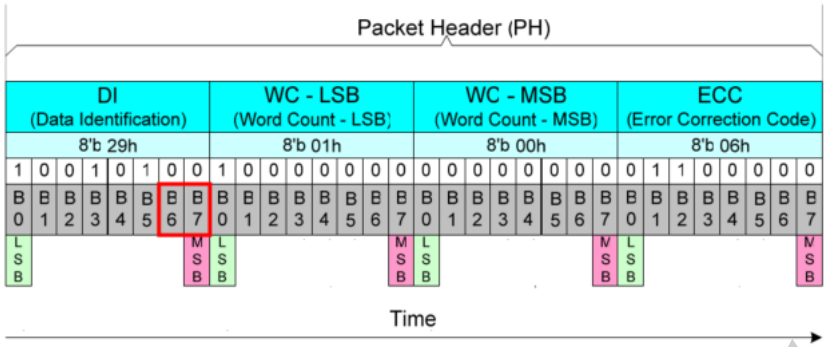


Figure 49 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MPU is using to send packets to them e.g.

The MPU is using the virtual channel 0 when it sends packets to this display module This display module is also using the virtual channel 0 when it sends packets to the MPU This functionality is illustrated below.

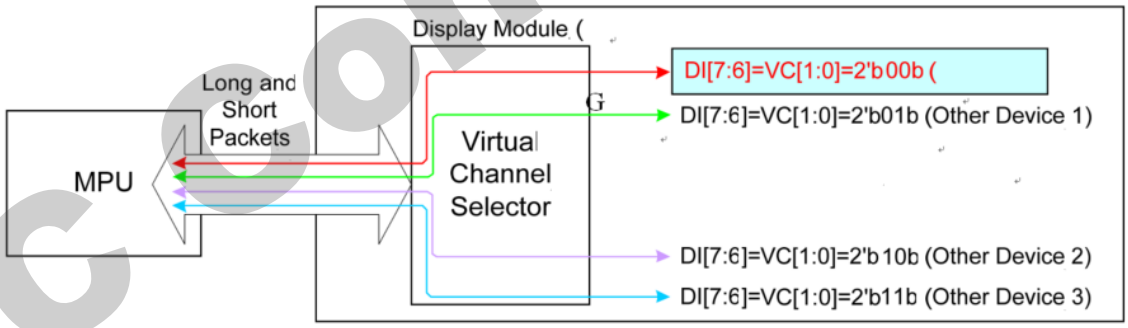


Figure 50 Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00_b) when the MPU is sending “End of Transmission Packet” to the display module. See chapter “End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for this display module.

5.2.22. Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

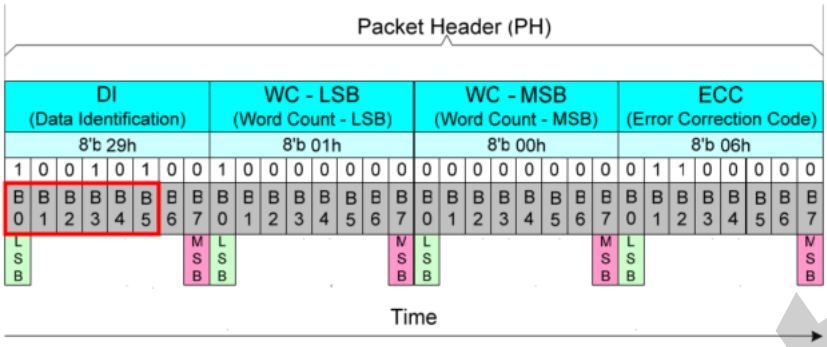


Figure 51 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MPU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

Table 14 Data Type (DT) from the MPU to the Display Module (GC9702C)

From the MPU to the Display Module (**GC9702C**)									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	He	Description	Short/Long	Abbreviati
0	0	1	0	0	0	08	End of Transmission Packet, Note 1	SPa (Short	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet	SPa (Short	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note 2	LPa (Long	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long	DCSW-L

Note 1 This can be used when the MPU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

Note 2 This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

Table 15 Data Type (DT) from the Display Module (GC9702C) to the MPU

From the Display Module (**GC9702C**) to the MPU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver is ignored other Data Type (DT) if they are not defined on tables: “ Table 14 Data Type (DT) from the MPU to the Display Module (or Other Devices)” or “ Table 15 Data Type (DT) from the Display Module (or Other Devices) to the MPU”.

5.2.23. Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

Data 1: 01hex (DCS's parameter)

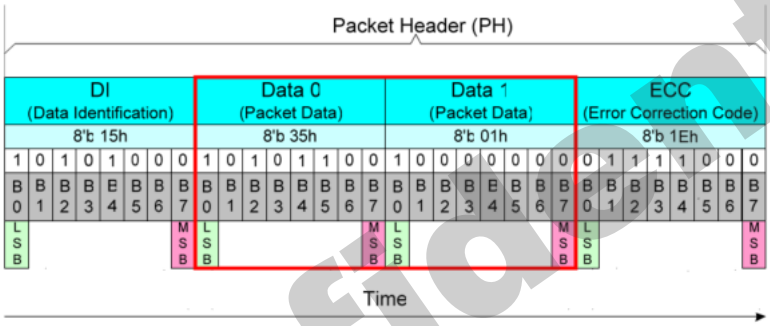


Figure 52 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

Data 1: 00hex (Null)

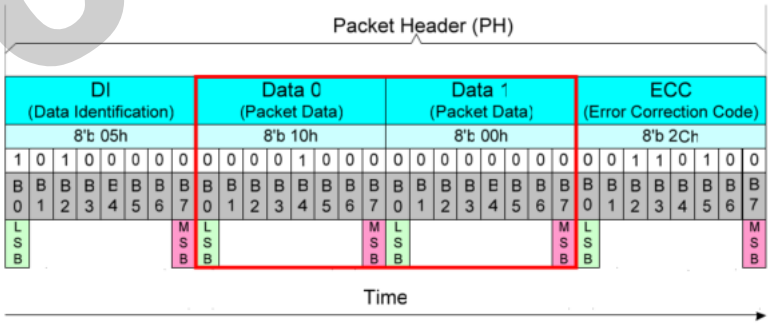


Figure 53 Packet Data (PD) for Short Packet (SPa), 1 Byte Information

5.2.24. Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

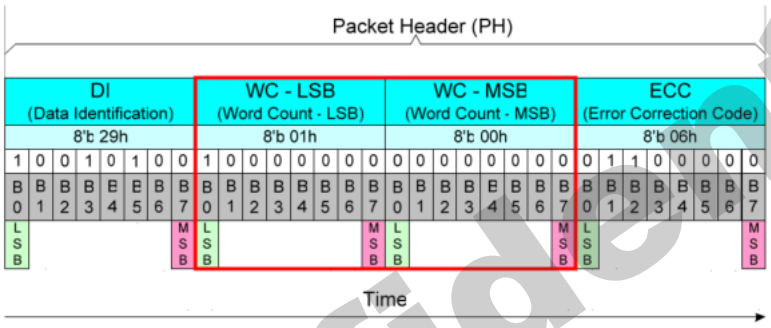


Figure 54 Word Count (WC) on the Long Packet (LPa)

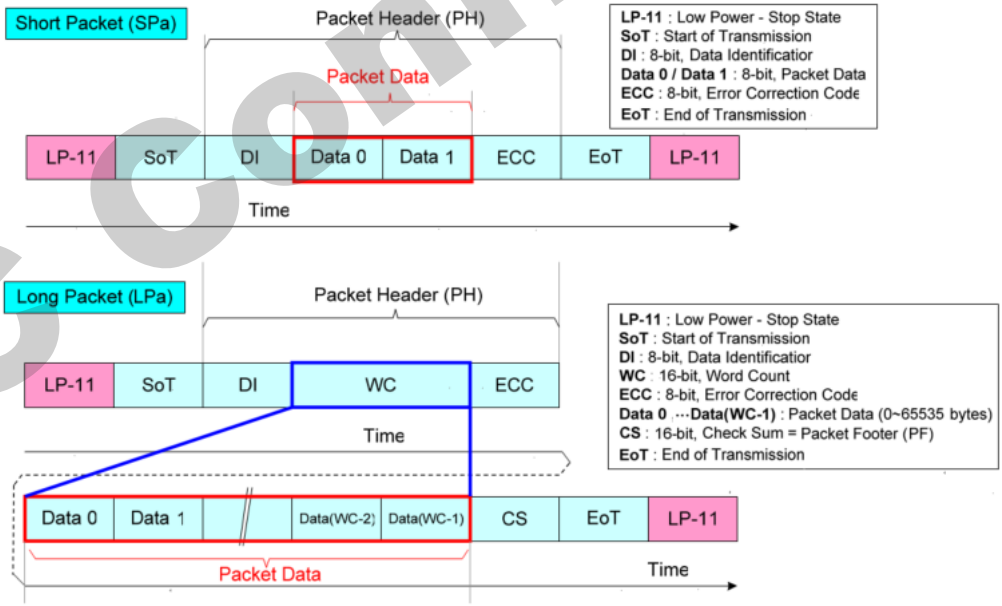


Figure 55 Packet Data in Short and Long Packets

5.2.25. Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0…7]), Packet Data (PD) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

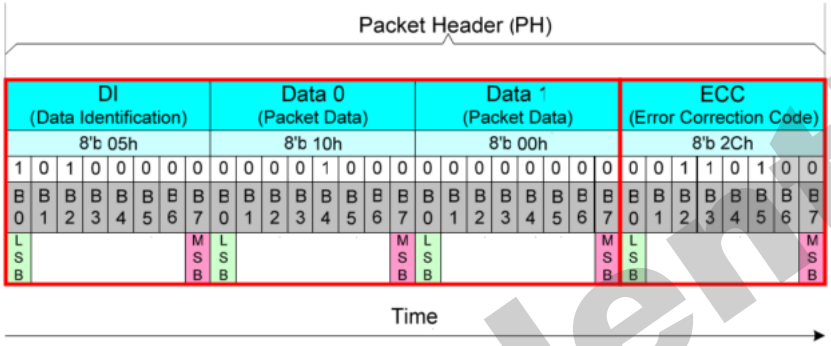


Figure 56 D[23…0] and P[7…0] on the Short Packet (SPa)

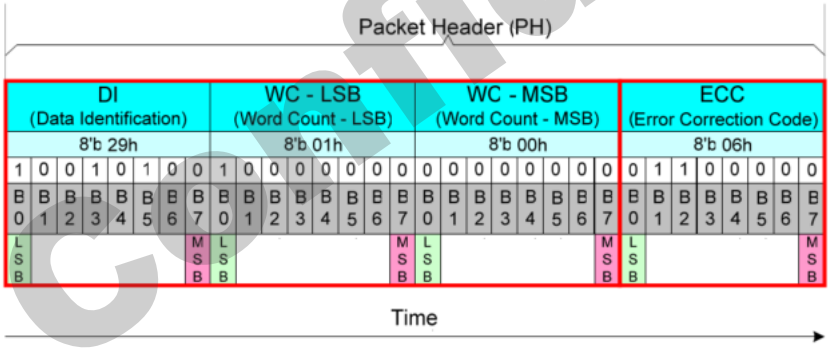


Figure 57 D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

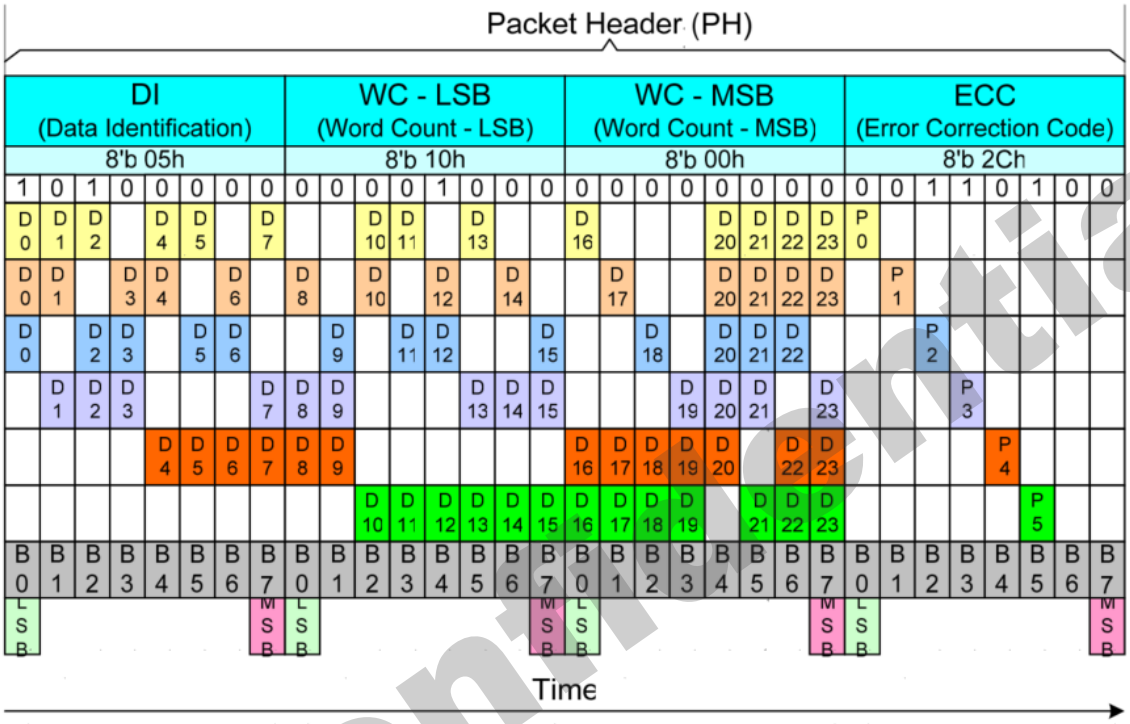


Figure 58 XOR Functionality on the Short Packet (SPa)

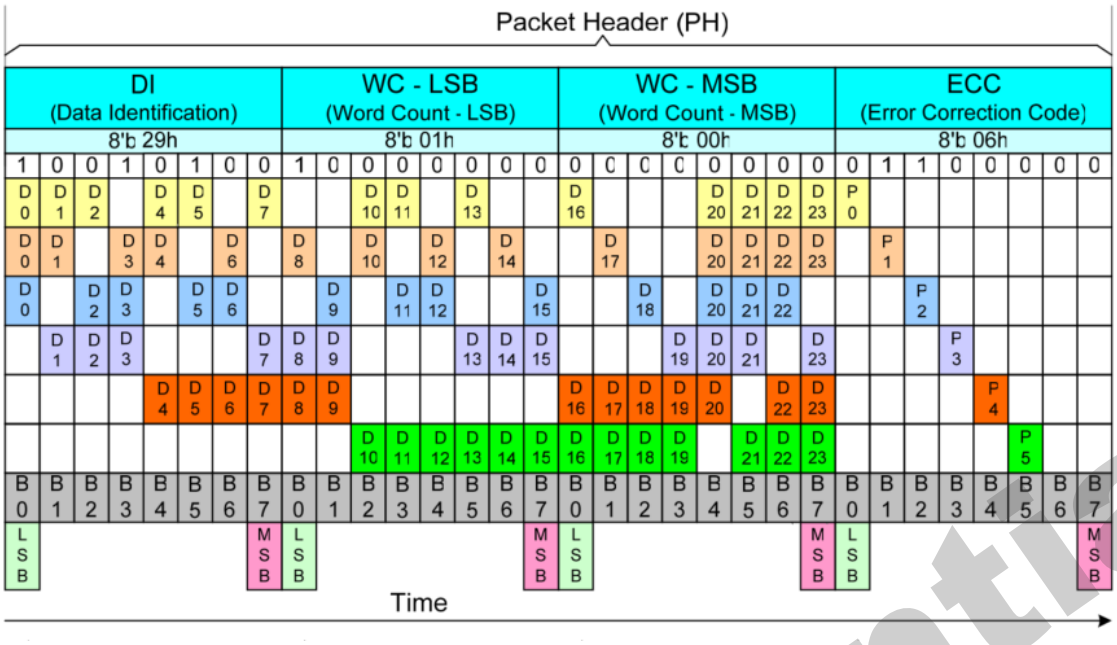


Figure 59 XOR Functionality on the Long Packet (LPa)

The transmitter (The MPU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MPU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MPU and the receiver is the display module, is illustrated for reference purposes below.

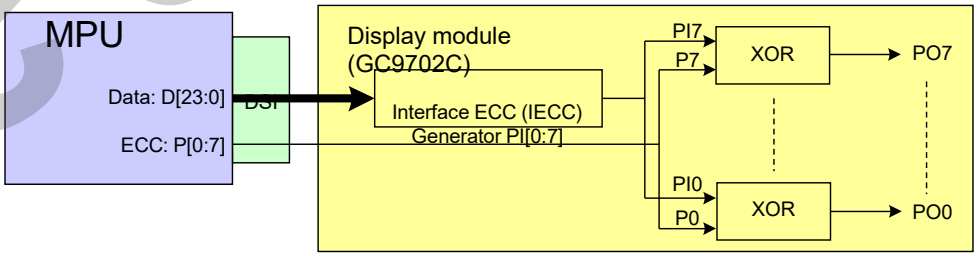


Figure 60 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 61 Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 62 Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Table 16 One Bit Error Value of the Error Correction Code (ECC)

Data	PO	PO	PO	PO	PO	PO	PO	PO	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on Table 25: One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on Table 25: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

5.2.26. Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

5.2.27. Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

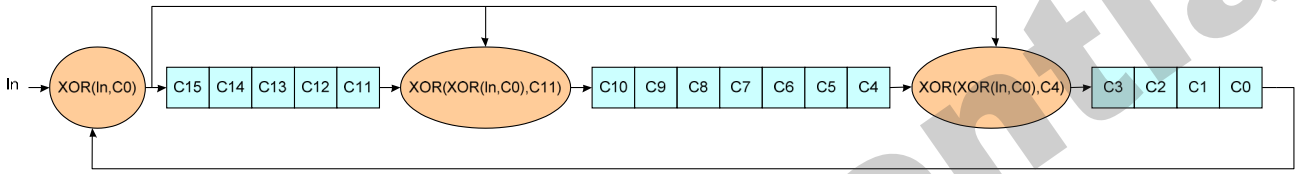
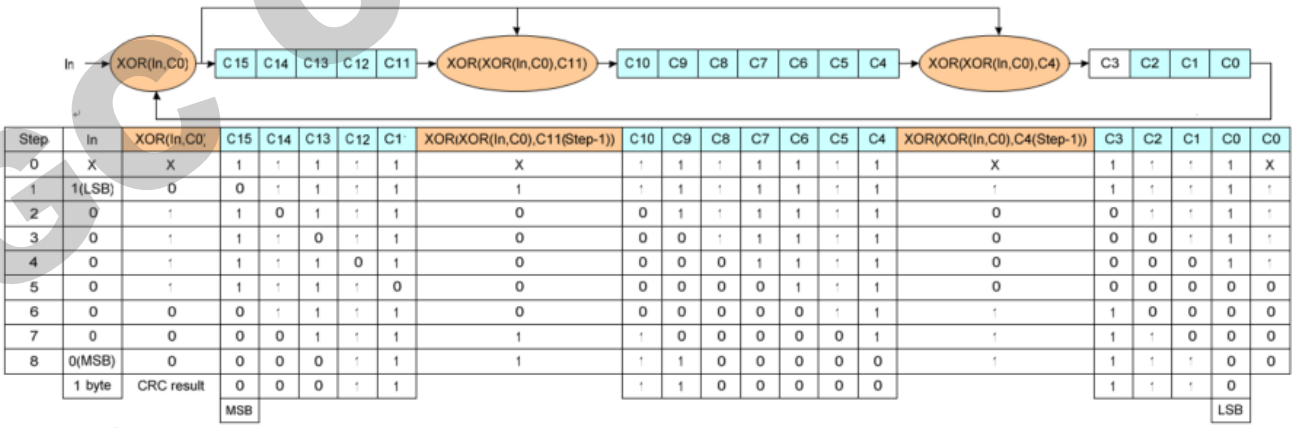


Figure 63 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	↑	1	↑	1	X	↑	1	↑	1	1	↑	1	X	1	↑	↑	1	X
1	1(LSB)	0	0	↑	1	↑	1	1	↑	1	↑	1	1	↑	1	↑	1	↑	↑	1	↑
2	0	↑	1	0	1	↑	1	0	0	1	↑	1	1	↑	1	0	0	↑	↑	1	↑
3	0	↑	1	↑	0	↑	1	0	0	0	↑	1	1	↑	1	0	0	0	↑	1	↑
4	0	↑	1	↑	1	0	1	0	0	0	0	1	1	↑	1	0	0	0	0	1	↑
5	0	↑	1	↑	1	↑	0	0	0	0	0	0	1	↑	1	0	0	0	0	0	0
6	0	0	0	↑	1	↑	1	0	0	0	0	0	0	↑	1	↑	1	0	0	0	0
7	0	0	0	0	1	↑	1	1	↑	0	0	0	0	0	1	↑	1	↑	0	0	0
8	0(MSB)	0	0	0	0	↑	1	1	↑	1	0	0	0	0	0	↑	1	↑	↑	0	0
	1 byte	CRC result	0	0	0	↑	1		↑	1	0	0	0	0	0		1	↑	↑	0	
			MSB																	LSB	

Figure 64 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

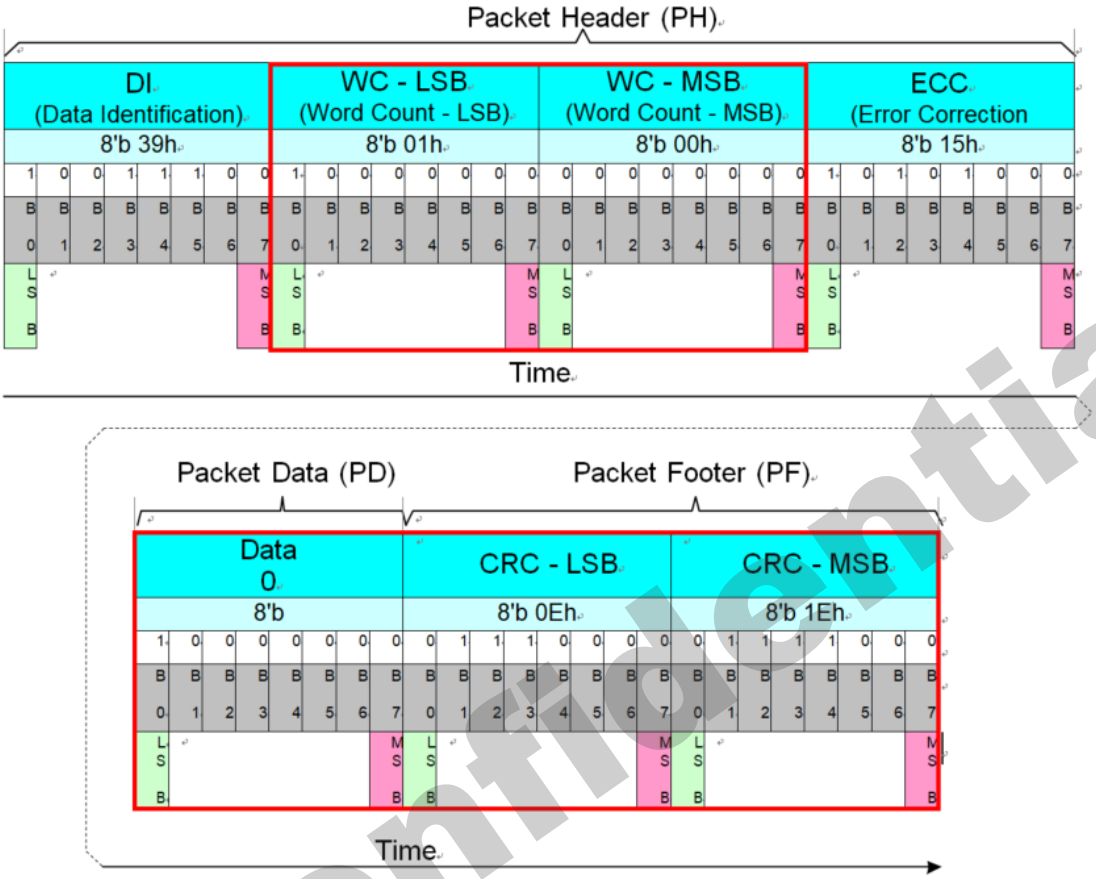


Figure 65 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.2.28. Packet Transmissions

5.2.28.1. Packet from the MPU to the Display Module

5.2.28.1.1. Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “5.2. Command Description” is used from the MPU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

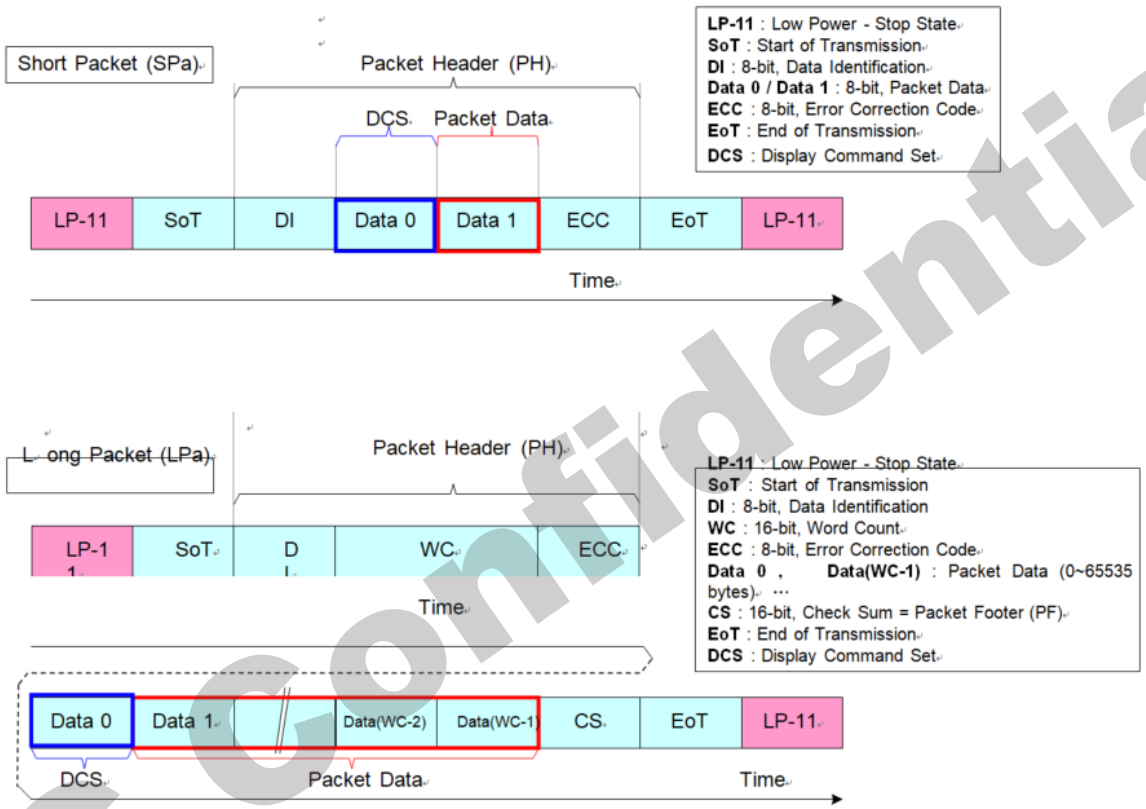


Figure 66 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

5.2.28.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MPU to the display module. These commands are defined on a table below. (See chapter "Command Description")

Table 17 Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Page 0 Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b o Data Type (DT, DI[5…0]): 00 0101b

Packet Data (PD)

o Data 0: "Sleep In (10h)", Display Command Set (DCS) o Data 1: Always 00hex

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

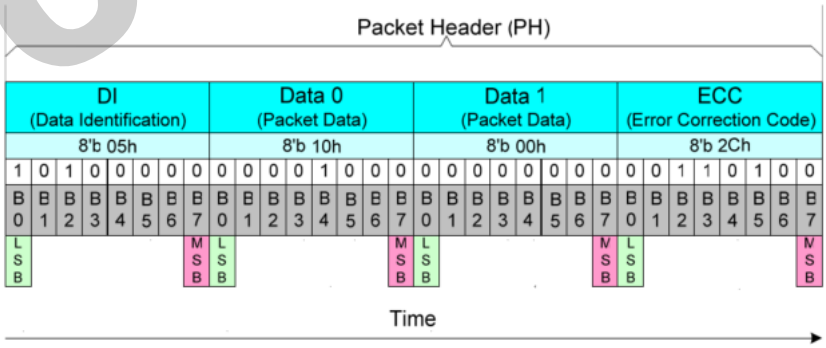


Figure 67 Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

5.2.28.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MPU to the display module. These commands are defined on a table (See chapter "Command Description") below.

Table 18 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Page 0 Command
Gamma Set (26h)
Interface Pixel Format (3Ah)
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control
Write CABC Minimum Brightness (5Eh)

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b o Data Type (DT, DI[5…0]): 01 0101b

Packet Data (PD)

o Data 0: "Gamma Set (26h)", Display Command Set (DCS) o Data 1: 01hex, Parameter of the DCS

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

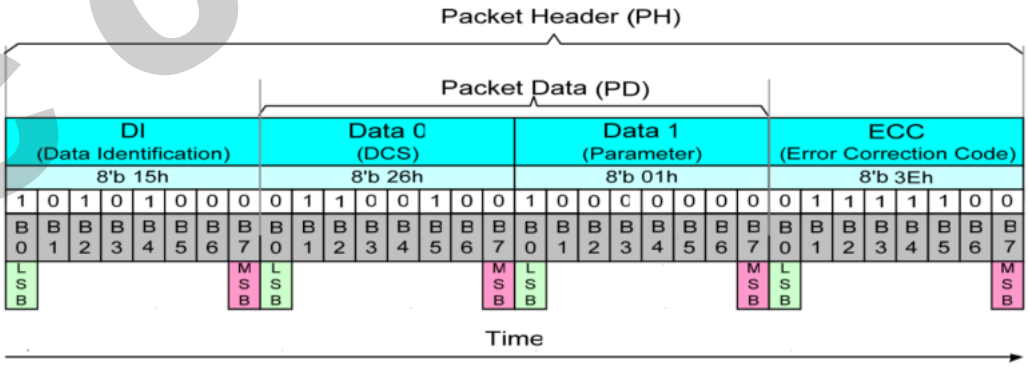


Figure 68 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

5.2.28.1.4. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MPU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "Command Description") below.

Table 19 Display Command Set (DCS) Write Long (DCSW-L)

Page 0 Command
NOP (00h) , Note 1
Software Reset (01h) , Note 1
Sleep In(10h) , Note 1
Sleep Out (11h) , Note 1
Normal Display Mode On (13h) , Note 1
All Pixel Off (22h)
All Pixel On (23h)
Gamma Set (26h), Note 2
Display Off (28h) , Note 1
Display ON (29h) , Note 1
Interface Pixel Format (3Ah)
Write Display Brightness (51h) , Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

Note 1 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, No Parameter"

Note 2 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, 1 Parameter

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

11 1001b

Word Count (WC)

o Word Count (WC): 0001h

Error Correction Code (ECC)

Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

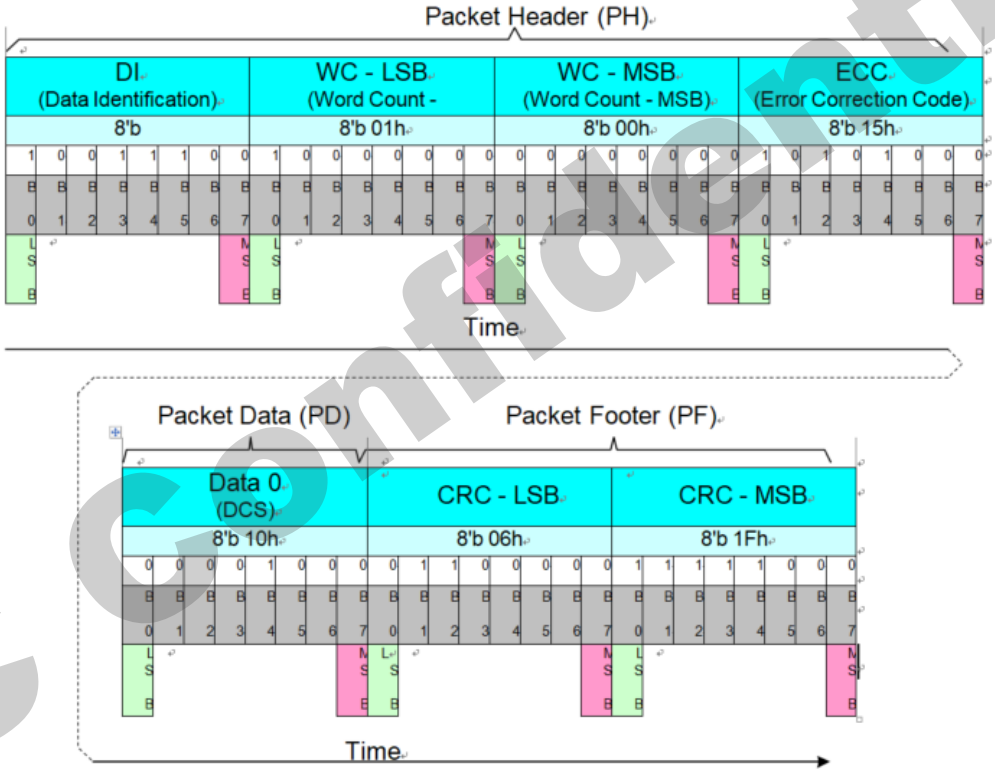


Figure 69 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

11 1001b

Word Count (WC)

o Word Count (WC): 0002h

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: “Gamma Set (26h)”, Display Command Set

(DCS) o Data 1: 01hex, Parameter of the DCS

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

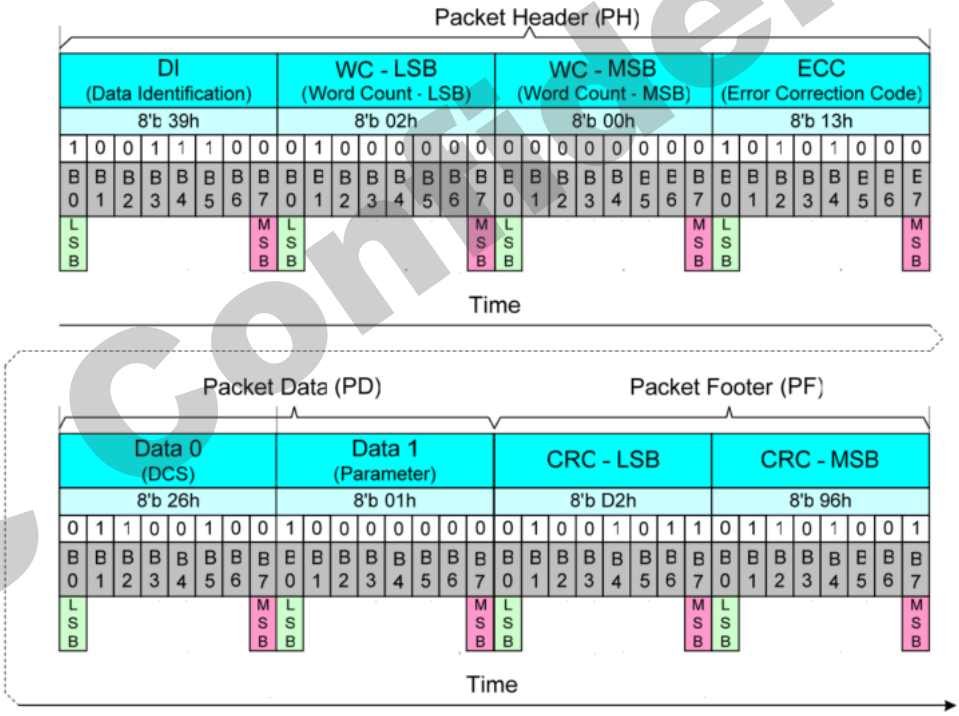


Figure 70 Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

11 1001b

Word Count (WC)

o Word Count (WC): 0005h

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS) o Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8] o Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC[7…0] o Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8] o Data 4: EFhex, 4th Parameter of the DCS, End Column EC[7…0]

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

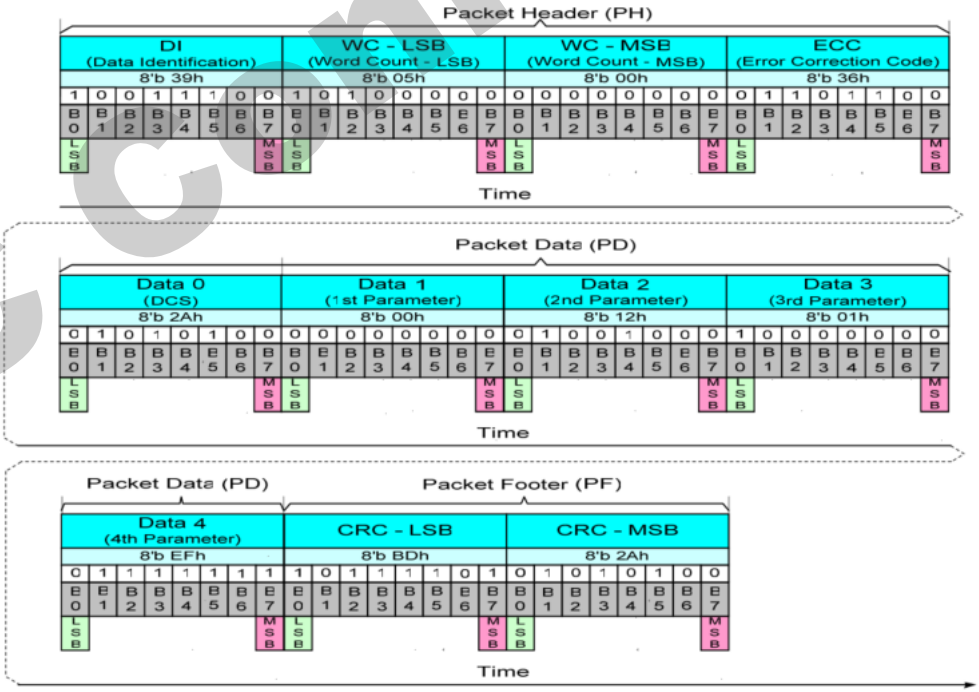


Figure 71 Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

5.2.28.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MPU to the display module. These commands are defined on a table (See chapter "5.2. Command Description") below.

Table 20 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Page 0 Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MPU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MPU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

The MPU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

11 0111b

Maximum Return Packet Size

(MRPS) o Data 0: 01hex

o Data 1: 00hex

Error Correction Code (ECC)

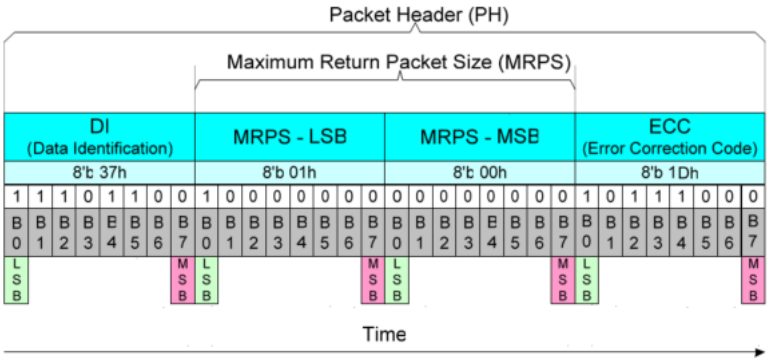


Figure 72 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MPU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MPU sends “Display Command Set (DCS) Read, No Parameter” to the display module

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

00 0110b

Packet Data (PD)

o Data 0: “Read ID1 (DAh)”, Display Command Set

(DCS) o Data 1: Always 00hex

Error Correction Code (ECC)

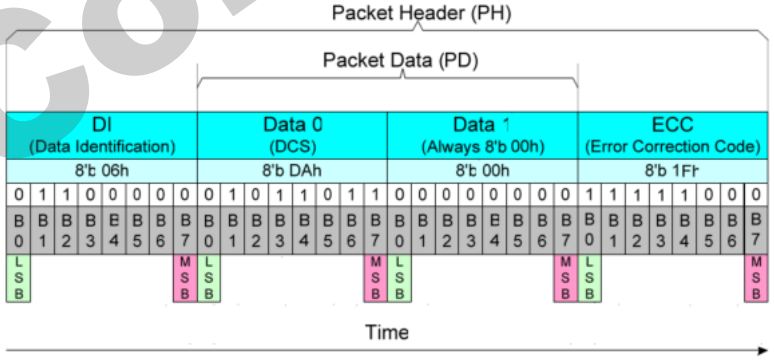


Figure 73 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MPU after Bus Turnaround (BTA)

An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a

command, See chapter “Acknowledge with Error Report (AwER)”

Information of the received command. Short Packet (SPa) or Long Packet (LPa)

5.2.28.1.6. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MPU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed.

The display module is ignored Packet Data (PD) what the MPU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

00 1001b

Word Count (WC)

o Word Count (WC): 0005hex

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: 89hex (Random data) o Data 1: 23hex (Random data) o Data 2: 12hex (Random data) o Data 3: A2hex (Random data) o Data 4: E2hex (Random data)

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

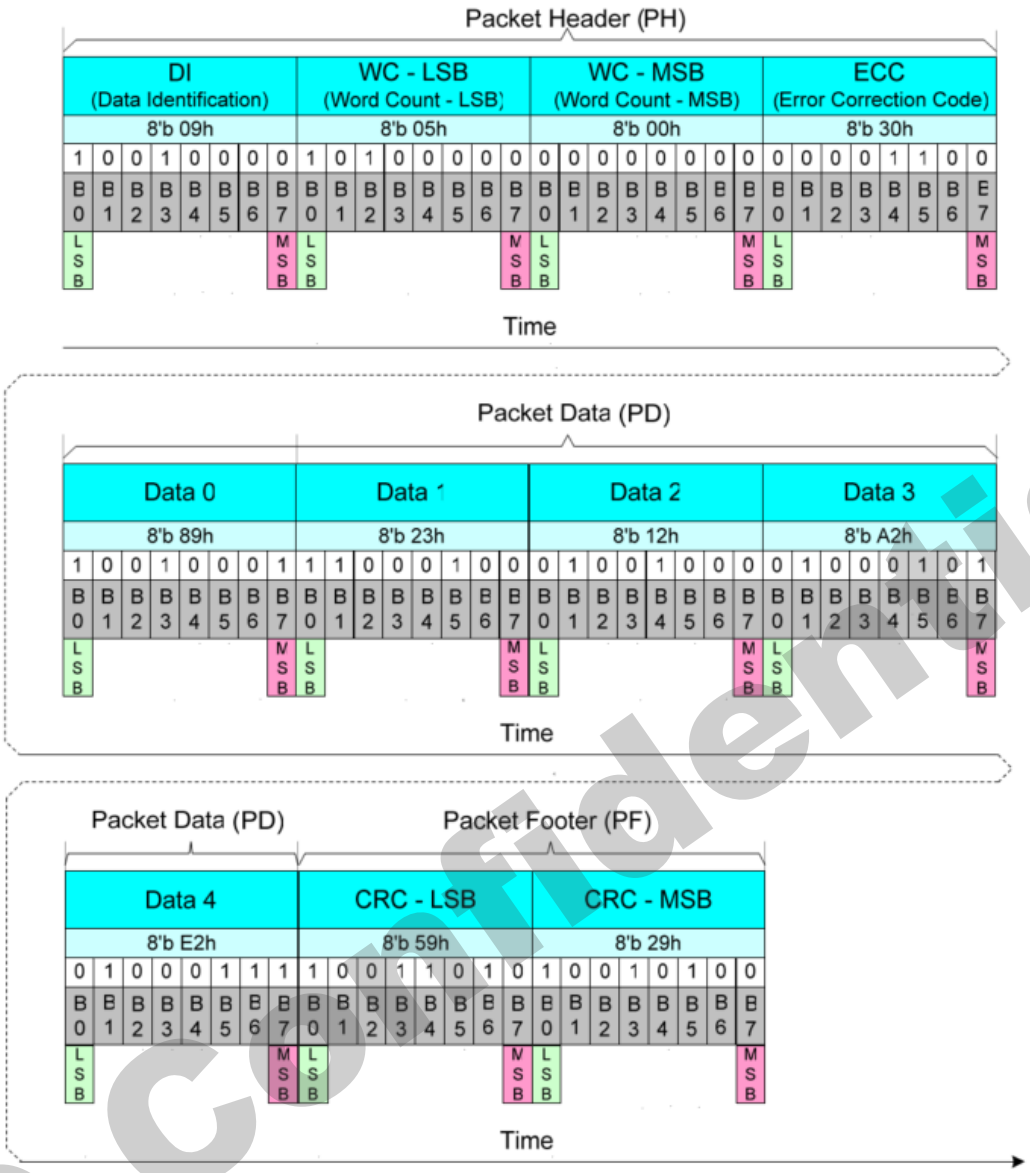


Figure 74 Null Packet, No Data (NP-L) - Example

End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MPU to the display module. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MPU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both: i.e. If the MPU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MPU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MPU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 21 Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission(LPDT)
MPU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MPU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) is using a fixed format as follows

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

00 1000b

Packet Data (PD)

o Data 0: 0Fhex

o Data 1: 0Fhex

Error Correction Code (ECC)

o ECC: 01hex

This is defined on the Short Packet (SPa) as follows.

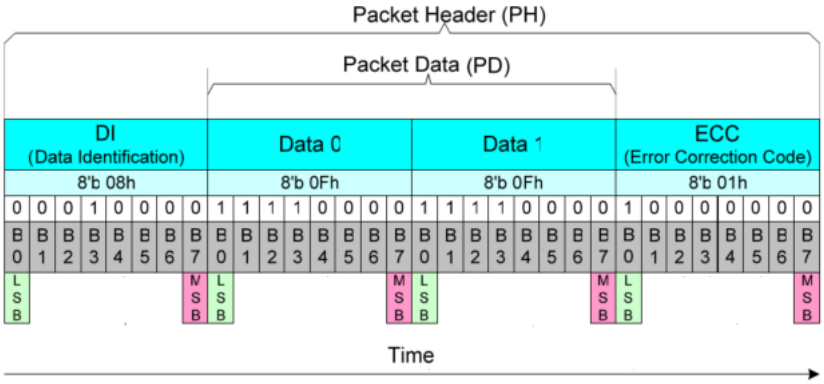


Figure 75 End of Transmission Packet (EoTP)

Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.

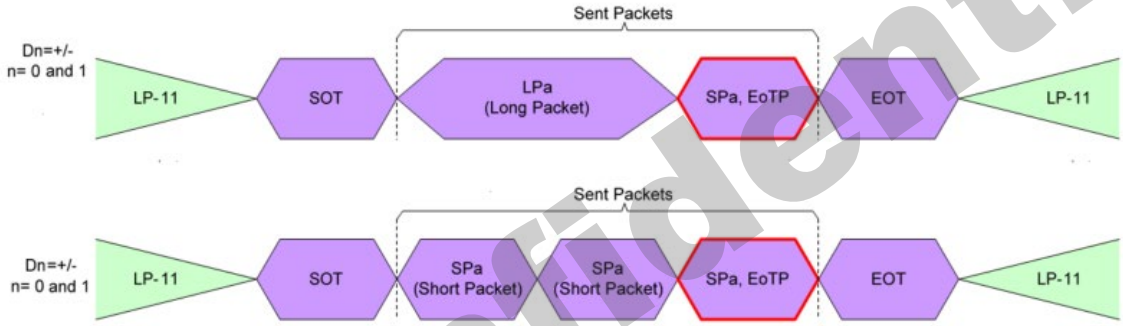


Figure 76 End of Transmission Packet (EoTP)-Examples

5.2.28.2. Packet from the Display Module to the MPU

5.2.28.2.1. Used Packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MPU after the MPU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter "Display Command Set (DCS) Read, No Parameter" (DCSRN-S)) or an Acknowledge with Error Report (See chapter: "Acknowledge with Error Report (AwER)" (AwER)).

The used packet type is defined on Data Type (DT). See chapter "Data Type (DT)". It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

Both cases are illustrated for reference purposes below.

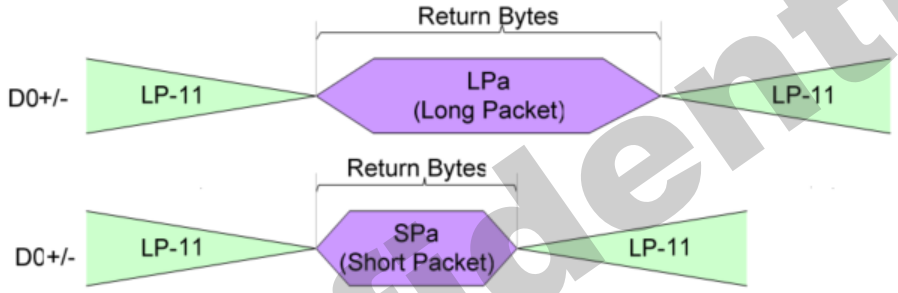


Figure 77 Return Bytes on Single Packet

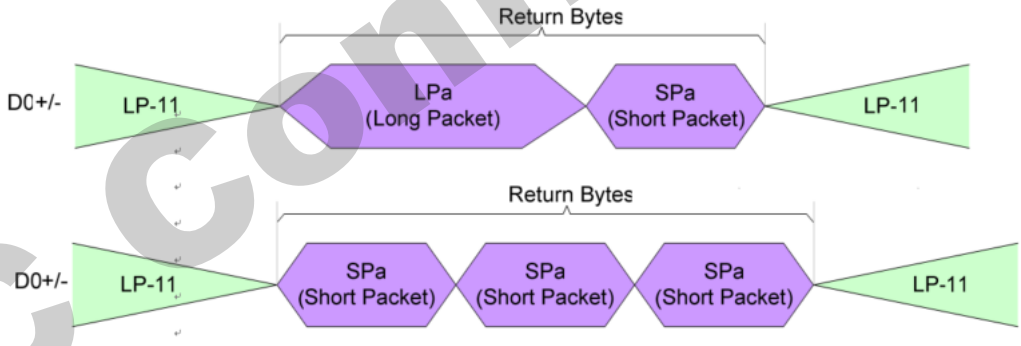


Figure 78 Return Bytes on Several Packets – Not Possible

Exception:

The display module is returning 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MPU when the display module has received a read command (See chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) where has been detected and corrected a single bit error by the EEC (See bit 8 on “Table 22: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”).

These return packets are illustrated for reference purposes below.

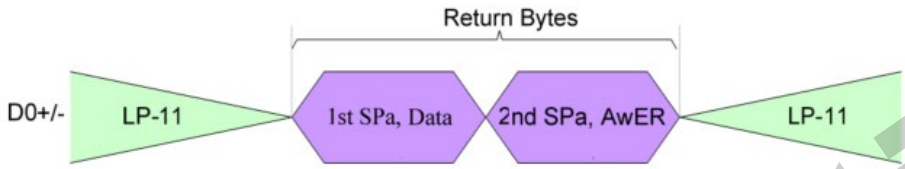


Figure 79 Exception when Return Bytes on Several Packets

AwER = Acknowledge with Error Report

5.2.28.2.2. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MPU. The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Table 22 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

B	Description
0	SoT Error
1	SoT Sync
2	EoT Sync
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 23 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync
2	EoT Sync
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to '0' internally Set to '0' internally (Only for Long Packet
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

These errors are included from all packages what has been received from the MPU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined

e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]):

00 0010b

Packet Data (PD)

o Bit 8: ECC Error, single-bit (detected and

corrected) o AwER: 0100h

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

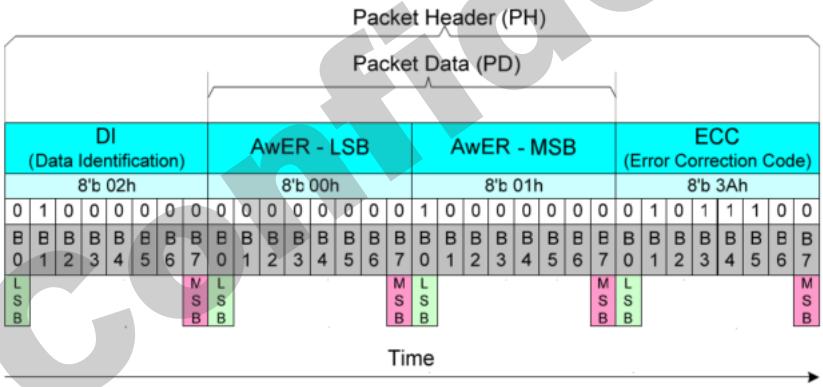


Figure 80 Acknowledge with Error Report (AwER) – Example

It is possible that the display module has received several packets, which have included errors, from the MPU before the MPU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

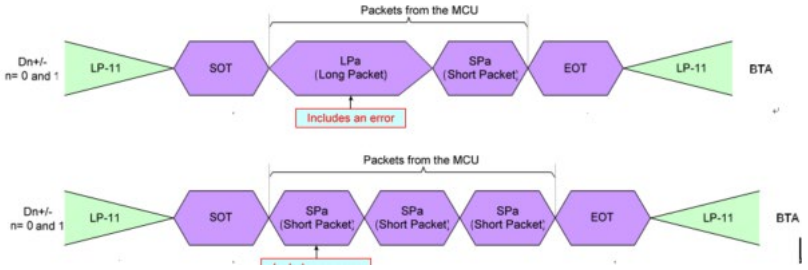


Figure 81 Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ***ECC or CRC*** error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MPU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.

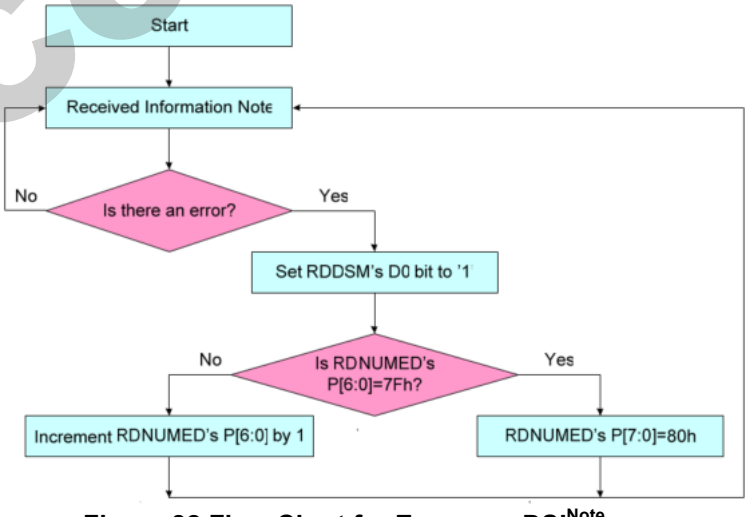


Figure 82 Flow Chart for Errors on DSI[Note]

Note 1. This information can be Interface or Packet Level Communication but it is always from the MPU to the display module in this case.

2. CRC or ECC error

5.2.28.2.3. DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 011100b), from the display module to the MPU.“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD)

Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

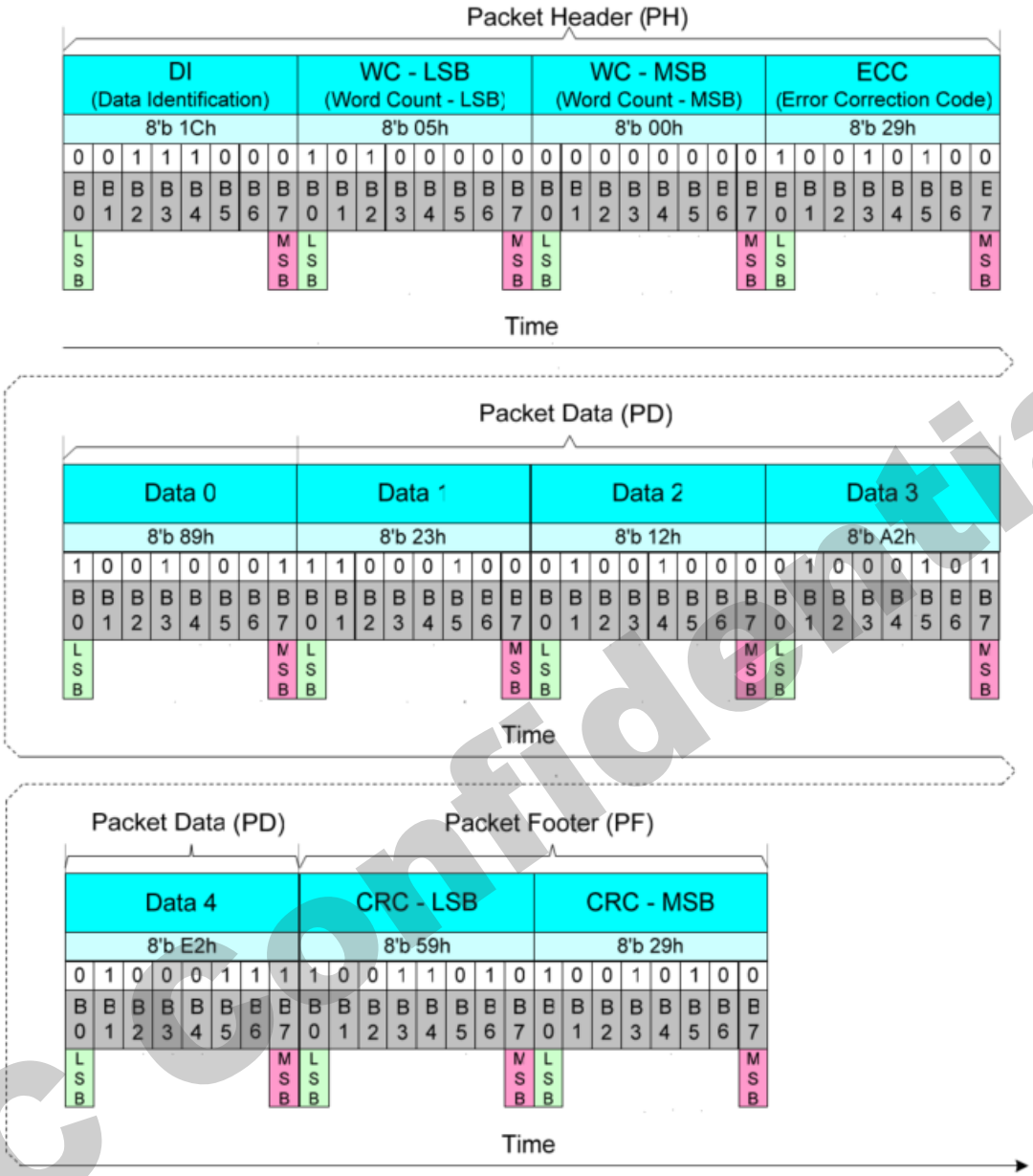


Figure 83 DCS Read Long Response (DCSRR-L) - Example

DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MPU."DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

Data Identification (DI)

Virtual Channel (VC, DI[7…6]):

00b

Data Type

(DT, DI[5…0]): 10 0001b

Packet Data

(PD) Data 0:

45hex

Data 1: 00hex (Always)

Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

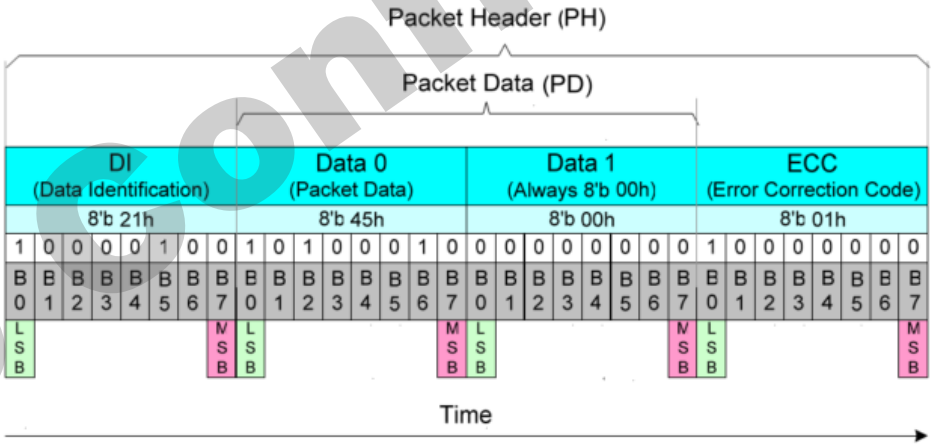


Figure 84 DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

5.2.28.2.4. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MPU."DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

This is defined on the Short Packet (SPa) as follows.

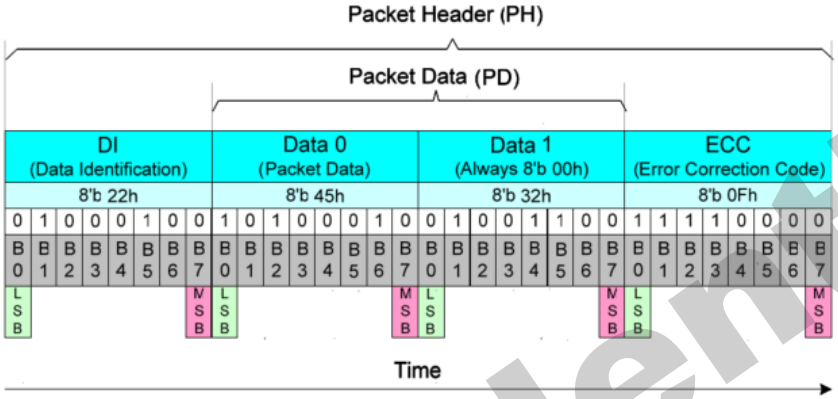


Figure 85 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

5.2.29. Communication Sequences

The communication sequences can be done on interface or packet levels between the MPU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes (DSI-D0+/- and DSI-D1+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See chapter “DSI-CLK Lanes”.

Functions of the interface level communication is described on the following table.

Table 24 Interface Level Communication

Interface	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High	HSDT	High speed Data

Functions of the packet level communication are described on the following table.

Table 25 Packet Level Communication

Interface Mode	Abbreviation	Packet	Interface Action Description
MPU	DCSW1-S	Short	DCS Write, 1 Parameter
	DCSWN-S	Short	DCS Write, No Parameter
	DCSW-L	Long	DCS Write Long
	DCSRN-S	Short	DCS Read, No Parameter
	SMRPS-S	Short	Set Maximum Return Packet
	NP-L	Long	Null Packet, No Data
	EoTP	Short	End of Transmission Packet
Display Module (GC9702C)	AwER	Short	Acknowledge with Error Packet
	DCSRR-L	Long	DCS Read Long Response
	DCSRR1-S	Short	DCS Read Short Response
	DCSRR2-S	Short	DCS Read Short Response

5.2.30. Sequences

5.2.30.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

Table 26 DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet	Interface Mode Control		Interface Mode	Packet	
1	- -	LP-11	- +	- -	- -	Start
2	DCSW1-S	LPDT	- +	- -	-	
3	- -	LP-11	- +	- -	- -	End

Table 27 DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sen	Interface Mode Control		Interface Mode Control	Packet Send	
1	- -	LP-11	- +	- -	- -	Start
2	DCSW1-S	HSDT	- +	- -	--	
3	EoTP	HSDT	- +	- -	--	End of Transmission Packet
4	- -	LP-11	- +	- -	- -	End

5.2.30.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

Table 29 DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	- -	LP-11	- +	- -	- -	Start
2	DCSWN-S	LPDT	-+	--	--	
3	- -	LP-11	- +	- -	- -	End

Table 30 DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	- -	LP-11	- +	- -	- -	Start
2	DCSWN-S	HSDT	- +	- -	- -	
3	EoTP	HSDT	- +	--	--	End of Transmission Packet
4	- -	LP-11	- +	- -	- -	End

Table 31 DCS Write, No Parameter Sequence – Example 3

5.2.30.3. DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 32 DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	-+	- -	--	Start
2	DCSW-L	LPDT	-+	- -	--	
3	--	LP-11	-+	- -	--	End

Table 33 DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	-+	- -	--	Start
2	DCSRN-S	HSDT	-+	- -	--	
3	EoTP	HSDT	-+	- -	--	End of Transmission Packet
4	--	LP-11	-+	- -	--	End

5.2.30.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

5.2.30.5. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Table 37 Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	- -	LP-11	- +	- -	- -	Start
2	NP-L	HSDT	- +	- -	- -	Only High Speed Data Transmission is used
3	EoTP	HSDT	- +	- -	- -	End of Transmission Packet
4	- -	LP-11	- +	- -	- -	End

5.2.30.6. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined on chapter “8.1.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

Table 38 End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MPU		Information Direction	Display Module (**GC9702C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	- +	- -	--	Start
2	NP-L	HSDT	- +	- -	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	- +	- -	--	End of Transmission Packet
4	--	LP-11	- +	- -	--	End

5.3. Display Data Format

5.3.1.16-bit per Pixel, Long packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, GC9702C has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

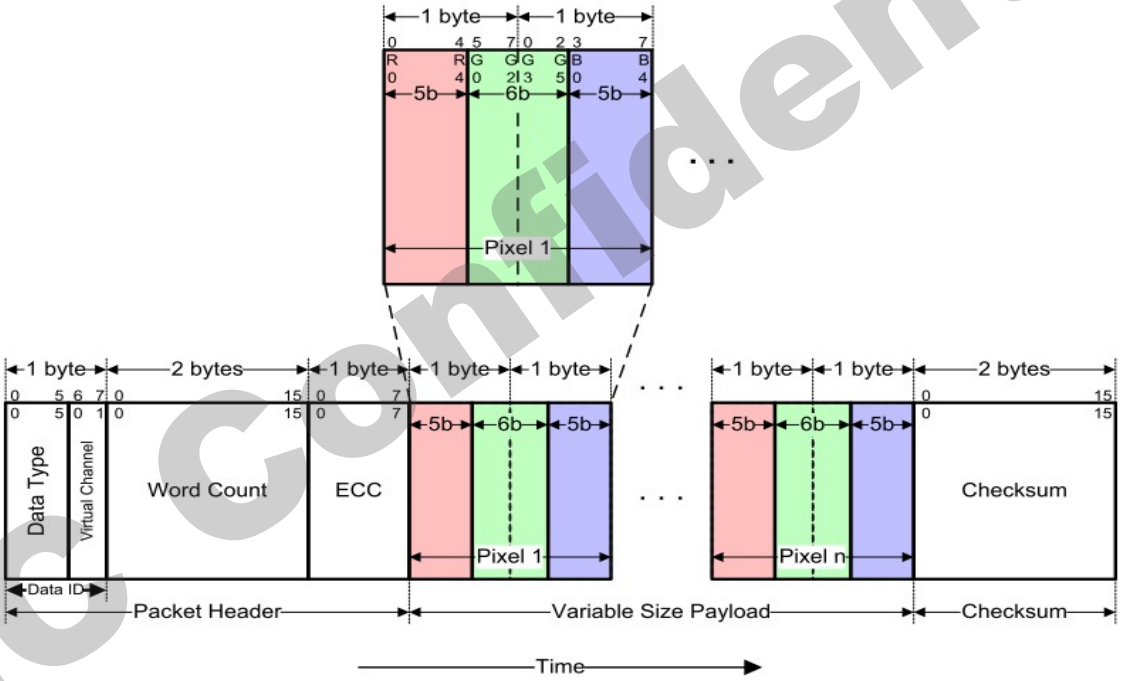


Figure 89 16-bit per Pixel, Data Type 00 1110 (0Eh)

5.3.2.18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

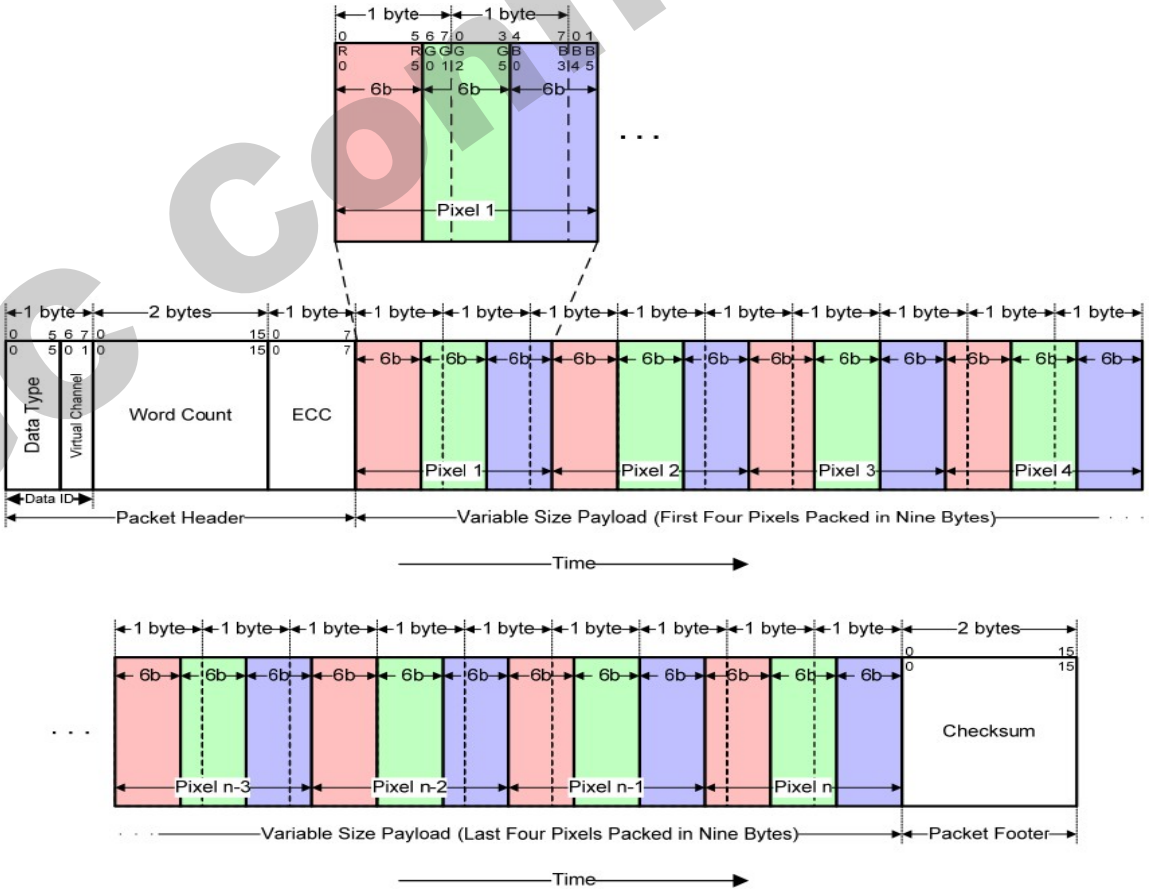


Figure 90 18-bit per Pixel, Data Type = 01 1110 (1Eh)

18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the "packed" format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

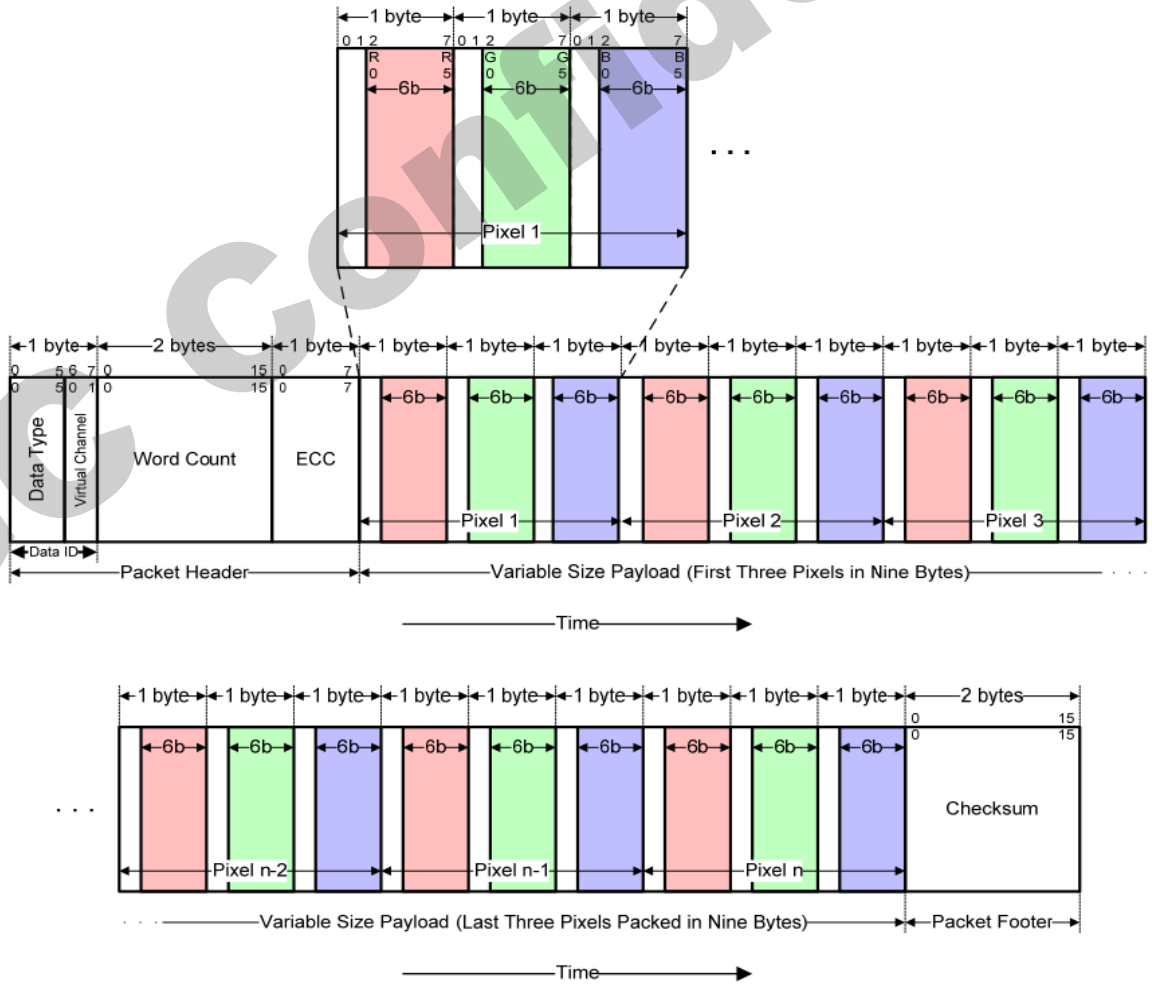


Figure 91 18-bit per Pixel, Data Type = 10 1110 (2Eh)

5.3.3. 24-bit per Pixel, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

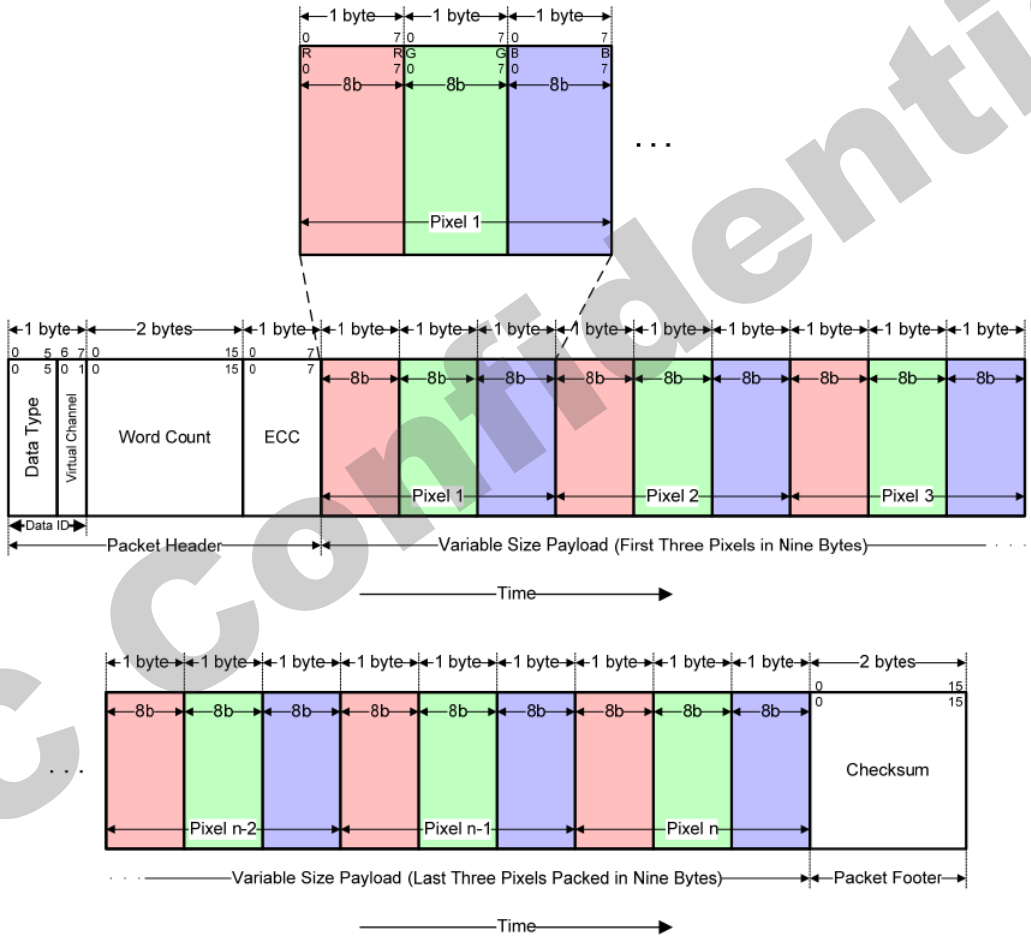


Figure 92 24-bit per Pixel, Data Type = 11 1110 (3Eh)

6. Command

6.1. User Command Set

Table 6.1.1 User Command Set

R/W	Address	Parameter								Function
	MIPI	D7	D6	D5	D4	D3	D2	D1	D0	
R	04h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
		ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
R	0Ah	Booster	idle		sleep_out	normal_on	disp_on			Read Display Power Mode
R	0Bh				gs	bgr	ss			Read Display MADCTR
R	0Dh			inv_on	pixel_on	pixel_off				Read Display Image Mode
R	0Eh	TE_ON	TE_MODE							Read TE Mode
W	10h	No Argument								Sleep in & booster off
W	11h	No Argument								Sleep out & booster on
W	13h	No Argument								Normal display mode on
W	20h	No Argument								INVOFF
W	21h	No Argument								INVON
W	22h	No Argument								ALLPOFF
W	23h	No Argument								ALLPON
W	28h	No Argument								Display off
W	29h	No Argument								Display on
W	34h	No Argument								TE OFF
W	35h								M	TE ON
W	36h					BGR		SS	GS	MADCTR
\W	38h	No Argument								Idle mode off
W	39h	No Argument								Idle mode on
W	44h						SCANLINE[10:8]			SETSCANLINE
		SCANLINE[7:0]								
R	45h						SCANLINE[10:8]			GETSCANLINE
		SCANLINE[7:0]								
W	51h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness
R	52h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness
W	53h			BCTL				BL		Write Control Display
R	54h			BCTL				BL		Read Control Display
W	55h							CABC[1:0]		Write Content Adaptive Brightness Control
R	56h							CABC[1:0]		Read Content Adaptive Brightness Control
W	5Eh	CMB[7:0]								Write CABC Minimum Brightness
R	5Fh	CMB[7:0]								Read CABC Minimum Brightness
R	DAh	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
R	DBh	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
R	DCh	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3
W	D5h	0X61								Manufacture command enable

		0X74							
		0X97							
W	D0h	0	0	0	MAUNC	0	0	PAGE[1:0]	Page set

Read Display ID (04h)

User Command Set		04h : RDNUMED (Read Display ID)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Read	ID1[7:0]								00h
2st Parameter	Read	ID2[7:0]								97h
3st Parameter	Read	ID3[7:0]								02h
Description	This read byte returns 24-bit display identification information. (the module's manufacture ID). And it is equal to returns value of DAh,DBh,DCh command.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009702
S/W Reset	24'h009702
H/W Reset	24'h009702

Read Display Power Mode (0Ah)

User Command Set		0Ah : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Read	Booster	idle	0	sleep_ out	normal_ on	disp_o n	0	0	8'h08

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or has a fault.
		1	Booster On and working OK
D6	IDEL MODE	0 1	IDEL MODE ON IDEL MODE OFF
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/Off	0	Display Normal Mode Off.
		1	Display Normal Mode On
D2	Display On/Off	0	Display is Off.
		1	Display is On

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h08
H/W Reset	8'h08

Read Display MADCTL (0Bh)

User Command Set		0Bh : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	1	0Bh
1st Parameter	Read	0	0	0	0	GS	BGR	0	SS	8'h00

Description

This command indicates the current status of the display as described in the table below.

Description	Value	Status
BGR	0	RGB
	1	BGR
GS	0	Gate output Top to Bottom
	1	Gate output Bottom to Top
SS	0	Source output Left to Right
	1	Source output Right to Left

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Read Display Image Mode (0Dh)

User Command Set		0Dh : RDDPM (Read Display Image Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	1	0Dh
1st Parameter	Read	0	0	INVO	allpon	allpoff	0	0	0	8'h00

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D5	Inversion On/Off	0	Inversion is Off.
		1	Inversion is On.
D4	All Pixels On	0	Normal Display
		1	White Display
D3	All Pixels Off	0	Normal Display
		1	Black Display

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Read TE Mode (0Eh)

User Command Set		0Eh : Read TE Mode								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	1	0	0Eh
1st Parameter	Read	TE_ON	TE_MODE	0	0	0	0	0	0	8'h00

Description

This command indicates the TE status of the display as described in the table below.

Bit	Description	Value	Status
D7	TE_ON	0	TE hiz
		1	TE output
D6	TE_Mode	0	Te mode on
		1	Te mode off

Restriction

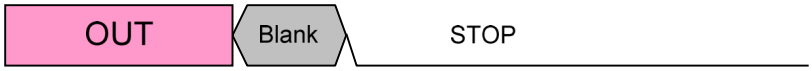
Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Sleep In (10h)

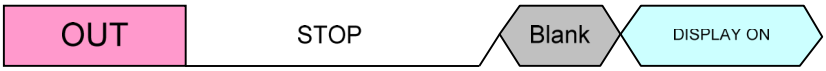
User Command Set		10h : CLOMD(Sleep In)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	0	10h
1st Parameter	-	XX								XXh
Description	This command causes the GC9702C to enter the minimum power consumption mode. 									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep out mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Sleep Out (11h)

User Command Set		11h : CLOMD(Sleep Out)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	1	11h
1st Parameter	-	XX								XXh
Description	This command causes the GC9702C to enter the Sleep Out mode 									
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The GC9702C loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the GC9702C is already Sleep Out mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default		
	Status	Default Value
	Power On Sequence	Sleep out mode
	S/W Reset	Sleep in mode
	H/W Reset	Sleep in mode

Normal Display Mode On (13h)

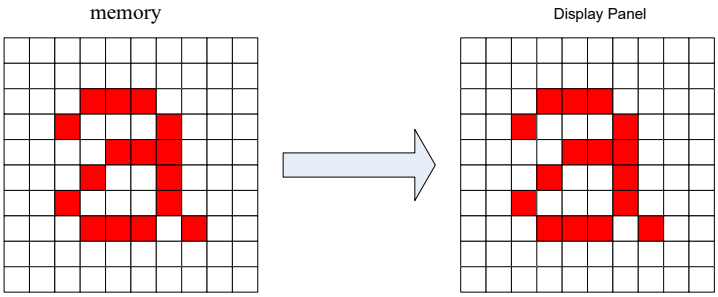
User Command Set		13h :CLOMD(Normal Display Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	1	1	13h
1st Parameter	Read	XX								XXh
Description	This command returns the display to Normal Display									
Restriction	This command has no effect when Normal Display Mode is active.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

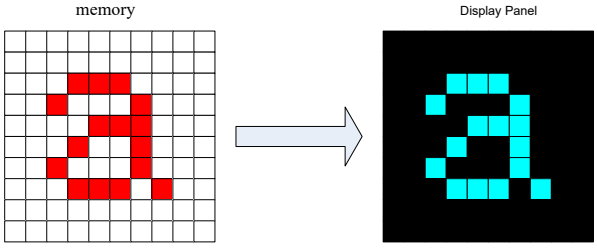
Display Inversion OFF (20h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20h
1st Parameter	-	XX								XXh
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. 									
Restriction										
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Display inversion off
H/W Reset	Display inversion off

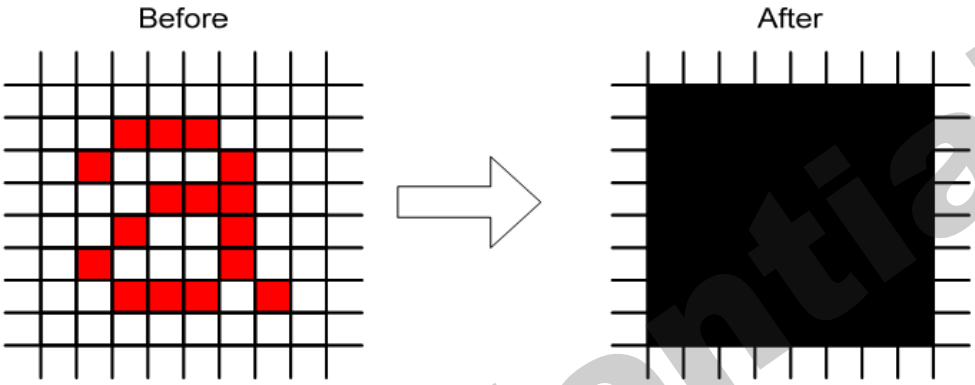
Display Inversion ON (21h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	21h
1st Parameter	-	XX								XXh
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.. 									
Restriction										
Register Availability										
Default										

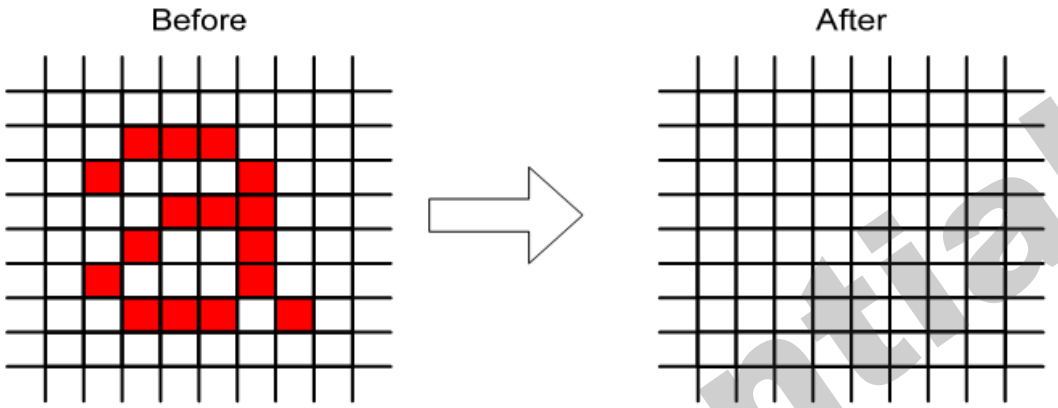
Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Display inversion off
H/W Reset	Display inversion off

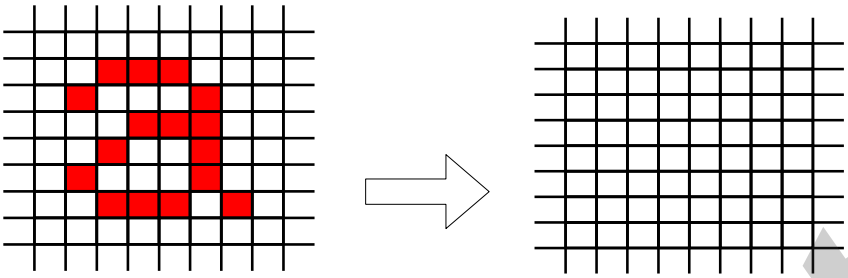
All Pixel Off (22h)

User Command Set		22h : CLOMD(all pixel Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	-	XX								XXh
Description	This command turns the display panel black in 'Sleep Out' mode and a status of the' Display On/Off' register can be 'on' or 'off'. This command does not change any other status 'All Pixels On', 'Normal Display Mode On' commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

All Pixel On (23h)

User Command Set		23h : CLOMD(all pixel On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	Read	XX								XXh
Description	This command turns the display panel white in 'Sleep Out ' mode and a status of the 'Display On/Off' register can be 'on' or 'off'. This command does not change any other status. 'All Pixels Off', 'Normal Display Mode On'– commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

Display Off (28h)

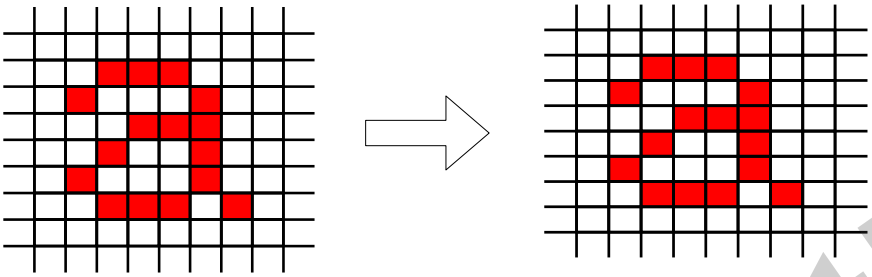
User Command Set		28h : CLOMD(Display Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	0	28h
1st Parameter	-	XX								XXh
Description	This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted. This command makes no change any other status. There will be no abnormal visible effect on the display. 									
Restriction	This command has no effect when module is already in Display Off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	display on mode
S/W Reset	display off mode
H/W Reset	display off mode

Display ON (29h)

User Command Set		29h : CLOMD(Display On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	1	29h
1st Parameter	-	XX								XXh
Description	This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status. 									
Restriction	This command has no effect when IC is already in Display on mode.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	display on mode
S/W Reset	display off mode
H/W Reset	display off mode

TE Off (34h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h
1st Parameter	-	XX								XXh
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									

Register Availability

Status	Availability
Power On Sequence	OFF
Sleep Out	OFF
Sleep In	OFF

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

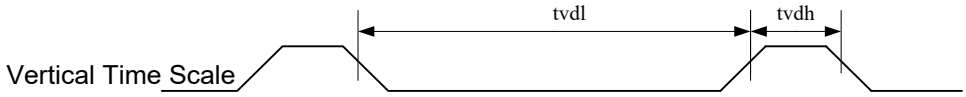
TE On(35h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	1	35h
1st Parameter	-								M	XXh

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already OFF.

Register Availability

Status	Availability
Power On Sequence	OFF
Sleep Out	OFF
Sleep In	OFF

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

MADCTR (36h)

<table>
<tr><th></th><th>Write / Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default (Hex)</th></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td>BGR</td><td></td><td>SS</td><td>GS</td><td>00</td></tr>
<tr><td>Description</td><td colspan="10">This command defines read/write scanning direction of frame memory.
<table>
<tr><td>GS</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr>
<tr><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr>
<tr><td>SS</td><td>Horizontal Refresh Order</td><td>LCD horizontal refreshing direction control.</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 16.7M colors.
X = Don’t care.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

Idle Mode Off (38h)

User Command Set		38h : CLOMD(Idle Mode Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	1	0	0	0	38h
1st Parameter	-	xx								xxh
Description	This command returns the display to Normal Display									
Restriction	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors. X = Don't care.									

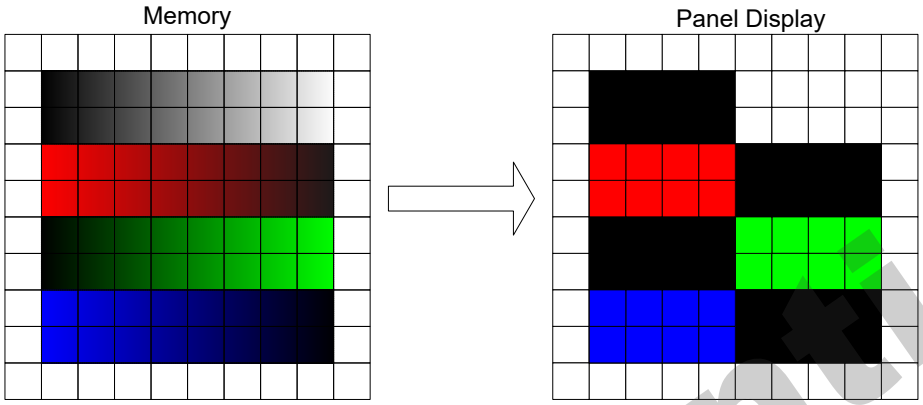
Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
S/W Reset	Idle mode OFF
H/W Reset	Idle mode OFF

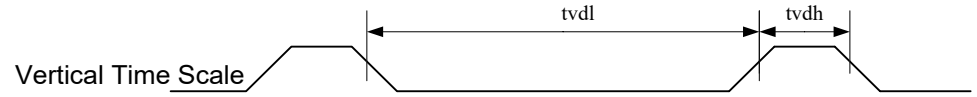
Idle Mode On (39h)

User Command Set		39h : CLOMD(Idle Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	1	0	0	1	39h
1st Parameter	Write	xx								xxh
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. 									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Idle mode OFF
S/W Reset	Idle mode OFF
H/W Reset	Idle mode OFF

Scan Line (44h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	0	0	44h
1st Parameter	Write						SCANLINE[10:8]			00h
2st Parameter	Write	SCANLINE[7:0]								00h
Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[10:0]  Note:that set_tear_scanline with STS is equivalent to set_tear_on with SCANLINE[10:0] eg:when the STS[8:0]=1,the TE will output at the position of Gate1. when the STS[8:0]=2,the TE will output at the position of Gate2. when the STS[8:0]=3,the TE will output at the position of Gate3.									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	11'h000
Sleep Out	11'h000
Sleep In	11'h000

Status	Default Value
Power On Sequence	11'h000
S/W Reset	11'h000
H/W Reset	11'h000

Write Display Brightness Value (51h)

	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write	0	DBV[7:0]							00h
Description	The command is used to adjust the brightness value of the display. DBV[7:0]: 8 bit, for display brightness of manual brightness setting. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read Display Brightness Value (52h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	1	0	1	0	52h
1st Parameter	Read	0	DBV[7:0]							00h
Description	The command is used to read the brightness value of the display. DBV[7:0]: 8 bit, for display brightness of manual brightness setting in the GC9702C.									
Restriction										
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Write CTL Display(53h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	00h

Description

This command is used to control ambient light, brightness and gamma setting.
BCTRL: Brightness Control Block On/Off
The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)
1	On, DBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

BL: Backlight Control On/Off without Dimming Effect
When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": output low (for high active) LEDONPOL="1": output high (for low active)
1	on	LEDONPOL="0": output high (for high active) LEDONPOL="1": output low (for low active)

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0_1 or 1_0.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read CTL Display(54h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Read	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command returns ambient light, brightness control and gamma setting value.
BCTRL: Brightness Control Block On/Off
The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)
1	On, DBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

BL: Backlight Control On/Off without Dimming Effect
When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": output low (for high active) LEDONPOL="1": output high (for low active)
1	on	LEDONPOL="0": output high (for high active) LEDONPOL="1": output low (for low active)

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0_1 or 1_0.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Write Content Adaptive Brightness Control Value **(55h)**

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	1	0	1	55h
1st Parameter	Write	0	0	0	0	0	0	CABC[1:0]		00h

Description

CABC[1:0]: Set parameters for image content based on the adaptive brightness control function. There are 4 different modes for the content adaptive image function. These modes are defined in the table below.

CABC [1:0]		Description
0	0	Off
0	1	UI mode
1	0	Still mode
1	1	Moving mode

Restriction

Register Availability

Status	**Availability**
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	**Default Value**
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read Content Adaptive Brightness Control Value **(56h)**

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	1	1	0	56h
1st Parameter	Read	0	0	0	0	0	0	CABC[1:0]		00h

Description

CABC[1:0]: Read the settings for image content based on the adaptive brightness control function.

CABC [1:0]		Description
0	0	Off
0	1	UI mode
1	0	Still mode
1	1	Moving mode

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Write CABC Minimum Brightness **(5Eh)**

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	1	1	1	0	5Eh
1st Parameter	Write	CMB[7:0]								00h
Description	This command is used to set the minimum brightness value of the display for the CABC function. **CMB[7:0]:** CABC minimum brightness control. This parameter is used to set a limit to the amount of brightness reduction allowed. When the CABC is active, it cannot reduce the display brightness to less than the CABC minimum brightness setting. Color enhancement function works normally, even if the brightness cannot be changed. This function does not affect the manual brightness setting. Manual brightness setting does not have a limit on allowable brightness reduction; display brightness can be set less than the CABC minimum brightness. Smooth transition and dimming function work normally. When the display brightness is turned off (BCTRL = 0 of Write CTRL Display (53h)), the CABC minimum brightness setting is ignored. The principle relationship is such that 00h value means the lowest brightness for the CABC, and FFh value means the highest brightness for the CABC.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read CABC Minimum Brightness **(5Fh)**

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	1	1	1	1	5Fh
1st Parameter	Read	CMB[7:0]								00h
Description	This command reads the minimum brightness value of the CABC function. The principle relationship is such that 00h value means the lowest brightness, and FFh value means the highest brightness. CMB[7:0] is the CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command.									
Restriction										
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read ID1 (DAh)

User Command Set		DAh : RDDPM (Read ID1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	0	DAh
1st Parameter	Read	ID1[7:0]								8h'00
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 1rst parameter of 04h command. The ID1 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0h'00
S/W Reset	0h'00
H/W Reset	0h'00

Read ID2 (DBh)

User Command Set		DBh : RDDPM (Read ID2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	1	DBh
1st Parameter	Read	ID2[7:0]								8'h97
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 2th parameter of 04h command. The ID2 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0'h97
S/W Reset	0'h97
H/W Reset	0'h97

Read ID3 (DCh)

User Command Set		DCh : RDDPM (Read ID3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	1	0	0	DCh
1st Parameter	Read	ID3[7:0]								8'h02
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 3th parameter of 04h command. The ID3 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h02
S/W Reset	8'h02
H/W Reset	8'h02

EXTC Command Set enable register (D5h)

User Command Set		D5h : EXTC Command Set enable register								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	0	1	0	1	D5h
1st Parameter	Write	0	1	1	0	0	0	0	1	61h
2st Parameter	Write	0	1	1	1	0	1	0	0	74h
3st Parameter	Write	1	0	0	1	0	1	1	1	97h
Description	‘D5h” is used to enable page select of page register.Three parameters must be wriitern continusly.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24h’ 000000
S/W Reset	24h’ 000000
H/W Reset	24h’ 000000

Page Sel (D0h)

User Command Set		D0h : Page Select								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	0	0	0	0	D0h
1st Parameter	Write	0	0	0	MAUC	0	0	PAGE[1:0]		00h

Description

Bit	Description	Value
MAUC	Manufacture Command Set enable/disable	"0": Manufacture Command Set disable "1": Manufacture Command Set enable
PAGE[1:0]	Manufacture Command Set selection	00:page0 01:page1 10:page2 11:reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8h' 00
S/W Reset	8h' 00
H/W Reset	8h' 00

6.2 Page 0 Command Set

Table 6.1.2 Page 0 Command Set

R/W	Address	Parameter								Function
	MIPI	D7	D6	D5	D4	D3	D2	D1	D0	
W	60h						F2_EN	F1_EN		VGL_CTL_EN
W	66h	Dinv_en								DISPLAY_CTL_EN
W	67h						Laneselen			LANSEL_EN
W	68h		A6_EN		A4_EN					VGH_CTL_EN
W	6Ah					Vcom_fix_en				VCOM_CTL_EN
W	6Bh	9F_EN	9E_EN	9D_EN						VREG_CTL
W	93h	D2D_VCOM_RES_FIX<7:0>								VCOM_CTL
W	B7h	0	0	0	0	dinv[3:0]				DISPLAY_CTL
W	BAh								D2D_LANSEL	INTER_LANSEL

VCOM_CTL(93h)

Page0 Command Set										
	Write/Rea	D7	D6	D5	D4	D3	D2	D1	D0	Default(Hex)
Command	Write	1	0	0	1	0	0	1	1	93h
1st Parameter	Write	D2D_VCOM_RES_FIX<7:0>								8'h7f

Description

D2D_VCOM_RES_FIX<7:0> is the adjustment register of VCOM in normal-temperature environment.

D2D_VCOM_RES_FIX<7:0>HEX	VCOM(V)
0	0
…	STEP -0.025
C	-0.3
D	-0.315
…	STEP -0.015
16	-0.45
17	-0.46
..	STEP -0.01
7F	-1.5
…	STEP -0.01
9D	-1.8
9E	-1.815
…	STEP -0.015
D0	-2.565
D1	-2.58
…	STEP -0.02
FF	-3.5

Restriction

To enable this command, "Page 0 Command Set enable register (F0h) " must set first.
Andenable register (6Ah)" b3" must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h7f
S/W Reset	8'h7f
H/W Reset	8'h7f

DISPLAY_CTL(B7h)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	1	0	1	1	1	B7h
1st Parameter	Write	0	0	0	0	DINV[3:0]				04

Description

DINV[3:0]	Inersion Mode for Source Driver
0h	1-Dot inversion
1h	2-Dot inversion
2h	3-Dot inversion
3h	4-Dot inversion
4h/5h	Column inversion
6h/7h	Test mode
8h	z-inv type1 (odd line shift left)
9h	z-inv type2 (even line shift left)
ah	z-inv type3 (odd line shift right)
bh	z-inv type4 (even line shift right)
others	reserved

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (66h)” b7” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8’h04
S/W Reset	8’h04
H/W Reset	8’h04

INTER_LANESEL(BAh)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	BAh
1st Parameter	Write	0	0	0	0	0	0	0	D2D_LANSEL	00

Description

External Pad Set				register	Configuration of MIPI				
LANSEL	IM2	IM1	IM0	D2D_LANSEL	CLKP/N	D0P/N	D1P/N	D2P/N	D3P/N
0	0	0	0	1	CLKP/N	D3P/N	D2P/N	D1P/N	D0P/N
0	0	0	1	1	CLKN/P	D3N/P	D2N/P	D1N/P	D0N/P
0	0	1	0	1	CLKP/N	D0P/N	D1P/N	D2P/N	D3P/N
0	0	1	1	1	CLKN/P	D0N/P	D1N/P	D2N/P	D3N/P
0	1	0	0	1	CLKP/N	D3P/N	D0P/N	D1P/N	D2P/N
0	1	0	1	1	CLKN/P	D3N/P	D0N/P	D1N/P	D2N/P
0	1	1	0	1	CLKP/N	D2P/N	D1P/N	D0P/N	D3P/N
0	1	1	1	1	CLKN/P	D2N/P	D1N/P	D0N/P	D3N/P
0	0	0	0	0	CLKP/N		D2P/N	D1P/N	D0P/N
0	0	0	1	0	CLKN/P		D2N/P	D1N/P	D0N/P
0	0	1	0	0	CLKP/N	D0P/N	D1P/N	D2P/N	
0	0	1	1	0	CLKN/P	D0N/P	D1N/P	D2N/P	
0	1	0	0	0	CLKP/N		D0P/N	D1P/N	D2P/N
0	1	0	1	0	CLKN/P		D0N/P	D1N/P	D2N/P
0	1	1	0	0	CLKP/N	D2P/N	D1P/N	D0P/N	
0	1	1	1	0	CLKN/P	D2N/P	D1N/P	D0N/P	
1	0	0	0	0	CLKP/N			D1P/N	D0P/N
1	0	0	1	0	CLKN/P			D1N/P	D0N/P
1	0	1	0	0	CLKP/N	D0P/N	D1P/N		
1	0	1	1	0	CLKN/P	D0N/P	D1N/P		
1	1	0	0	0	CLKP/N		D0P/N	D1P/N	
1	1	0	1	0	CLKN/P		D0N/P	D1N/P	
1	1	1	0	0	CLKP/N		D1P/N	D0P/N	
1	1	1	1	0	CLKN/P		D1N/P	D0N/P	
Others					Reserved				

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (66h)” b7” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00
S/W Reset	00
H/W Reset	00

VGH_CTL(A4h&A6h)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	0	0	1	0	0	A4h
1st Parameter	Write	VGHS_temp_low[3:0]				VGHS[3:0]				F6
Command	Write	1	0	1	0	0	1	1	0	A6h
1st Parameter	Write	VGH_BOOST_H	0	1	1	1	1	0	0	BC

Description

VG[illegible] and VGH_BOOST_H the adjustment register of VGH amplitude (AVDD -5.5V

VGH_BOOST_H	VGHS[3:0]	VGH/V	VGH_BOOST_H	VGHS[3:0]	VGH/V
0	0	7.01AVEE=-5.5V）	1	0	12
0	1	7.2	1	1	12.56
0	2	7.4	1	2	12.86
0	3	7.61	1	3	13.5
0	4	7.83	1	4	13.85
0	5	7.94	1	5	14.59
0	6	8.18	1	6	15
0	7	8.44	1	7	15.43
0	8	8.57	1	8	15.88
0	9	8.85	1	9	16.36
0	A	9	1	A	16.88
0	B	9.47	1	B	17.42
0	C	10	1	C	18
0	D	10.59	1	D	18.62
0	E	11.02	1	E	19.29
0	F	11.49	1	F	20

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (68h)” b6” and ” b4” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

A4h		A6h	
Status	**Default Value**	**Status**	**Default Value**
Power On Sequence	F6	Power On Sequence	BC
S/W Reset	F6	S/W Reset	BC
H/W Reset	F6	H/W Reset	BC

VGL_CTL(F1h&F2h)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	0	0	0	1	F1h
1st Parameter	Write	0	1	0	1	VGLS[3:0]				53
Command	Write	1	1	1	1	0	0	1	0	F2h
1st Parameter	Write	0	0	VGL_BT[1:0]		0	1	0	1	05

Description

VGL_BT[1:0]	VGLS[3:0]	VGL/V	VGL_BT[1:0]	VGLS[3:0]	VGL/V
00	0	-8.1	01	0	-7.5
00	1	-8.8	01	1	-8.33
00	2	-9.56	01	2	-9.4
00	3	-10.28	01	3	-10.33
00	4	-10.84	01	4	-11.27
00	5	-10.85	01	5	-12.12
00	6	-10.85	01	6	-13.07
00	7	-10.85	01	7	-13.63
00	8	-10.85	01	8	-14.45
Others reserved					

VGLS[3:0] the adjustment register of VGL amplitude（AVDD=5.5V AVEE=-5.5V）

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (60h)” b1” and ” b2” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

F1h		F2h	
Status	**Default Value**	**Status**	**Default Value**
Power On Sequence	53	Power On Sequence	05
S/W Reset	53	S/W Reset	05
H/W Reset	53	H/W Reset	05

VREG_CTL1(9Dh)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	1	1	1	0	1	9Dh
1st Parameter	Write	VRH [7:0]								87
2nd Parameter	Write	VRH_temp_low[7:0]								87
3rd Parameter	Write	VRH_temp_high[7:0]								87

Description

VRH[7:0] is the adjustment register of VGMP/VGNM in normal temperature environment.
VRH_temp_low[7:0] is the adjustment register of VGMP/VGNM in low temperature environment
VRH_temp_high[7:0] is the adjustment register of VGMP/VGNM in high temperature environment
VGMP=(VBP<7:0>+VRH<7:0>)*0.0125+2.8125
VGMN=(VBN<7:0>+VRH<7:0>)*(-0.0125)-2.8125

VRH[7:0]	VBP[7:0]	VGMP(V)	VRH[7:0]	VBN[7:0]	VGMN(V)
0	0	2.8125	0	0	-2.8125
1	0	2.825	1	0	-2.825
..	0	…	..	0	..
N	0	2.8125+0.0125*N	N	0	-2.8125-0.0125*N
…	0	…	…	0	…
135	0	4.5	135	0	-4.5
…	0	…	…	0	…
255	0	6	255	0	-6

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (6Bh)” b5” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8’h87
S/W Reset	8’h87
H/W Reset	8’h87

VREG_CTL2(9Eh)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	1	1	1	1	0	9Eh
1st Parameter	Write	VBP [7:0]								00
2nd Parameter	Write	VBP_temp_low[7:0]								00
3rd Parameter	Write	VBP_temp_high[7:0]								00

Description

VBP[7:0] is the adjustment register of VGMP in normal temperature environment.
VBP_temp_low[7:0] is the adjustment register of VGMP in low temperature environment
VBP_temp_high[7:0] is the adjustment register of VGMP in high temperature environment
VGMP=(VBP<7:0>+VRH<7:0>)*0.0125+2.8125

VRH[7:0]	VBP[7:0]	VGMP(V)
87	0	4.5
87	1	4.5125
.87.	…	…
87	N	2.8125+0.0125*N
87	…	…
87		4.5
87	…	…
87	255	7.6875

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (6Bh)” b6” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8’h00
S/W Reset	8’h00
H/W Reset	8’h00

VREG_CTL3(9Fh)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	1	1	1	1	1	9Fh
1st Parameter	Write	VBN [7:0]								00
2nd Parameter	Write	VBN_temp_low[7:0]								00
3rd Parameter	Write	VBN_temp_high[7:0]								00

Description

VBN[7:0] is the adjustment register of VGNM in normal temperature environment.
VBN_temp_low[7:0] is the adjustment register of VGNM in low temperature environment
VBN_temp_high[7:0] is the adjustment register of VGNM in high temperature environment
VGMN=(VBN<7:0>+VRH<7:0>)*(-0.0125)-2.8125

VRH[7:0]	VBN[7:0]	VGMN(V)
87	0	-4.5
87	0	-4.5125
.87.	0	…
87	0	-2.8125-0.0125*N
87	0	…
87	0	-7.6875

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (6Bh)” b7” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8’h00
S/W Reset	8’h00
H/W Reset	8’h00

6.2 Page 1 Command Set

Table 6.1.3 Page 1 Command Set

R/W	Address	Parameter								Function
	MIPI	D7	D6	D5	D4	D3	D2	D1	D0	
W	60h						F2_EN	F1_EN		Gamma_en

GAMMA SET(F1h)

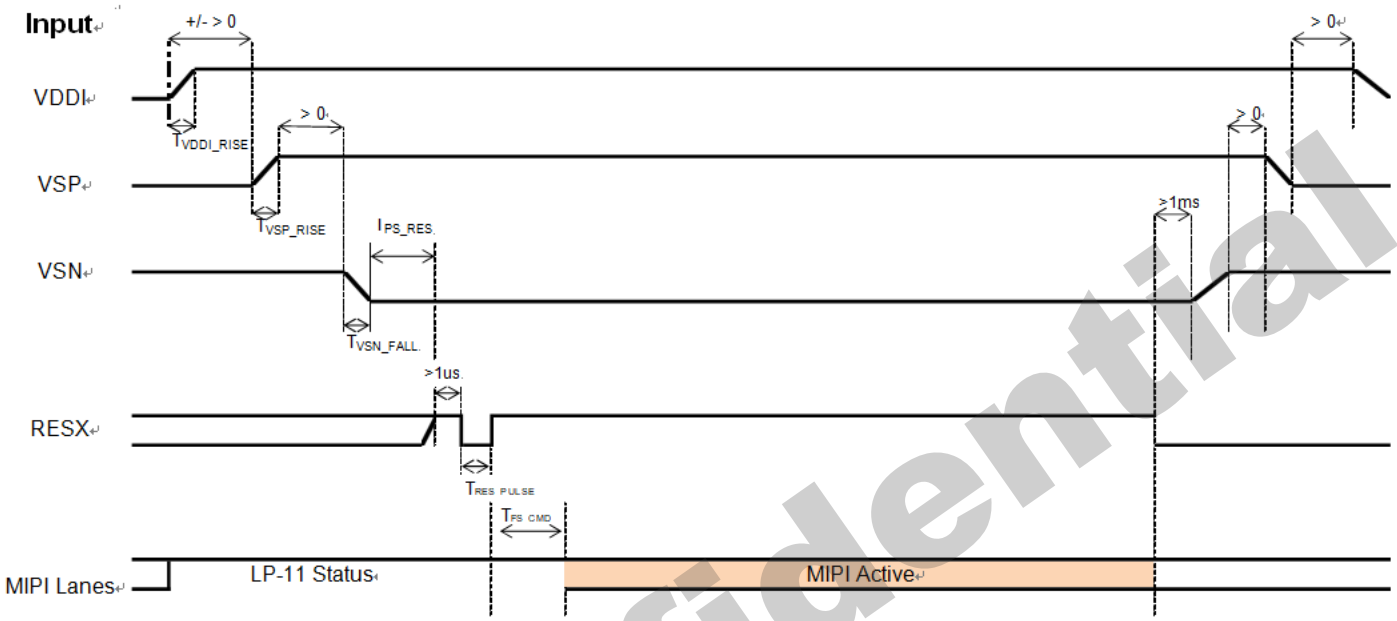
Page1 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	1	F1h
		Grey 0								
1st Parameter	Write		1	1	1	1	1	1	1	7F
		Grey 4								
2nd Parameter	Write		1	1	1	0	0	1	1	73
		Grey 8								
3rd Parameter	Write		1	1	0	1	0	0	0	68
		Grey 12								
4th Parameter	Write		1	0	1	1	1	1	1	5F
		Grey 19								
5th Parameter	Write		1	0	1	1	1	1	1	5F
		Grey 27								
6th Parameter	Write		1	0	1	0	0	0	1	51
		Grey 43								
7th Parameter	Write		1	0	1	0	1	1	1	57
		Grey 63								
8th Parameter	Write		1	0	0	0	0	0	1	41
		Grey 95								
9th Parameter	Write		1	0	1	1	0	0	1	59
		Grey 127								
10th Parameter	Write		1	0	1	0	1	1	1	57
		Grey 159								
11st Parameter	Write		1	0	1	0	1	1	1	57
		Grey 191								
12nd Parameter	Write		1	1	1	0	1	0	0	74
		Grey 211								
13rd Parameter	Write		1	1	0	0	0	0	1	61
		Grey 227								
14th Parameter	Write		1	1	0	0	1	1	0	66
		Grey 235								
15th Parameter	Write		1	0	1	0	1	0	1	55
		Grey 243								
16th Parameter	Write		1	0	0	1	0	1	1	53
		Grey 247								
17th Parameter	Write		0	1	1	1	0	0	1	39
		Grey 251								
18th Parameter	Write		0	1	0	0	0	0	1	21
		Grey 255								
19th Parameter	Write		0	0	0	0	0	0	0	00
Description	F1h is the positive polarity of gamma.. This command is used to set the gray scale voltage to adjust the gamma characteristics of the TFT panel. For IPS panel, the luminance: grey0>grey4>……>grey255. For TN panel, the luminance: grey255>grey251>……>grey0									
Restriction	To enable this command, “Page1 Command Set enable register (F0h) ” must set first. Andenable register (60h)” b1” must set 1									

GAMMA SET(F2h)

Page1 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	1	0	F2h
		Grey 0								
1st Parameter	Write		1	1	1	1	1	1	1	7F
		Grey 4								
2nd Parameter	Write		1	1	1	0	0	1	1	73
		Grey 8								
3rd Parameter	Write		1	1	0	1	0	0	0	68
		Grey 12								
4th Parameter	Write		1	0	1	1	1	1	1	5F
		Grey 20								
5th Parameter	Write		1	0	1	1	1	1	1	5F
		Grey 28								
6th Parameter	Write		1	0	1	0	0	0	1	51
		Grey 44								
7th Parameter	Write		1	0	1	0	1	1	1	57
		Grey 64								
8th Parameter	Write		1	0	0	0	0	0	1	41
		Grey 96								
9th Parameter	Write		1	0	1	1	0	0	1	59
		Grey 128								
10th Parameter	Write		1	0	1	0	1	1	1	57
		Grey 160								
11st Parameter	Write		1	0	1	0	1	1	1	57
		Grey 192								
12nd Parameter	Write		1	1	1	0	1	0	0	74
		Grey 212								
13rd Parameter	Write		1	1	0	0	0	0	1	61
		Grey 228								
14th Parameter	Write		1	1	0	0	1	1	0	66
		Grey 236								
15th Parameter	Write		1	0	1	0	1	0	1	55
		Grey 243								
16th Parameter	Write		1	0	0	1	0	1	1	53
		Grey 247								
17th Parameter	Write		0	1	1	1	0	0	1	39
		Grey 251								
18th Parameter	Write		0	1	0	0	0	0	1	21
		Grey 255								
19th Parameter	Write		0	0	0	0	0	0	0	00
Description	F2h is the negative polarity of gamma.. This command is used to set the gray scale voltage to adjust the gamma characteristics of the TFT panel. For IPS panel, the luminance: grey0>grey4>……>grey255. For TN panel, the luminance: grey255>grey251>……>grey0									
Restriction	To enable this command, “Page1 Command Set enable register (F0h) ” must set first. Andenable register (60h)” b2” must set 1									

7. Power ON/OFF Sequence

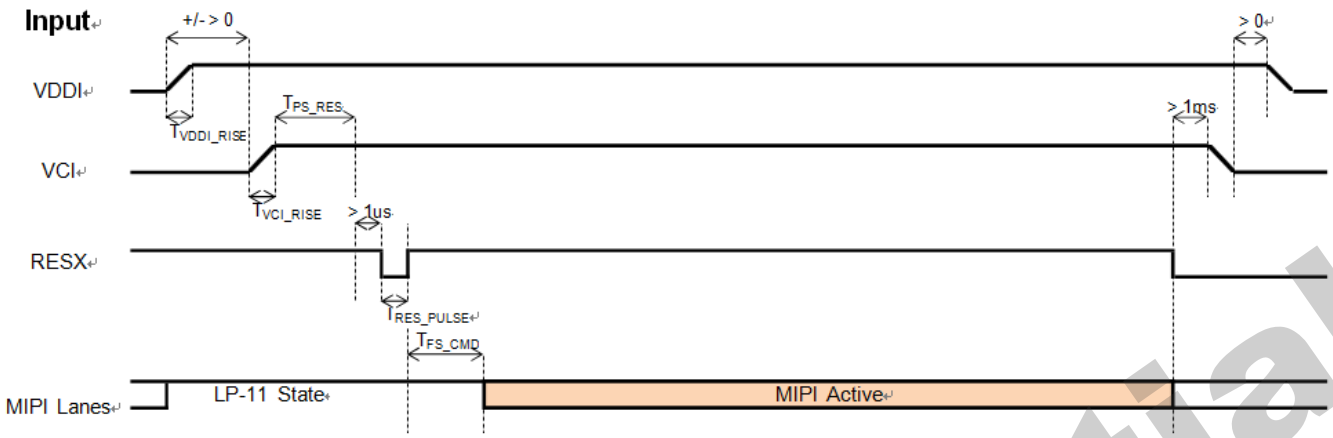
7.1. 3 Power Mode



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	10	-	-	us
T_{VSN_FALL}	VSN Fall time	10	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	50	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Power on/off sequence with 3 Power Mode

7.2. 2 Power Mode



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	VCI Rise time	10	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	50	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Power on/off sequence with 2 Power Mode

7.3. Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9702C will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it u

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

The absolute maximum rating is listed on Table 42. When the GC9702C is used out of the absolute maximum ratings, it may be permanently damaged. To use the GC9702C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the GC9702C will malfunction and cause poor reliability.

Table 43 Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VDD ~ AGND	V	-0.3 ~ +4.6
Supply voltage (I/O)	VDDI ~ DGND	V	-0.3 ~ +4.6
OTP Supply voltage	VPP ~ AGND	V	-0.3 ~ +10
Supply voltage	AVDD ~ AGND	V	-0.3 ~ +8
Supply voltage	AVEE ~ AGND	V	0.3 ~ -8
Supply voltage	VGH ~ AGND	V	-0.3 ~ +20
Supply voltage	VGL ~ AGND	V	0.3 ~ -16
Driver supply voltage	AVDD – AVEE	V	≦14V
Driver supply voltage	VGH – VGL	V	≦30V
Input voltage	V_{IN}	V	-0.3 ~ VDDI + 0.3
HS Input voltage	V_{HSIN}	V	-0.3 ~ + 2
Operating temperature	Topr	℃	-40 ~ +80
Storage temperature	Tstg	℃	-55 ~ +110

Note:

Even if the one of the above parameters is exceeded momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the exceeding values which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	VDDR VDDA VDDB	-	2.5	2.8	3.3	V	
Operating voltage	VDDI	-	1.65	1.8	3.3	V	Note1,2
OTP Supply voltage	VPP	-		8.0		V	Note1
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE, SDO (SDA) , LEDPWM	VOH	-	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE, SDO (SDA) , LEDPWM	VOL	-	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	10	-	16	V	
Gate Driver Low Voltage	VGL	-	-12	-	-8.0	V	
Driver Supply Voltage	-	|VGH-VGL|	17	-	28	V	
DC VCOM Amplitude Voltage	VCOM		-3.5	-1.5	0	V	Note3
Source Output Range	VSOUT	-	VGMN +0.1	-	VGMP -0.1	V	Note4
Positive Gamma Reference Voltage	VGMP	-	2.8125	4.5	6	V	Note5
Negative Gamma Reference Voltage	VGMN	-	-2.8125	-4.5	-6	V	Note5
Positive Gamma Reference Voltage	VGSP	-	-3.1875	0	0	V	Note5
Negative Gamma Reference Voltage	VGSN	-	0	0	3.1875	V	Note5

Note:

1. Ta = -30 to 70 °C (to 85 °C no damage), VDDI=1.65V to 3.3V, VDDR VDDA VDDB=2.5V to 3.3V.
2. Supply digital VDDI voltage equal or less than analog VDDR VDDA VDDB voltage.
3. Source channel loading = 10pF/channel
4. The Max. Value is between with Note 3 measure point and Gamma setting value

.

8.3. DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

8.4. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	VDD	Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	V_{VDD_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	V_{VDDI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. These values are not symmetric amplitude, which centersm3g points are VDDI or VDD. See examples as reference purposes, when V_{VDD_NOISE} and V_{VDDI_NOISE} are maximums, below.

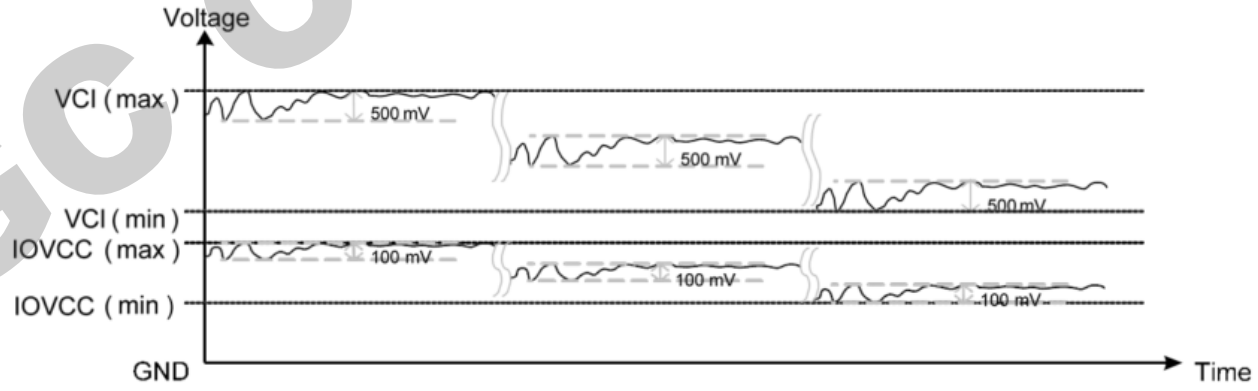


Figure 109 Noise on Power Supply Lines

8.5. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA, Note 2	0.8 V_{VDD}	-	V_{VDD}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=1mA, Note 2	0.0	-	0.2V_{VDD}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD, Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD, Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1), Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1), Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. LEDPWM
3. DSI High Speed mode is off

8.6. Spike / Glitch Rejection

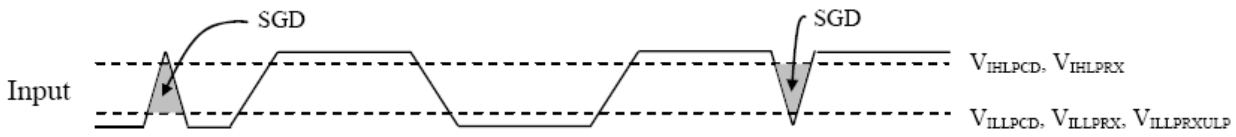


Figure 110 Spike / Glitch Rejection

Note:

1. Peak Interference Amplitude max. 200mV and Interference Frequency min. 450MHz.
2. n = 0 and 1.

Table 44 Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-, DSI-Dn+/-	SGD	Input pulse rejection for DSI	-	300	Vps

8.7. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	00	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-		-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

1. Ta = -30℃ to 70℃ (to +85℃ no damage), VDDI = 1.65 to 1.95V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0 and 1.
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.

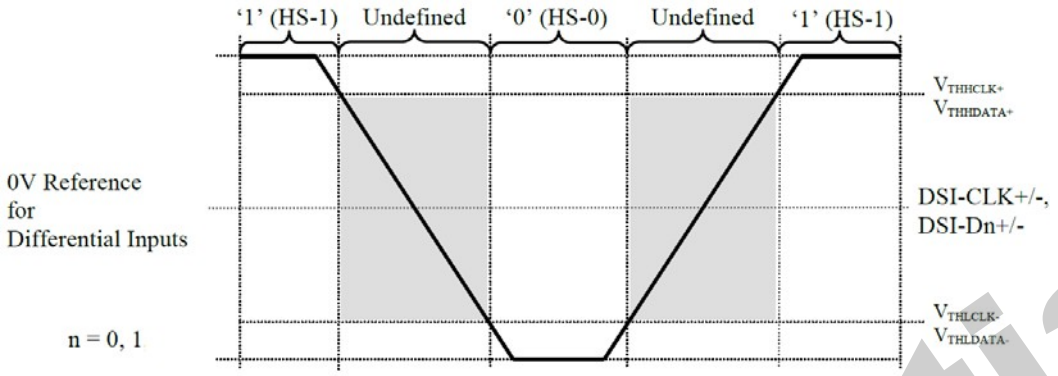
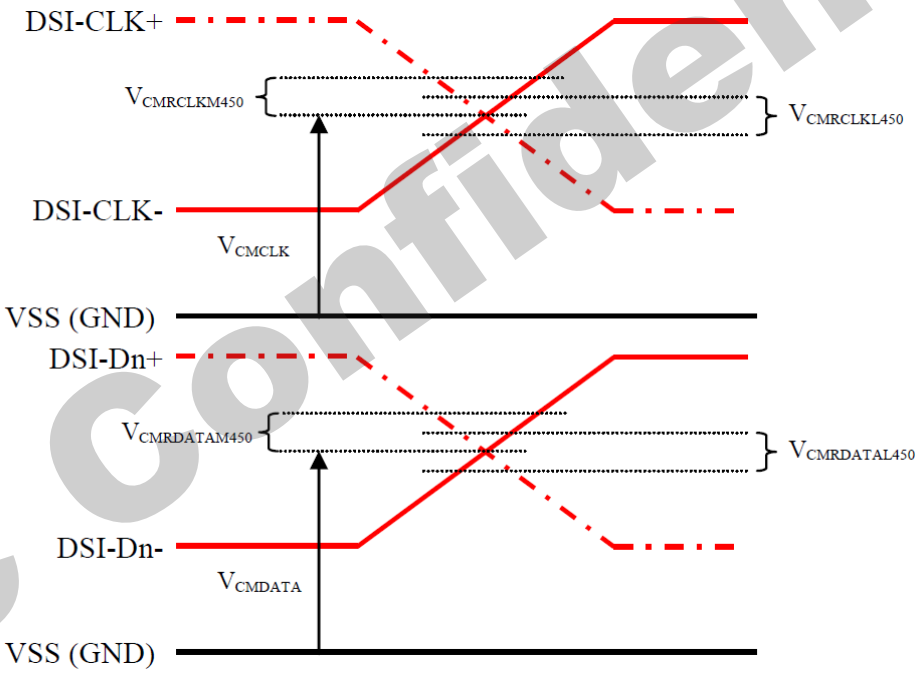


Figure 111 Differential Inputs Logical '0's and '1's, Threshold High/Low, Differential Voltage Range



Note: n = 0 and 1

Figure 112 Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs
  (DSI-CLK+ Ù DSI-CLK- or DSI-D0+ Ù DSI-D0- or DSI-D1+ Ù DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs
  (DSI-CLK+ Ù DSI-CLK- or DSI-D0+ Ù DSI-D0- or DSI-D1+ Ù DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

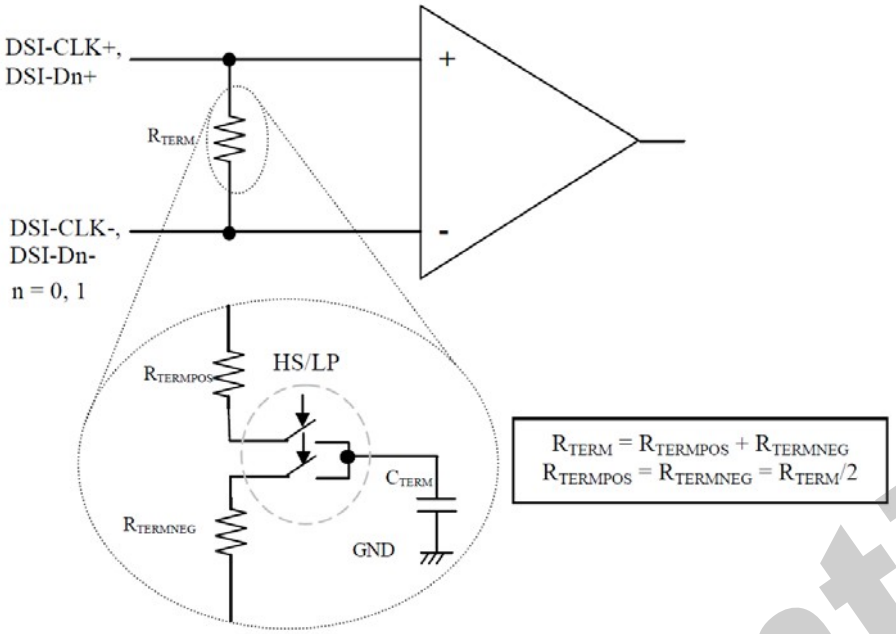


Figure 113 Differential Pair Termination Resistor on the Receiver Side

8.8. AC Characteristic

8.8.1.DSI Timing Characteristics

8.8.1.1. High Speed Mode – Clock Channel Timing

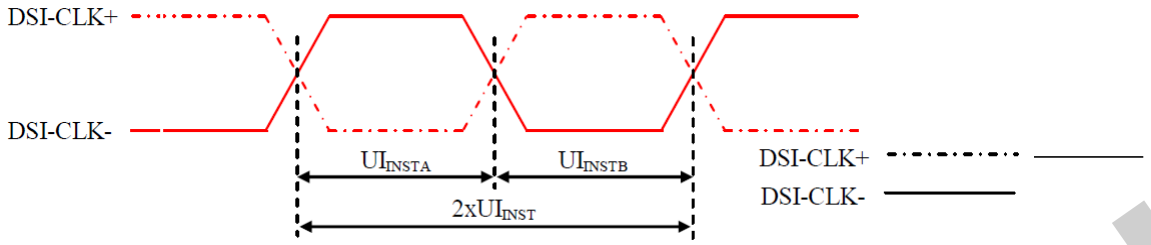


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

8.8.1.2. High Speed Mode – Data Clock Channel Timing

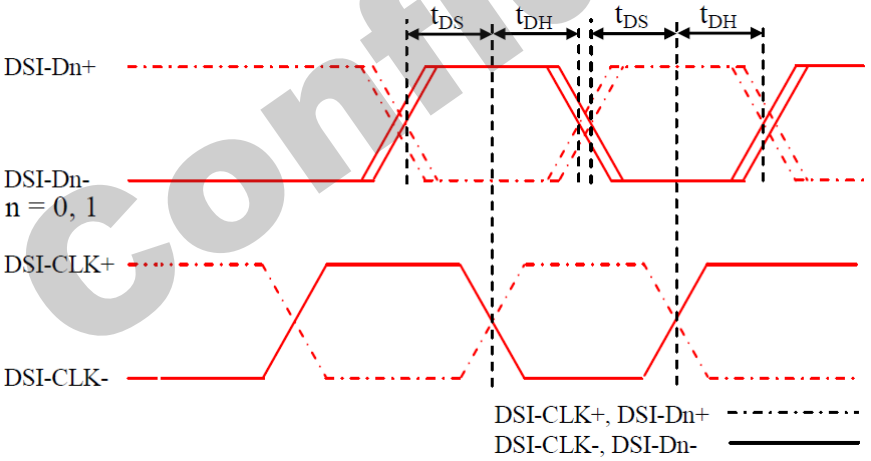


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

8.8.1.3. High Speed Mode – Rise and Fall Timings

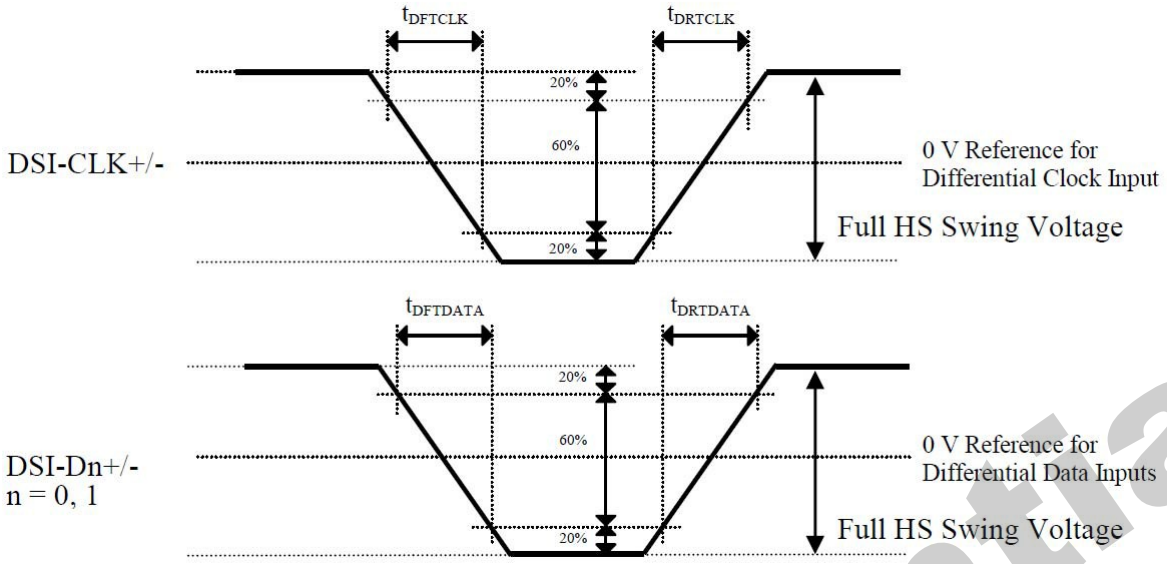


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

8.8.1.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9702C) sequence below.

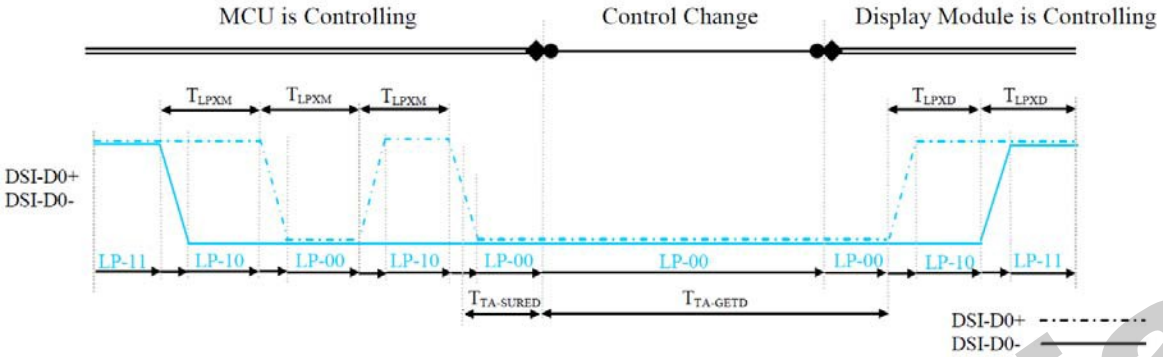


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (GC9702C) to the MPU sequence below.

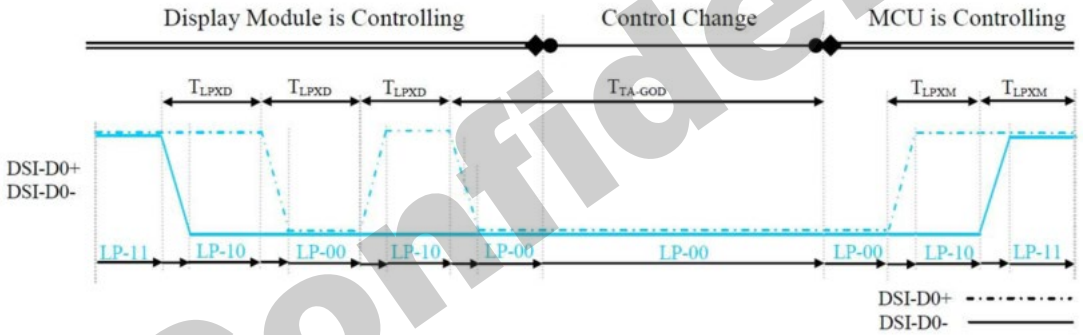


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ⬆ Display Module (GC9702C)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (GC9702C) ⬆ MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (GC9702C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DS-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (GC9702C)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4 \times T_{LPXD}$	ns

8.8.1.5. Data Lanes from Low Power Mode to High Speed Mode

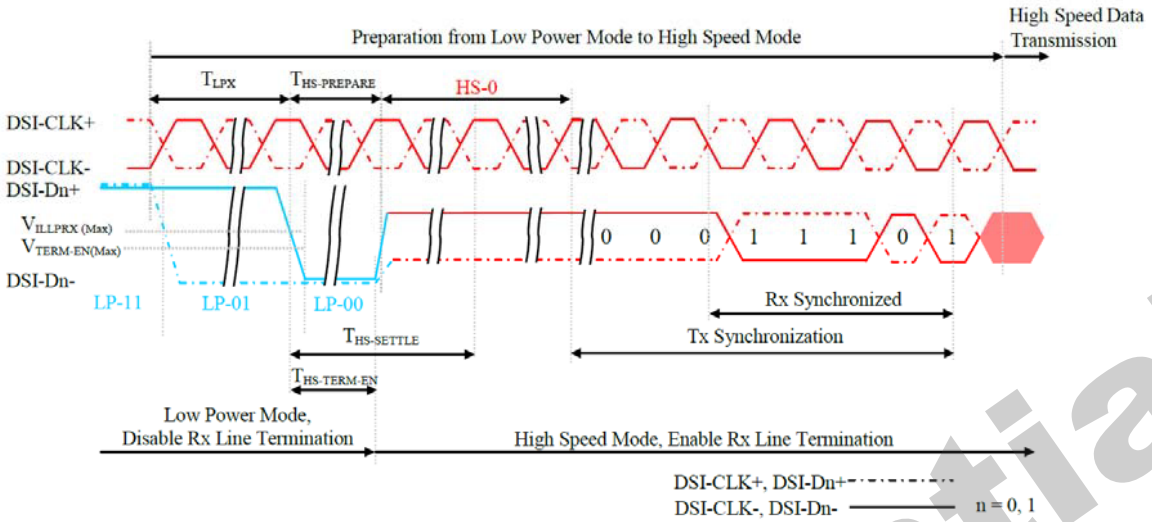


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

8.8.1.6. Data Lanes from High Speed Mode to Low Power Mode

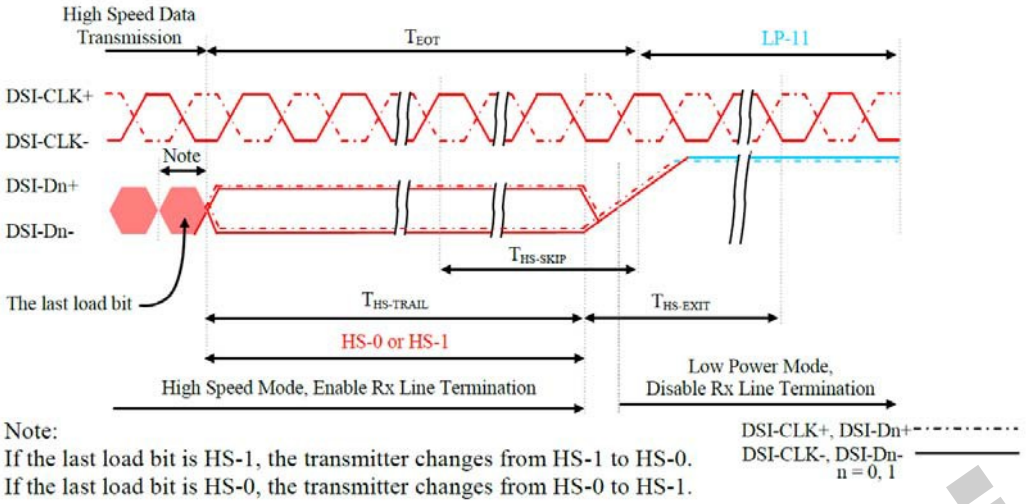


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (GC9702C) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

8.8.2. DSI Clock Burst – High Speed Mode to/from Low Power Mode

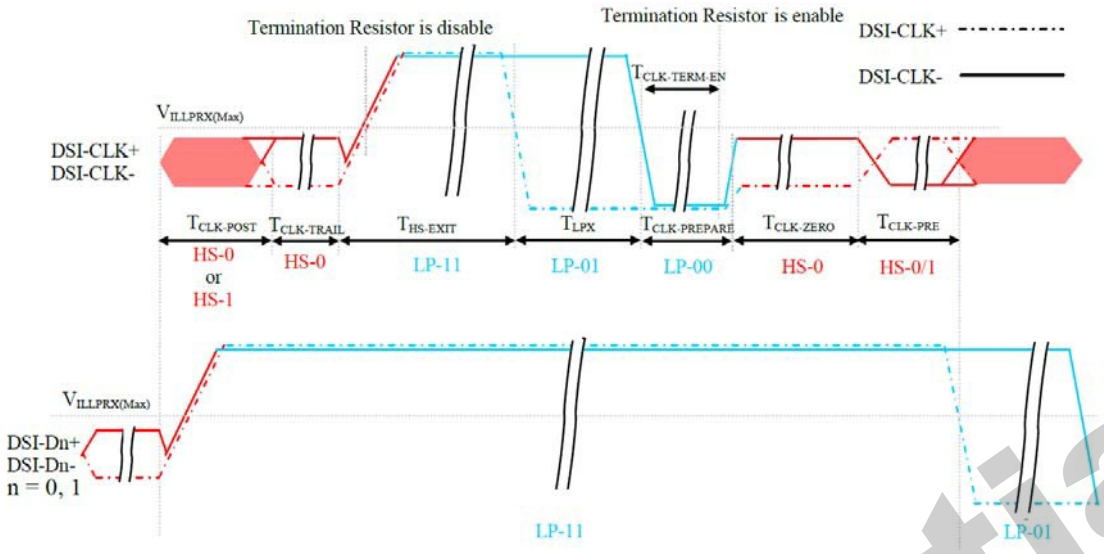


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
SI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns