

Osptek Display

AMOLED SPECIFICATION

Model No:

FLS-AM0178R585-A

osptek[®]

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1 Scope

This Specification defines AMOLED manufactured by Shenzhen Osprey Optoelectronics Technology Co., Ltd. , from here on refer as OSP. In the case of any unspecified item, it may require both OSP and the party designs this module into its product to work out a solution.

2 Features

2.1 Product Applications

Smart Watch(On-cell)

2.2 Product Features

- 1) Display color: 16.7M (RGB x 8bits)
- 2) Display format: 1.78”(368RGBx448)
- 3) Pixel arrangement: Real RGB arrangement
- 4) Interface: MIPI/SPI
- 5) Driver IC: SH8601A0 TP IC: CHSC5816

3 Mechanical Specifications

Item	Specification	unit
Panel outline	34.8*41.04	mm
LTPS Glass outline	30.6*37.99	mm
Number of dots	368(W) x RGB x 448(H)	dots
Active area	28.7*34.94	mm
Diagonal size	1.78	inch
Pixel pitch	78*78	μm
Glass thickness (LTPS/Encap. glass)	0.2 / 0.3	mm
Weight	TBD	g

4 Maximum Rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	5.5	V	-
I/O voltage	VDDIO	-0.3	-	5.5	V	-
Operating temperature	Top	-20	-	70	°C	-
Storage temperature	Tstg	-40	-	80	°C	-

5 Electrical Specifications

5.1 Electrical Characteristics

5.1.1 Power Characteristic:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	3.0	4.6	5.0	V	-
AMOLED power Negative	ELVSS	-4.0	-2.0	-0	V	Ref
Digital Power supply	VDDIO	1.65	1.8	3.3	V	Ref
Analog Power supply	VCI	2.7	2.8	3.6	V	Ref

1) Normal Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: $F_{frame}=60\text{HZ}$ @ 25degC, Brightness 500 nits, Command Mode,

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
100% Pixel On 500nits	IELVDD /ELVSS	-	27.9	-	mA	Ref
	IVCI	-	6	7.2	mA	Ref
	IVDDIO	-	2	2.4	mA	Ref

2) Idle Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: $F_{frame}=15\text{HZ}$ @ 25degC, Brightness:50nits, OPR:10%,Command Mode

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
10% Pixel On 50 nits	IELVDD /ELVSS	-	2.8	-	mA	Supplied by Driver IC
	IVCI	-	3.5	4.5	mA	Ref
	IVDDIO	-	1.2	1.5	mA	Ref

3) Deep Standby Mode

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
Deep Standby	IVCI	-	-	15	uA	-
	IVDDIO	-	-	4	uA	-
	Power Consumpti on	-	-	<50	uW	Ref

5.1.2 Driver IC

SH8601A.

5.2 TP IC Recommended Operating Conditions

Touch IC: CHSC5816(refer to the datasheet)

Symbol	Description	Min	TYP	MAX	UNIT
VCCA	Analog power supply voltage	2.7	2.8	3.6	V
V _{IN} (I2C)	Input voltage range	0	-	3.6	V
V _{OUT} (I2C)	Output voltage range	0	-	3.6	V
V _{IN} (INT)	Input voltage range	0	-	3.6	V
V _{OUT} (INT)	Output voltage range	0	-	3.6	V
V _{OUT} (TX)	Output voltage range	0	-	VCCA	V
V _{OUT} (RX)	Input voltage range	0	-	VCCA	V

The logo for Osprey Optoelectronics, featuring a stylized bird icon above the word "osptek" in a lowercase, sans-serif font with a registered trademark symbol.

Item	Spec	Remark
Operating voltage	2.7-3.6V	
Operating current	2mA	
Linearity	Center part \leq 1mm	Test tool: ϕ 7mm copper cylinder
	The peripheral position \leq 2mm	
Sensitivity	No broken line	Lineation with 5mm/s&20mm/s respectively by Φ 7mm copper cylinder
Response time	\leq 10ms	

5.3 I/O Connection

5.3.1 COF Bonding FPC PAD Define

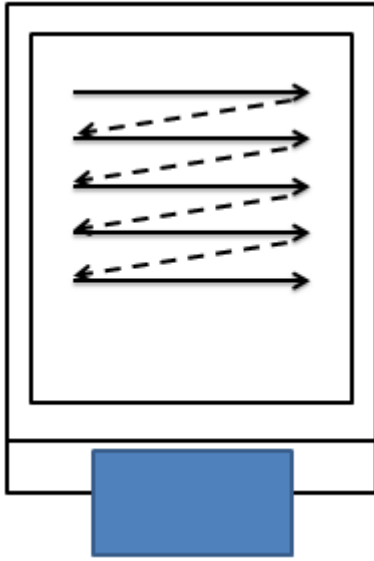
No.	Symbol	Function
1	NFC_ANT2	Near Field Communication Antenna 2
2	NFC_ANT1	Near Field Communication Antenna 1
3	GND	Ground
4	TP_INT(1.8V)	Touch IC's interrupt to Host
5	TP_SDA(1.8V)	Touch IC I2C data
6	TP_SCL(1.8V)	Touch IC I2C clock
7	TP_RESET(1.8V)	This signal will reset Touch IC.Signal is active low.
8	TP_VDD(3.3V)	Power supply for Touch IC
9	TP_VDD(3.3V)	Power supply for Touch IC
10	GND	Ground
11	CLKN	MIPI DSI clock lane-
12	CLKP	MIPI DSI clock lane+
13	GND	Ground
14	D0N	MIPI DSI data lane0-
15	D0P	MIPI DSI data lane0+

16	VDDIO(1.8V)	Power supply for I/O block provided from outside VDDI < 0.05V (When power is turned off)
17	VDDIO(1.8V)	Power supply for I/O block provided from outside VDDI < 0.05V (When power is turned off)
18	VCI_EN	Power Supply for Analog Circuits VCI < 0.05V (When power is turned off)
19	REST	Reset
20	TE	Tearing effect signal is used to synchronize MCU to frame memory
21	GND	Ground
22	QSPI_CLK	This pin is used to be serial interface clock
23	QSPI_S103	Serial input signal in QSPI serial data interface
24	QSPI_S102	Serial input signal in QSPI serial data interface
25	QSPI_S101	Serial input signal in QSPI serial data interface
26	QSPI_S100	Serial input signal in QSPI serial data interface
27	QSPI_CS	Chip selection pin ;Low enable ,high disable.
28	GND	Ground
29	IM1	
30	MTP_PWR	Power supply for OTP. Leave the pin to open when not in use.
31	VBAT(3.7V)	Power Supply for DC/DC Converter Circuit
32		This is the power supply pin for the internal buffer of the DC/DC voltage converter.It must be connected to external source when the converter is used.It should be connected to VDD when the converter is not used.
33		
34	GND	Ground
35	GND	Ground
36	GND	Ground

5.3.2 TP FPC connector pin Define

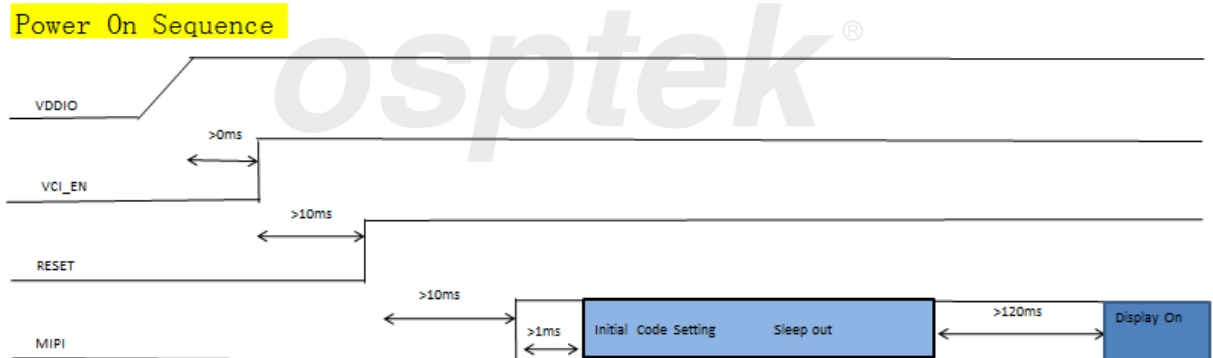
Pin No.	Symbol	I/O	Function Description	When not use
1	GND	-	GND	
2	TSP_INT	I	IIC interface	
3	TSP_SDA	Power	Power	
4	TSP_SCL	I	IIC interface	
5	TSP_VCC	Power	Power	
6	TSP_RESET	I/O	Interrupt	

5.4 Graphic memory writing direction



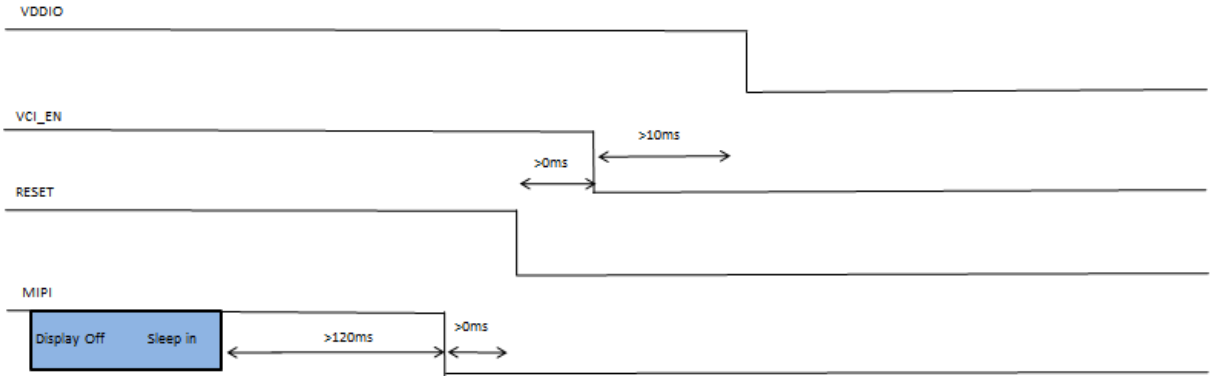
5.5 Recommended Operating Sequence

5.5.1 Power on sequence



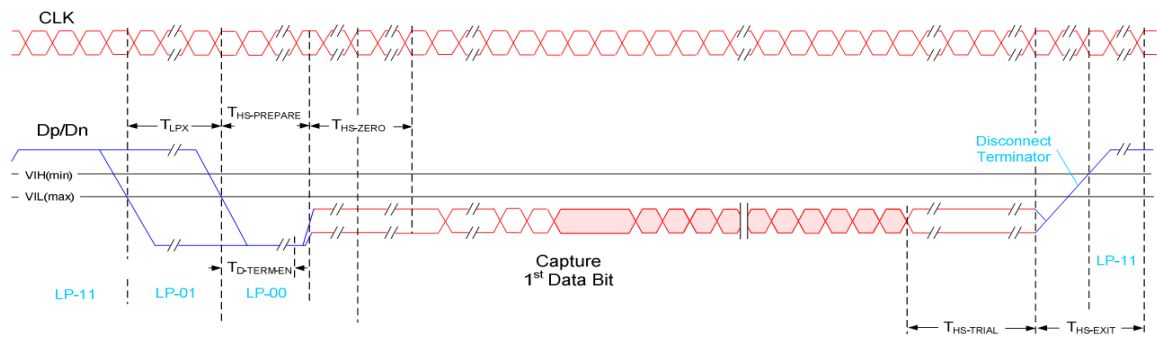
5.5.2 Power off sequence

Power Off Sequence

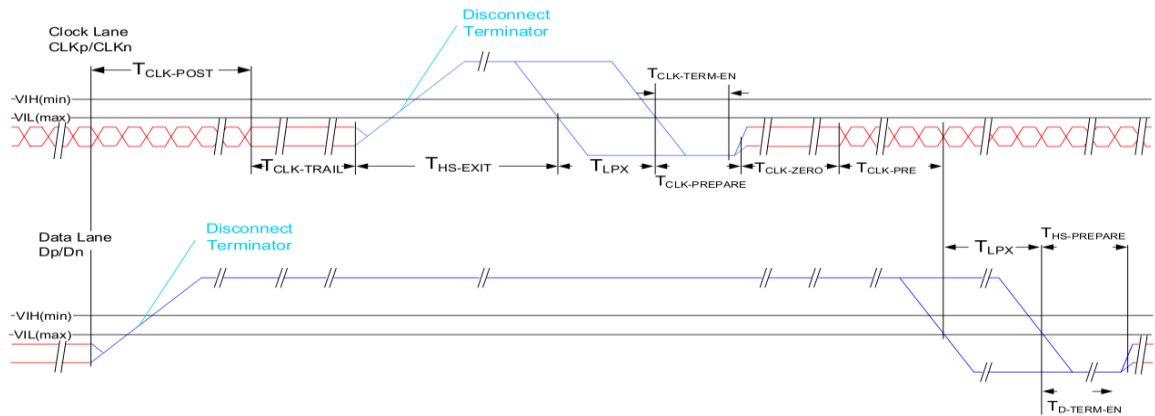


5.5.3 AC Characteristics (MIPI)

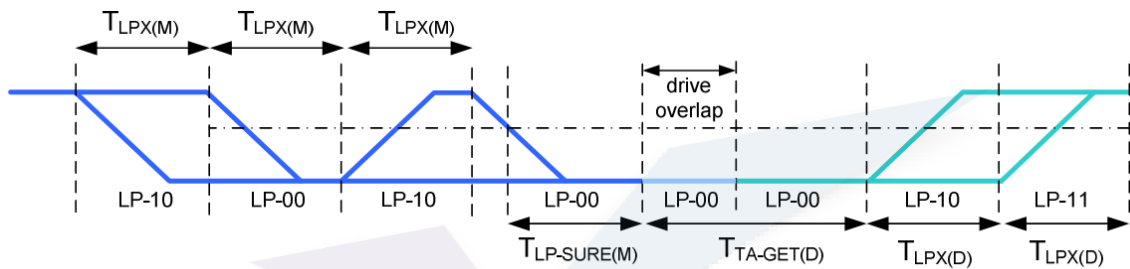
HS Data Transmission Burst



HS Clock Transmission



Turnaround Procedure



Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
TREOT	30%-85% rise time and fall time	-	-	35	ns
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
TCLK-POST*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60ns + 52*UI (For DCS)	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any	8	-	-	ns

	associated Data Lane beginning the transition from LP to HS mode.				
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE.	95	-	300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		38	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THSPREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
TEOT	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	-	-	105ns+48*UI	ns
THS-EXIT(1)	time to drive LP-11 after HS burst	100	-	-	ns
THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
TLPX	Length of any Low-Power state period	50	-	-	ns

Ratio TLPX	Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side	2/3	-	3/2	ns
TTA-GET	Time to drive LP-00 by new TX	5*TLPX	5*TLPX	5*TLPX	ns
TTA-GO	Time to drive LP-00 after Turnaround Request	4*TLPX	4*TLPX	4*TLPX	ns
TTA-SURE	Time-out before new TX side starts driving	TLPX	-	2*TLPX	ns

Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.

When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, TA=-20°C~+70°C)

Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table: Reset timing



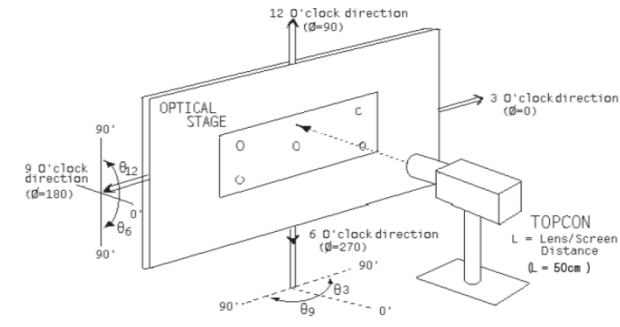
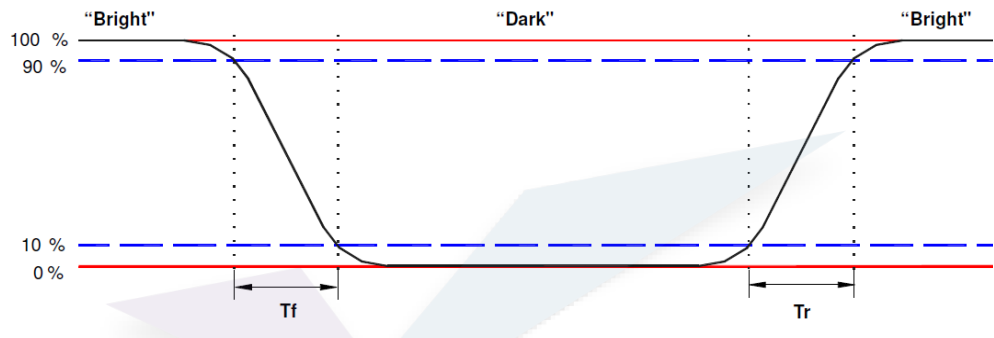
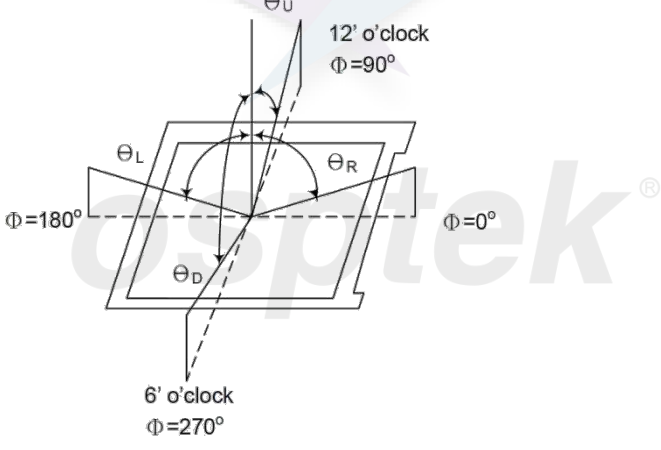
6 Electro-Optical Specification

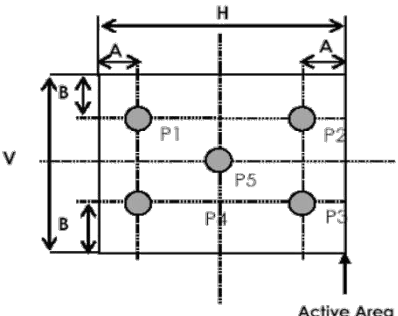
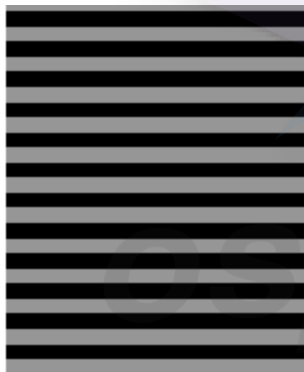
Test condition: 25°C±3°C, 65±20%RH, darkroom.

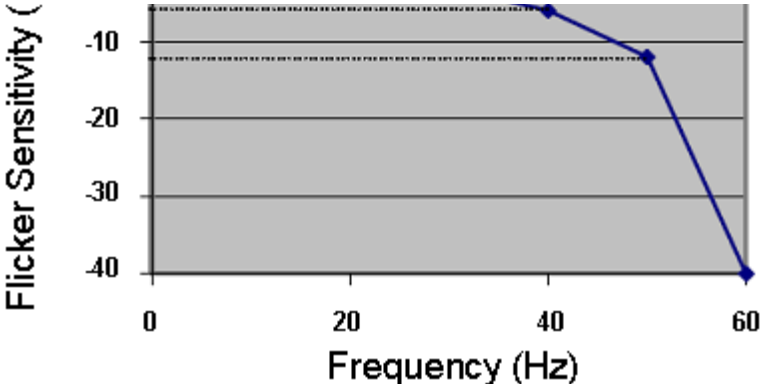
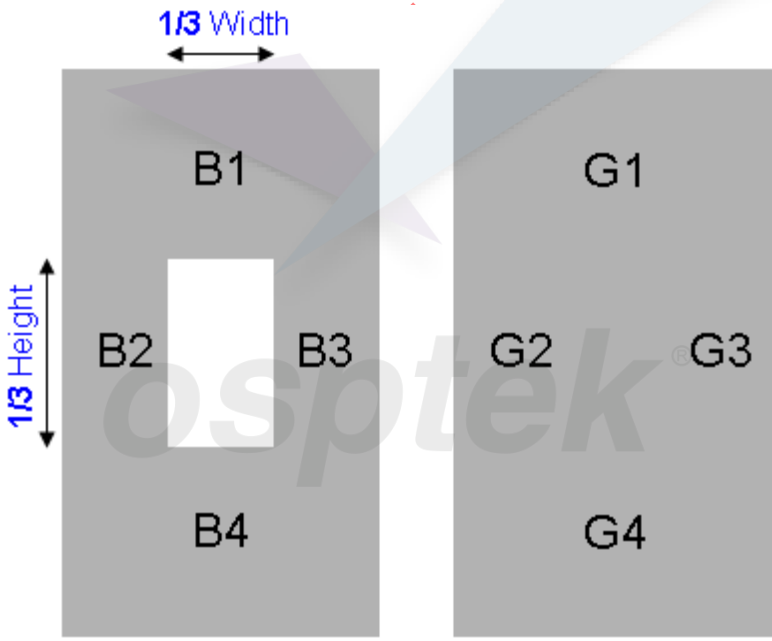
No	Item	Symbol	Condition	Value			Unit	Remark
				Min.	Typ.	Max.		
1	Brightness	L	Full white Without CG	450	500	550	cd/m ²	Note1.
2	Brightness Uniformity	UL	Full white	80	85	-	%	Note4
3	Contrast Ratio	CR	Normal θ=Φ=0°	10000	100000	-	-	Note3.

4	Response time		Ton+Toff	Normal $\Theta=\Phi=0^\circ$	-	2	4	ms	Note2.
5	Color Coordinate of CIE1931	White	X	Normal $\Theta=\Phi=0^\circ$	0.27	0.29	0.31	-	Note1.
			Y		0.29	0.31	0.33		
		Red	X		0.647	0.687	0.727		
			Y		0.272	0.312	0.352		
		Green	X		0.175	0.225	0.275		
			Y		0.679	0.729	0.779		
		Blue	X		0.102	0.143	0.183		
			Y		0.002	0.043	0.083		
6	Color Gamut		NTSC	CIE1931	90	105	-	%	
7	Viewing Angle			Top/Bottom/Right/Left CR ratio ≥ 1000	80			°	Note3.
8	Gamma			$\text{Log}(L_v - L_b) = \log(V) + \log(a)$ $V(\text{Gray}) = 48, 72, 104, 132, 164, 192, 224$ $\text{Lum}(\text{gray}255) = 350\text{nit}$	2.0	2.2	2.4	-	
9	Flicker			Normal $\Theta=\Phi=0^\circ$	-	-35 [®]	-30	dB	Note6.
10	Crosstalk			-	-	-	4	%	Note7.
11	Color shift			$\Theta_L = 30^\circ$			6		
12	OLED Life Time			0.95*(TYP brightness) At 25°C, with white color pattern	150			hrs	Note8.
13	Image Retention			With 8*8 black-white chess board test image, lighting on with maximum luminance for 10min	8*8 black-white chess board 10min, to G128, 20s disappear				

See the note in the table below:

No	Item	Details
Note1	Brightne ss	
Note 2	Respons e time	
Note 3	Viewing Angle	 <p>Contrast Ratio Dark Room C.R=LW/LB LW: full white brightness of display center P0; LB: full black brightness of display center P0.</p>
Note 4	Brightne ss	

	Uniformity	 <p>A: 1/4H B: 1/4V H.V: Active Area</p>
Note 5	Luminance decrease ration	<p>Definition of Luminance decrease ratio Test pattern : Full White The luminance decrease ratio is calculated by using following formula:</p> $\text{Luminance decrease ratio} = 1 - \frac{\text{Luminance test at left, right, top, bottom :}}{\text{Luminance test at left, right, top, bottom}}$
Note 6	Flicker	<p>Suggested Instruments: Konica Minolta CA-310 or Klein Instruments K-8</p>  <p>Odd row : L0 Black Even row : L186 gray level</p> <p>Flicker Test Pattern</p> <p>The flicker level is defined by Fast Fourier Transformation (FFT) as follows:</p> $\text{Flicker} = 20 \log_{10} \left(2 \frac{f_{FFTC}(n)}{f_{FFTC}(0)} \right) + FS(Hz) \quad (\text{dB})$ <p>Where fFFTC(n) is the n-th FFT coefficient. fFFTC(0) is the 0-th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency. The peak flicker level shall be reported based on the calculation using above formula in which FS(Hz) is determined by the flicker weighing factor shown below.</p>

		
Note 7	Crosstalk	<p>Crosstalk shall be calculated by the luminance of B1~B4 and G1~G4 in the patterns shown below.</p> <p>Box Pattern: L128 gray level background with a L255 White window in the central area.</p> <p>Gray Pattern: L128 gray level background only.</p>  <p style="text-align: center;">Box Pattern Gray Pattern</p> <p><i>Crosstalk</i></p> $\equiv \text{Maximum} : \left\{ \frac{ B1 - G1 }{G1}, \frac{ B2 - G2 }{G2}, \frac{ B3 - G3 }{G3}, \frac{ B4 - G4 }{G4} \right\} \times 100\%$
Note 8	Life Time	<p>OLED life time is defined by the Minimum Duration Time that the luminance is decayed to a specific ratio (ex. 92%) of initial state.</p> <p>Test Pattern under duration period: L255 White</p>

7 Reliability

7.1 Environmental Test

Item	Main spec	No. of failures / No. of examinations
High Temperature Operation	70°C / 240hrs	0/10
Low Temperature Operation	-20°C / 240hrs	0/10
High Temperature Storage	80°C / 240hrs	0/10
Low Temperature Storage	-40°C / 240hrs	0/10
High Temperature Humidity Operation	60°C/90%RH/ 240hrs	0/32
Thermal Shock	-40°C~85°C dwell time=0.5hr, 100cycles.	0/10

7.2 Electrical Test

Item	Main spec	Note
Air Discharge	±4 kV , 150pF/330Ω (Module level; without CG)	5Points, Each 10times. After one time discharge, panel and gun touch the ground, through the whole test, turn on ion fan. No degradation of OLED performance after this test.
Contact Discharge	±2kV, 150pF/330Ω (Module level; without CG)	

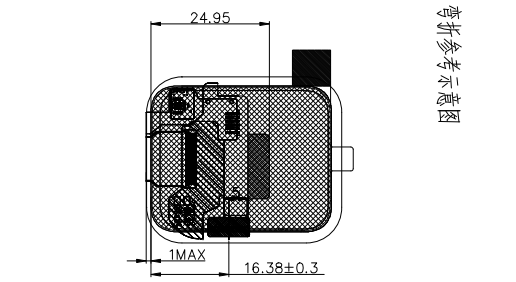
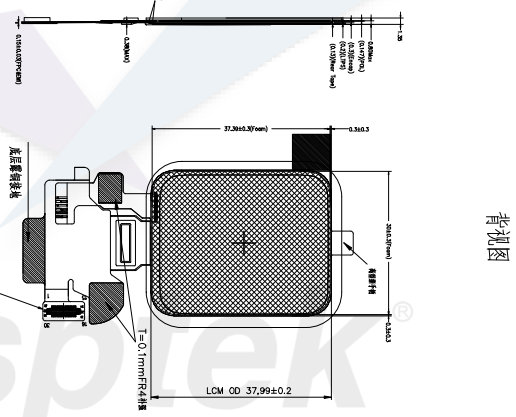
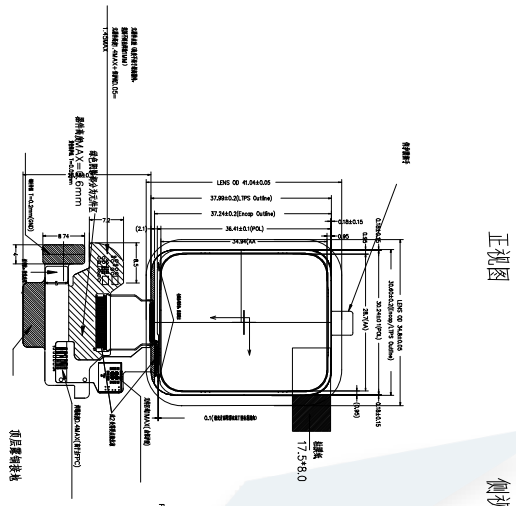
7.3 Mechanical Test

Test item	Test condition	Note
Packing vibration-proof test	2g, f=10->55->10Hz apply in each of X, Y, and Z direction for 30 min	Package
Packing Drop test	Drop the packing from 60cm height, 6-faces, 3-edges and 1-corner(one time for each)	Package

8 Outline Dimension Drawing

客户(customer):
客户单位名称:
Customer signature:

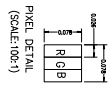
REV.	DESCRIPTION	DATE
A	New	20220528



零件参考示意图

No.	Symbol	Part Name
1	REF. PART	REF. PART
2	REF. PART	REF. PART
3	REF. PART	REF. PART
4	REF. PART	REF. PART
5	REF. PART	REF. PART
6	REF. PART	REF. PART
7	REF. PART	REF. PART
8	REF. PART	REF. PART
9	REF. PART	REF. PART
10	REF. PART	REF. PART
11	REF. PART	REF. PART
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28	REF. PART	REF. PART
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30	REF. PART	REF. PART
31	REF. PART	REF. PART
32	REF. PART	REF. PART
33	REF. PART	REF. PART
34	REF. PART	REF. PART
35	REF. PART	REF. PART
36	REF. PART	REF. PART

- NOTES:
1. OPERATING TEMPERATURE: -10°C TO 60°C
 2. STORAGE TEMPERATURE: : -20°C TO 70°C
 3. DRIVING IC: SH8601A
TP IC: CH5C5816
 4. DISPLAY MODEL: TPS-AMOLED
 5. GENERAL TOLERANCE: ±0.20mm
 6. MEANS DIMENSION FOR REFERENCE
 7. SPECIAL REQUIREMENT: NO
 8. WITH (*) MARK DIMENSIONS ARE IMPORTANT DIMENSIONS.
 9. WITH (**) MARK DIMENSIONS ARE REFERENCE DIMENSIONS.
 9. REQUIREMENTS ON ENVIRONMENTAL PROTECTION: ROHS.



APPROVALS	DATE	SCALE	TITLE
DRAWN:		1:1	MODULE
CHECK:		mm	
APPROVAL:			

深圳市鱼鹰光电科技有限公司
Shenzhen Osprey Optoelectronics Technology Co., Ltd.

DWG NO: A PAGE: 1/1

9 Packing Specification

TBD

10 The Control of Hazardous Substances

The control of Hazardous substances refer to OSP document 《有害物质管控标准书》 (Standard document for the Control of Hazardous substances) OSP -IS- 110, the latest version.

