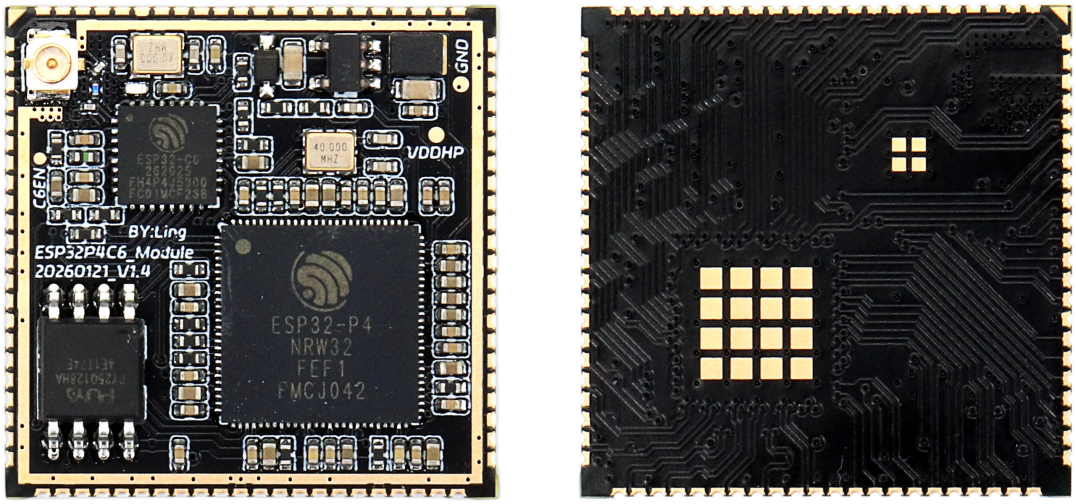


ESP32-P4C6-Core

Technical Specification

Revision History

Version	Date	Established/Revised Content	Author/Modifier	Approver

Table of Contents

1.Overview

1.1. Product Introduction

The ESP32-P4C6-Core is a compact stamp-pin core board integrating NOR FLASH, designed around Espressif's ESP32-P4 chip. The core processor chip ESP32-P4 incorporates either 32MB of PSRAM within its package, featuring two high-performance (HP) cores and one low-power (LP) core.The HP cores utilise a dual-core RISC-V processor operating at up to 360MHz,incorporating a JPEG codec, pixel processing accelerator, H.264 video encoder, and MIPIinterface; delivering robust image and voice processing capabilities.

1.2. Functional Features

· Dual-core 360 MHz high-frequency CPU.

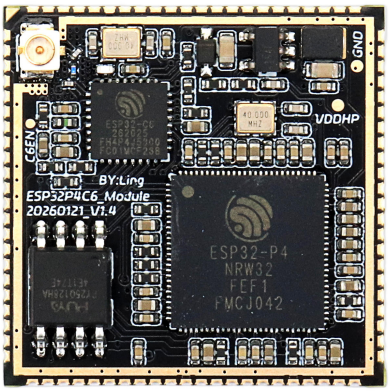
· Integrated 16 MB Flash and 32 MB Psram.

· Full pinout of the ESP32-P4 chip.

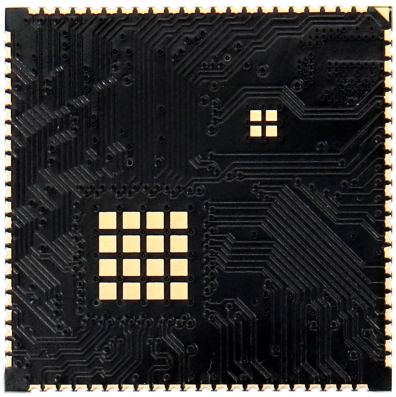
· Compact core board size for streamlined hardware design.

· Comprehensive development documentation provided.

1.3. Product Images



Front view



Rear view

1.4. Application Scenarios

· Smart home systems

· Industrial Automation

· Consumer Electronics

· HMI (Human-Machine Interface)

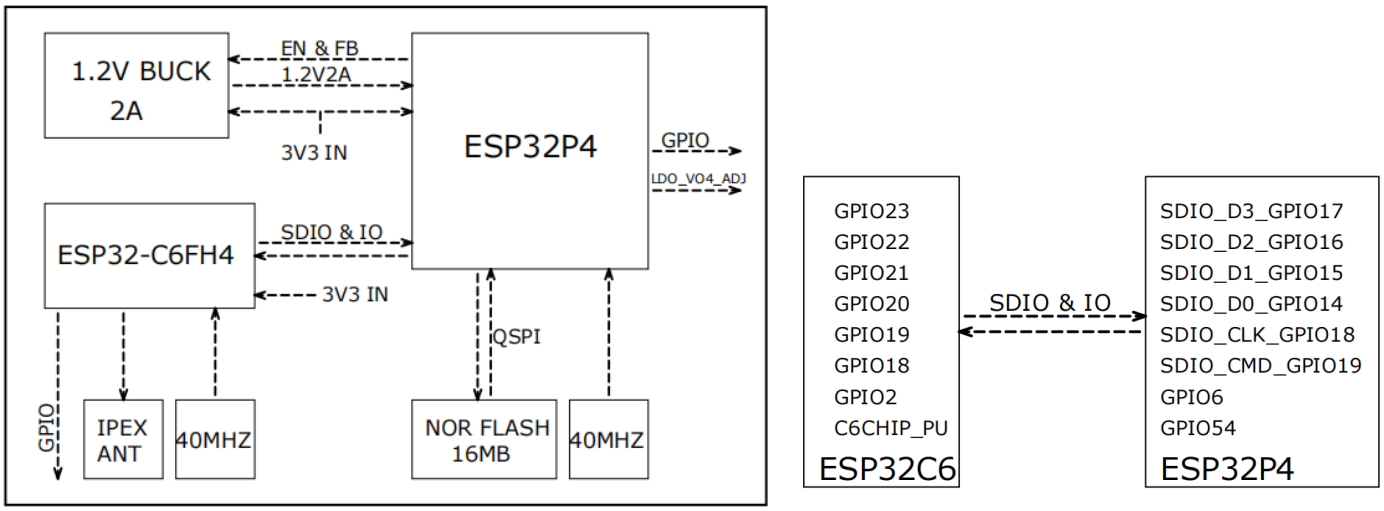
· Electronic Robotics

· Camera video streaming

· USB Devices

2. Product Specifications

2.1. Functional Block Diagram



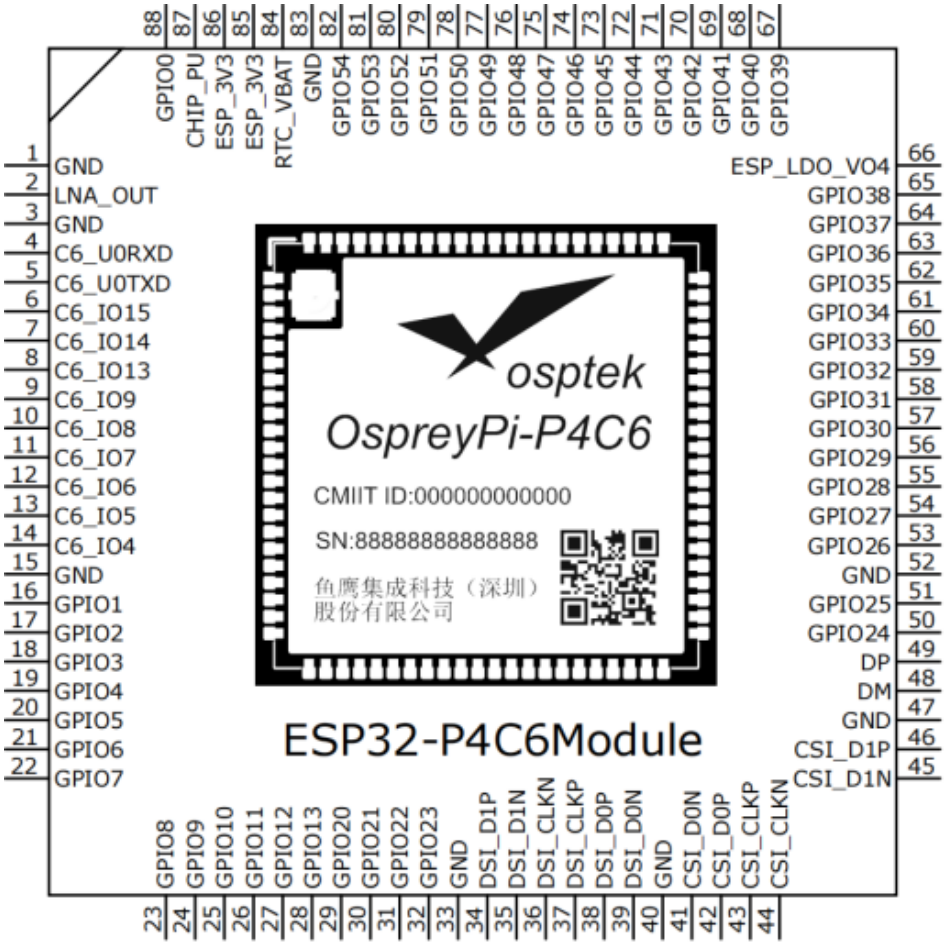
2.2 Hardware Specifications

Main Controller	CPU	ESP32-P4
	Core	RISC-V 32-bit dual-core processor
	Clock Speed	360 MHz (High Performance system)
		40 MHz (LP system)
Memory	ROM	128 KB HP ROM
		16 KB LP ROM
	SRAM	768 KB High-Performance L2 Memory
		32 KB Low-Power SRAM
	Flash	16MB
Peripheral Interface	GPIO	55
	SPI	2

	LP SPI	1
	UART	5
	LP UART	1
	I3C	1
	I2C	2
	LP I2C	1
	I2S	3
	LP I2S	1
	USB JTAG	1
	SDIO	1
	LED PWM	1
	MCPWM	2
	TWAI Controller (ISO 11898-1 compliant)	3
	High-Speed USB 2.0 OTG	1
	Full-Speed USB 2.0 OTG	1
	100Mbps Ethernet MAC	1
	MIPI CST-2	1
	MIPI DSI	1
	Parallel I/O (PARLIO) Controller	1
	12-bit Multi-Channel Analogue-to-Digital Converter	2
	Temperature Sensor	1
	Touch sensor	1
	Analogue Voltage Comparator	1
	Undervoltage Monitoring	1
Image and Voice Processing Interface	JPEG Encoder/Decoder	1
	Pixel Processing Accelerator (PPA)	1
	Image Signal Processor (ISP)	1
	H.264 Video Encoder	1

3. Pin Definitions

3.1. Pin Layout



3.2. Pin Descriptions

Pin	Name	Description
1	GND	Power Ground
2	LAN_OUT	ESP32-C6FH4's ANT, IPEX1 generation antenna interface
3	GND	Power ground
4	C6_U0RXD	ESP32-C6FH4's U0RXD (ESP32-C6 programming pin)
5	C6_U0TXD	ESP32-C6FH4's U0TXD (ESP32-C6 programming pin)
6	C6_IO15	ESP32-C6FH4's GPIO15
7	C6_IO14	ESP32-C6FH4's GPIO14
8	C6_IO13	ESP32-C6FH4's GPIO13
9	C6_IO9	ESP32-C6FH4's GPIO9 (ESP32-C6 strapping pin)

10	C6_IO8	ESP32-C6FH4's GPIO8, with an internal 10K pull-up resistor (ESP32-C6 strapping pin)
11	C6_IO7	ESP32-C6FH4's GPIO7
12	C6_IO6	ESP32-C6FH4's GPIO6
13	C6_IO5	ESP32-C6FH4's GPIO5
14	C6_IO4	ESP32-C6FH4's GPIO4
15	GND	Power ground
16	GPIO1	GPIO1, LP_GPIO1, XTAL_32K_P
17	GPIO2	GPIO2, MTCK, LP_GPIO2, TOUCH_CHANNEL0
18	GPIO3	GPIO3, MTDI, LP_GPIO3, TOUCH_CHANNEL1
19	GPIO4	GPIO4, MTMS, LP_GPIO4, TOUCH_CHANNEL2
20	GPIO5	GPIO5, MTDO, LP_GPIO5, TOUCH_CHANNEL3
21	GPIO6	GPIO6, SPI2_HOLD_PAD, LP_GPIO6, TOUCH_CHANNEL4
22	GPIO7	GPIO7, SPI2_CS_PAD, LP_GPIO7, TOUCH_CHANNEL5
23	GPIO8	GPIO8, UART0_RTS_PAD, SPI2_D_PAD, LP_GPIO8, TOUCH_CHANNEL6
24	GPIO9	GPIO9, UART0_CTS_PAD, SPI2_CK_PAD, LP_GPIO9, TOUCH_CHANNEL7
25	GPIO10	GPIO10, UART1_TXD_PAD, SPI2_Q_PAD, LP_GPIO10, TOUCH_CHANNEL8
26	GPIO11	GPIO11, UART1_RXD_PAD, SPI2_WP_PAD, LP_GPIO11, TOUCH_CHANNEL9
27	GPIO12	GPIO12, LP_GPIO12, TOUCH_CHANNEL10
28	GPIO13	GPIO13, LP_GPIO13, TOUCH_CHANNEL11
29	GPIO20	GPIO20, ADC1_CHANNEL4
30	GPIO21	GPIO21, ADC1_CHANNEL5
31	GPIO22	GPIO22, ADC1_CHANNEL6
32	GPIO23	GPIO23, ADC1_CHANNEL7, REF_50M_CLK_PAD
33	GND	Power ground
34	DSI_D1P	MIPI DSI PHY DATA P1
35	DSI_D1N	MIPI DSI PHY DATA N1
36	DSI_CLKN	MIPI DSI PHY CLOCK
37	DSI_CLKP	MIPI DSI PHY CLKP
38	DSI_D0P	MIPI DSI PHY DATAP0
39	DSI_D0N	MIPI DSI PHY DATA N0
40	GND	Power Ground
41	CSI_D0N	MIPI CSI PHY Data 0
42	CSI_D0P	MIPI CSI PHY DATA P0

43	CSI_CLKP	MIPI CSI PHY CLKP
44	CSI_CLKN	MIPI CSI PHY CLKN
45	CSI_D1N	MIPI CSI PHY DATA N1
46	CSI_D1P	MIPI CSI PHY DATA P1
47	GND	Power Ground
48	DM	USB2 OTG PHY Data Mask
49	DP	USB2 OTG PHY DP
50	GPIO24	GPIO24, USB1P1_N0
51	GPIO25	GPIO25, USB1P1_P0
52	GND	Power Ground
53	GPIO26	GPIO26, USB1P1_N1
54	GPIO27	GPIO27, USB1P1_P1
55	GPIO28	GPIO28, SPI2_CS_PAD, GMAC_PHY_RXDV_PAD
56	GPIO29	GPIO29, SPI2_D_PAD, GMAC_PHY_RXD0_PAD
57	GPIO30	GPIO30, SPI2_CK_PAD, GMAC_PHY_RXD1_PAD
58	GPIO31	GPIO31, SPI2_Q_PAD, GMAC_PHY_RXER_PAD
59	GPIO32	GPIO32, SPI2_HOLD_PAD, GMAC_RMII_CLK_PAD
60	GPIO33	GPIO33, SPI2_WP_PAD, GMAC_PHY_TXEN_PAD
61	GPIO34	GPIO34, SPI2_IO4_PAD, GMAC_PHY_TXD0_PAD
62	GPIO35	GPIO35, SPI2_IO5_PAD, GMAC_PHY_TXD1_PAD (no pull-up internally within the module)
63	GPIO36	GPIO36, SPI2_IO6_PAD, GMAC_PHY_TXER_PAD (no pull-up internally within the module)
64	GPIO37	GPIO37, UART0_TXD_PAD, SPI2_IO7_PAD (ESP32-P4 programming pin)
65	GPIO38	GPIO38, UART0_RXD_PAD, SPI2_DQS_PAD (ESP32-P4 programming pin)
66	ESP_LDO_VO4	Output power supply (output voltage range 0.5–2.7V or 3.3V, maximum output current 0.2A)
67	GPIO39	GPIO39, SD1_CDATA0_PAD, REF_50M_CLK_PAD
68	GPIO40	GPIO40, SD1_CDATA1_PAD, GMAC_PHY_TXEN_PAD
69	GPIO41	GPIO41, SD1_CDATA2_PAD, GMAC_PHY_TXD0_PAD
70	GPIO42	GPIO42, SD1_CDATA3_PAD, GMAC_PHY_TXD1_PAD
71	GPIO43	GPIO43, SD1_CCLK_PAD, GMAC_PHY_TXER_PAD
72	GPIO44	GPIO44, SD1_CCMD_PAD, GMAC_RMII_CLK_PAD
73	GPIO45	GPIO45, SD1_CDATA4_PAD, GMAC_PHY_RXDV_PAD

74	GPIO46	GPIO46, SD1_CDATA5_PAD, GMAC_PHY_RXD0_PAD
75	GPIO47	GPIO47, SD1_CDATA6_PAD, GMAC_PHY_RXD1_PAD
76	GPIO48	GPIO48, SD1_CDATA7_PAD, GMAC_PHY_RXER_PAD
77	GPIO49	GPIO49, GMAC_PHY_TXEN_PAD, ADC2_CHANNEL0
78	GPIO50	GPIO50, GMAC_RMII_CLK_PAD, ADC2_CHANNEL1
79	GPIO51	GPIO51, GMAC_PHY_RXDV_PAD, ADC2_CHANNEL2, ANA_COMP0
80	GPIO52	GPIO52, GMAC_PHY_RXD0_PAD, ADC2_CHANNEL3, ANA_COMP0
81	GPIO53	GPIO53, GMAC_PHY_RXD1_PAD, ADC2_CHANNEL4, ANA_COMP1
82	GPIO54	GPIO54, GMAC_PHY_RXER_PAD, ADC2_CHANNEL5, ANA_COMP1
83	GND	Power ground
84	RTC_VBAT	The backup power supply pin must not be left floating. The voltage range is 2.3V to 3.6V (can be connected to a 3.3V supply).
85	ESP_3V3	Power supply (3.3V input for core board power)
86	ESP_3V3	Power supply (3.3V input for core board power supply)
87	CHIP_PU	Enables ESP32-P4 chip (no internal RC reset; external reset required)
88	GPIO0	GPIO0, LP_GPIO0, XTAL_32K_N

3.3. Boot Configuration

3.3.1. Strapping Pins

Upon power-up or hardware reset, the following boot parameters may be configured via the strapping pin and eFuse bits without microprocessor involvement:

· Chip startup mode

- Strapping pins: GPIO35, GPIO36, GPIO37, GPIO38

· ROM log printing

- Strapping pins: GPIO36
- eFuse bit: EFUSE UART PRINT CONTROL

· JTAG Signal Source

- Strapping pin: GPIO34
- eFuse Bits: EFUSE_DIS_PAD_JTAG, EFUSE DIS USB JTAG, and EFUSE_JTAG_SEL_ENABLE The default values for the aforementioned eFuse bits are all 0, meaning they have not been programmed.

eFuses can only be programmed once; once set to 1, they cannot be restored to 0.

If the aforementioned strapping pins are not connected to any circuitry or if the connected circuitry is in a high-impedance state, their default value (i.e., logic level) depends on the state of

the internal weak pull-up/pull-down resistors during reset.

Default configuration of strapping pins

Strapping Pin	Default Configuration	Value
GPIO34	Floating	-
GPIO35	Weak pull-up	1
GPIO36	Floating	-
GPIO37	Floating	-
GPIO38	Floating	-

To alter the strapping pin's value, an external pull-down/pull-up resistor may be connected. When the ESP32-P4 operates as a slave device to a host MCU, the strapping pin's level may also be controlled by the host MCU.

All strapping pins feature latches. During system reset, the latches sample and store the corresponding strapping pin values, maintaining these until the chip is powered down or disabled. The latch state cannot be altered by other means. Consequently, strapping pin values remain readable throughout chip operation, and strapping pins function as standard I/O pins after chip reset.

3.3.2. Chip Start-up Mode Control

Upon reset release, GPIO35 to GPIO38 collectively determine the start-up mode. Refer to the table below for details.

Start-up Mode	GPIO35	GPIO36	GPIO37	GPIO38
SPI Boot*	1*	Any value	Any value	Any value
Joint Download Boot	0	1	Any value	Any value

Indicates default values and default configuration.

The following download methods are supported in Joint Download Boot mode:

USB Download Boot:

- USB-Serial-JTAG Download Boot
- USB 2.0 OTG Download Boot

· UART Download Boot

· SPI Slave Download Boot

3.3.3. ROM Log Printing Control

During system boot, ROM code logs may be printed to:

· (Default) UARTO and USB serial port/JTAG controller

· USB serial port/JTAG controller

· UARTO

EFUSE_UART_PRINT_CONTROL and GPIO36 govern UARTO ROM log printing; refer to the table below for details

UARTO ROM Log Printing	EFUSE_UART_PRINT_CONTROL	GPIO37
Enable	0*	Ignore
	1	0
	2	1
Close	1	1
	2	0
	3	Ignore

*Indicates default values and default configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT Controls USB serial/JTAG controller ROM log printing; see table below for details.

USB Serial/JTAG ROM Log Printing Control	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enable*	0*
Disable	1

*Indicates default value and default configuration

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Exceeding absolute maximum ratings may cause permanent damage to the device. These are merely emphasised ratings and do not imply functional operation of the device beyond these or other conditions specified in this technical specification. Prolonged exposure to absolute maximum ratings may affect the reliability of the ESP32-P4C6-Core.

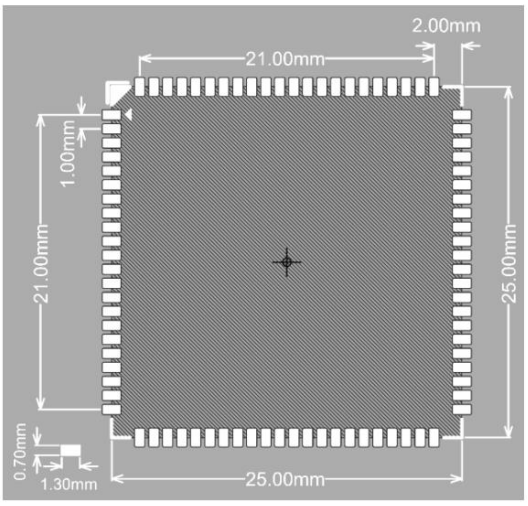
4.2. Power Consumption Characteristics

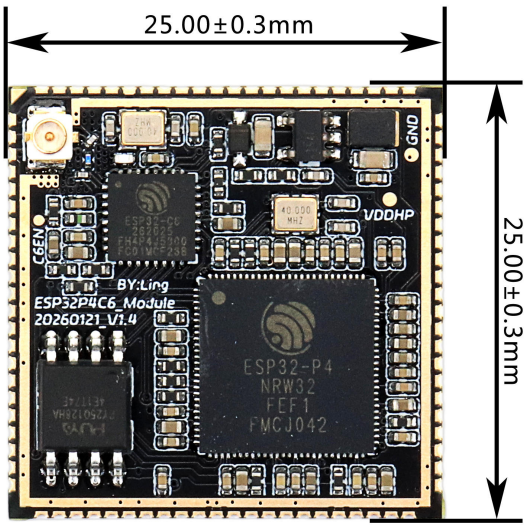
Symbol	Parameter	Minimum	Typical	Maximum	Unit
VCC	Power supply pin voltage	3.0	3.3	3.6	V
IVCC	External power supply current	-	1	-	A
TA	Operating ambient temperature	-40	-	85	° C

5. Schematic Diagram

Not available

6. Product Dimensions





7. Storage Conditions

Conditions	Parameters
Storage Conditions	Sealed MBB, non-condensing atmospheric environment at {<}40°C/90% RH
Operating Conditions	Within 168 hours at 25±5°C and 60% RH
Moisture Sensitivity	Level 3

8. Reflow soldering profile