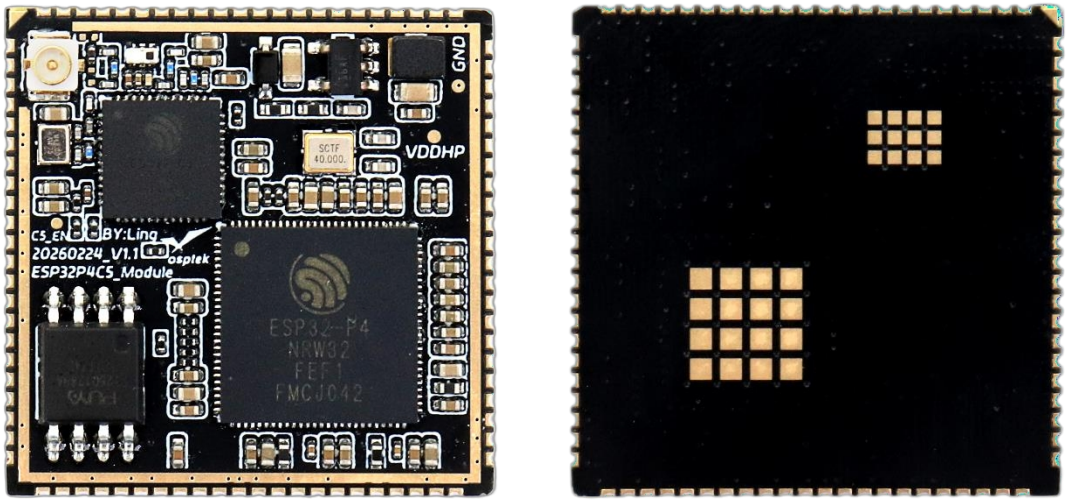



# ESP32-P4C5-Core Development Board

## Technical Specifications

## Revision History

| Version | Date | Content created/amended | Author/Reviser | Reviewer |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |

# Table of Contents

# 1. Overview

## 1.1. Product Overview

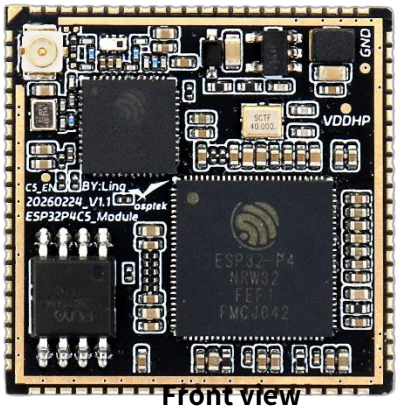
The ESP32-P4C5-Core is a compact, pin-pitch core board with integrated NOR FLASH, designed based on the Espressif ESP32-P4 chip.The core processor chip, the ESP32-P4, features 32MB of on-chip PSRAM and comprises two high-performance (HP) cores and one low-power (LP) core. The HP cores utilise a RISC-V dual-core processor with a clock speed of up to 360MHz, incorporating a JPEG codec, a pixel processing accelerator,

an H.264 video encoder and a MIPI interface; it offers powerful image and voice processing capabilities.

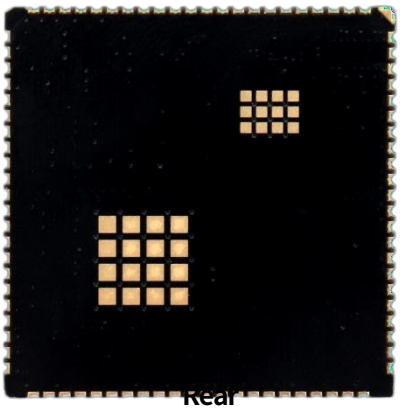
## 1.2. Features

- Dual-core CPU with a high clock speed of 360 MHz.
- Built-in 16 MB Flash and 32 MB PSRAM.
- Full pin-out of the ESP32-P4 chip.
- The core board is compact, facilitating hardware design
- Comprehensive development resources

## 1.3. Product images




Front view



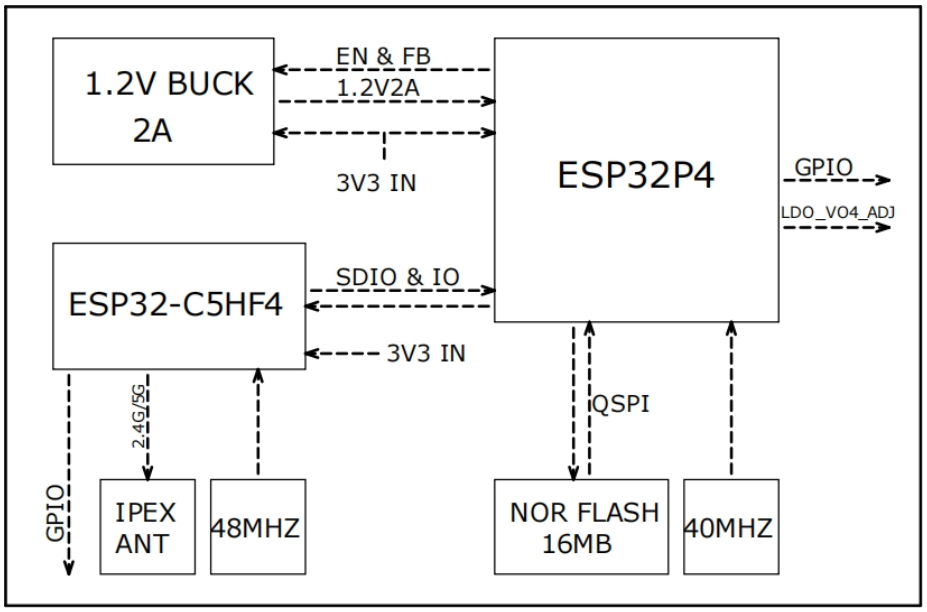
Real

## 1.4. Application scenarios

- Smart Home
- Industrial Automation
- Consumer Electronics
- HMI (Human-Machine Interface)
- Robotics
- Camera video streaming
- USB devices

# 2. Product Specifications

## 2.1. Function Block Diagram



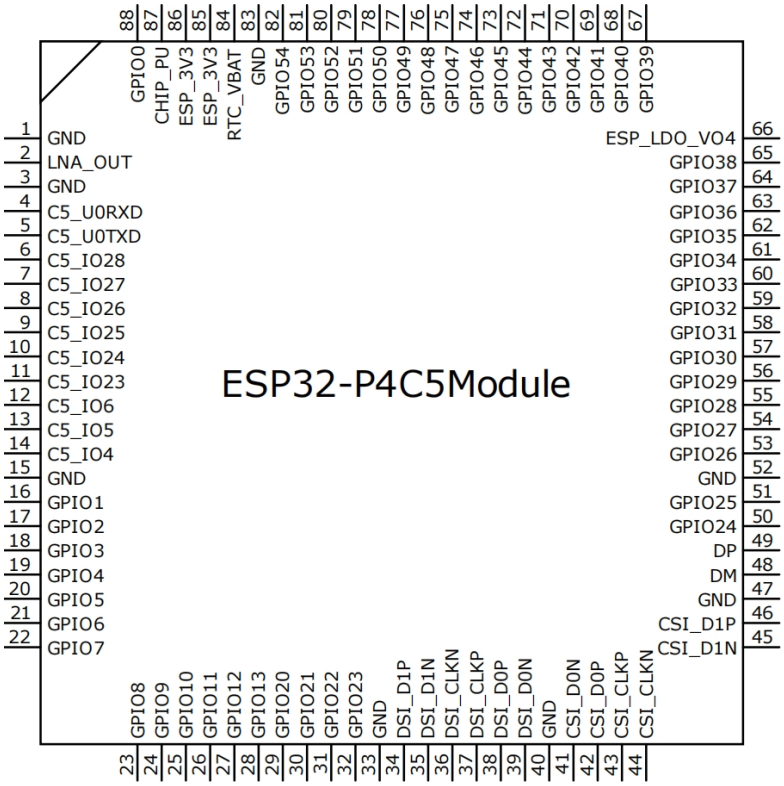

## 2.2 Hardware Specifications

| | | |
|---|---|---|
| Main controller | CPU | ESP32-P4 |
| | Core | RISC-V 32-bit dual-core processor |
| | Clock speed | 360 MHz (HP system) |
| | | 40 MHz (LP system) |
| Memory | ROM | 128 KB HP ROM |
| | | 16 KB LP ROM |
| | SRAM | 768 KB HP L2MEM |
| | | 32 KB LP SRAM |
| | Flash | 16 MB |
| Peripheral interfaces | GPIO | 55 |
| | SPI | 2 |
| | LP SPI | 1 |
| | UART | 5 |

| | | |
|---|---|---|
| | LP UART | 1 |
| | I3C | 1 |
| | I2C | 2 |
| | LP I2C | 1 |
| | I2S | 3 |
| | LP I2S | 1 |
| | USB JTAG | 1 |
| | SDIO | 1 |
| | LED PWM | 1 |
| | MCPWM | 2 |
| | TWAI Controller<br>(ISO 11898-1 compliant) | 3 |
| | High-speed USB 2.0 OTG | 1 |
| | Full-Speed USB 2.0 OTG | 1 |
| | 100 Mbps Ethernet MAC | 1 |
| | MIPI CST-2 | 1 |
| | MIPI DSI | 1 |
| | Parallel I/O (PARLIO) Controller | 1 |
| | 12-bit multi-channel analogue-to-digital converter | 2 |
| | Temperature sensor | 1 |
| | Touch sensor | 1 |
| | Analogue voltage comparator | 1 |
| | Undervoltage monitoring | 1 |
| Image and Audio Processing Interface | JPEG Encoder/Decoder | 1 |
| | Pixel Processing Accelerator (PPA) | 1 |
| | Image Signal Processor (ISP) | 1 |
| | H.264 Video Encoder | 1 |

# 3. Pin Definitions

## 3.1. Pin Layout



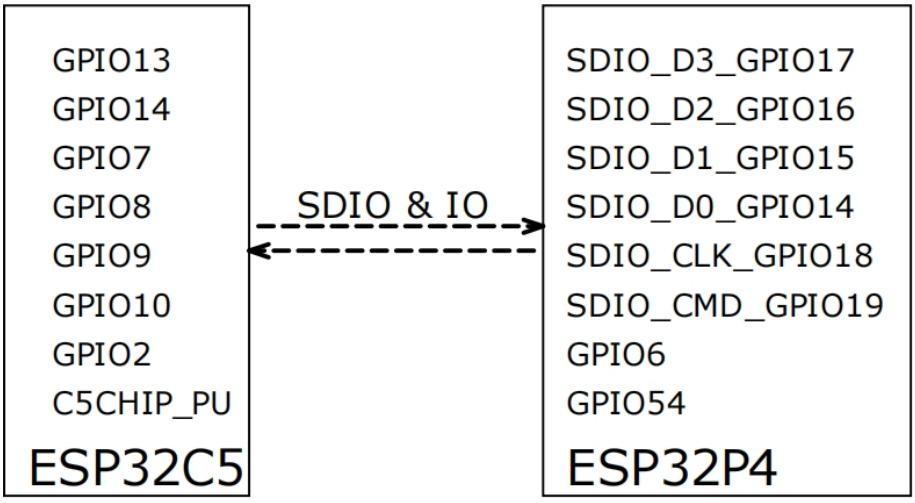

## 3.2. Pin Description

| Pin | Name | Description |
|---|---|---|
| 1 | GND | Power ground |
| 2 | LAN_OUT | ESP32-C5 ANT antenna interface (on-board IPEX-1 interface) |
| 3 | GND | Power ground |
| 4 | C5_U0RXD | ESP32-C5 U0RXD (ESP32-C5 programming pin) |
| 5 | C5_U0TXD | ESP32-C5 U0TXD (ESP32-C5 programming pin) |
| 6 | C5_IO28 | GPIO28 on the ESP32-C5 (ESP32-C5 strapping pin) |
| 7 | C5_IO27 | GPIO27 on the ESP32-C5 (ESP32-C5 strapping pin) |
| 8 | C5_IO26 | GPIO26 on the ESP32-C5 (ESP32-C5 strapping pin) |

| | | |
|---|---|---|
| 9 | C5_IO25 | GPIO25 on the ESP32-C5 |
| 10 | C5_IO24 | GPIO24 on the ESP32-C5 |
| 11 | C5_IO23 | GPIO23 on the ESP32-C5 |
| 12 | C5_IO6 | GPIO6 on the ESP32-C5 |
| 13 | C5_IO5 | GPIO5 on the ESP32-C5 |
| 14 | C5_IO4 | GPIO4 on the ESP32-C5 |
| 15 | GND | Ground |
| 16 | GPIO1 | GPIO1, LP_GPIO1, XTAL_32K_P |
| 17 | GPIO2 | GPIO2, MTCK, LP_GPIO2, TOUCH_CHANNEL0 |
| 18 | GPIO3 | GPIO3, MTDI, LP_GPIO3, TOUCH_CHANNEL1 |
| 19 | GPIO4 | GPIO4, MTMS, LP_GPIO4, TOUCH_CHANNEL2 |
| 20 | GPIO5 | GPIO5, MTDO, LP_GPIO5, TOUCH_CHANNEL3 |
| 21 | GPIO6 | GPIO6, SPI2_HOLD_PAD, LP_GPIO6, TOUCH_CHANNEL4 |
| 22 | GPIO7 | GPIO7, SPI2_CS_PAD, LP_GPIO7, TOUCH_CHANNEL5 |
| 23 | GPIO8 | GPIO8, UART0_RTS_PAD, SPI2_D_PAD, LP_GPIO8, TOUCH_CHANNEL6 |
| 24 | GPIO9 | GPIO9, UART0_CTS_PAD, SPI2_CK_PAD, LP_GPIO9, TOUCH_CHANNEL7 |
| 25 | GPIO10 | GPIO10, UART1_TXD_PAD, SPI2_Q_PAD, LP_GPIO10, TOUCH_CHANNEL8 |
| 26 | GPIO11 | GPIO11, UART1_RXD_PAD, SPI2_WP_PAD, LP_GPIO11, TOUCH_CHANNEL9 |
| 27 | GPIO12 | GPIO12, LP_GPIO12, TOUCH_CHANNEL10 |
| 28 | GPIO13 | GPIO13, LP_GPIO13, TOUCH_CHANNEL11 |
| 29 | GPIO20 | GPIO20, ADC1_CHANNEL4 |
| 30 | GPIO21 | GPIO21, ADC1_CHANNEL5 |
| 31 | GPIO22 | GPIO22, ADC1_CHANNEL6 |
| 32 | GPIO23 | GPIO23, ADC1_CHANNEL7, REF_50M_CLK_PAD |
| 33 | GND | Power ground |
| 34 | DSI_D1P | MIPI DSI PHY DATAP1 |
| 35 | DSI_D1N | MIPI DSI PHY DATAN1 |
| 36 | DSI_CLKN | MIPI DSI PHY CLKN |
| 37 | DSI_CLKP | MIPI DSI PHY CLKP |
| 38 | DSI_D0P | MIPI DSI PHY DATAP0 |
| 39 | DSI_D0N | MIPI DSI PHY DATAN0 |
| 40 | GND | Power Ground |
| 41 | CSI_D0N | MIPI CSI PHY DATA N |

| | | |
|---|---|---|
| 42 | CSI_D0P | MIPI CSI PHY DATAP0 |
| 43 | CSI_CLKP | MIPI CSI PHY CLKP |
| 44 | CSI_CLKN | MIPI CSI PHY CLKN |
| 45 | CSI_D1N | MIPI CSI PHY DATAN1 |
| 46 | CSI_D1P | MIPI CSI PHY DATAP1 |
| 47 | GND | Power Ground |
| 48 | DM | USB 2.0 OTG PHY DM |
| 49 | DP | USB 2.0 OTG PHY DP |
| 50 | GPIO24 | GPIO24, USB1P1_N0 |
| 51 | GPIO25 | GPIO25, USB1P1_P0 |
| 52 | GND | Power ground |
| 53 | GPIO26 | GPIO26, USB1P1_N1 |
| 54 | GPIO27 | GPIO27, USB1P1_P1 |
| 55 | GPIO28 | GPIO28, SPI2_CS_PAD, GMAC_PHY_RXDV_PAD |
| 56 | GPIO29 | GPIO29, SPI2_D_PAD, GMAC_PHY_RXD0_PAD |
| 57 | GPIO30 | GPIO30, SPI2_CK_PAD, GMAC_PHY_RXD1_PAD |
| 58 | GPIO31 | GPIO31, SPI2_Q_PAD, GMAC_PHY_RXER_PAD |
| 59 | GPIO32 | GPIO32, SPI2_HOLD_PAD, GMAC_RMII_CLK_PAD |
| 60 | GPIO33 | GPIO33, SPI2_WP_PAD, GMAC_PHY_TXEN_PAD |
| 61 | GPIO34 | GPIO34, SPI2_IO4_PAD, GMAC_PHY_TXD0_PAD |
| 62 | GPIO35 | GPIO35, SPI2_IO5_PAD, GMAC_PHY_TXD1_PAD (no pull-up inside the module) |
| 63 | GPIO36 | GPIO36, SPI2_IO6_PAD, GMAC_PHY_TXER_PAD (no pull-up inside the module) |
| 64 | GPIO37 | GPIO37, UART0_TXD_PAD, SPI2_IO7_PAD (ESP32-P4 programming pin) |
| 65 | GPIO38 | GPIO38, UART0_RXD_PAD, SPI2_DQS_PAD (ESP32-P4 programming pin) |
| 66 | ESP_LDO_VO4 | Output power supply (output voltage range 0.5–2.7 V or 3.3 V, maximum output current 0.2 A) |
| 67 | GPIO39 | GPIO39, SD1_CDATA0_PAD, REF_50M_CLK_PAD |
| 68 | GPIO40 | GPIO40, SD1_CDATA1_PAD, GMAC_PHY_TXEN_PAD |
| 69 | GPIO41 | GPIO41, SD1_CDATA2_PAD, GMAC_PHY_TXD0_PAD |
| 70 | GPIO42 | GPIO42, SD1_CDATA3_PAD, GMAC_PHY_TXD1_PAD |
| 71 | GPIO43 | GPIO43, SD1_CCLK_PAD, GMAC_PHY_TXER_PAD |
| 72 | GPIO44 | GPIO44, SD1_CCMD_PAD, GMAC_RMII_CLK_PAD |
| 73 | GPIO45 | GPIO45, SD1_CDATA4_PAD, GMAC_PHY_RXDV_PAD |
| 74 | GPIO46 | GPIO46, SD1_CDATA5_PAD, GMAC_PHY_RXD0_PAD |
| 75 | GPIO47 | GPIO47, SD1_CDATA6_PAD, GMAC_PHY_RXD1_PAD |

| | | |
|---|---|---|
| 76 | GPIO48 | GPIO48, SD1_CDATA7_PAD, GMAC_PHY_RXER_PAD |
| 77 | GPIO49 | GPIO49, GMAC_PHY_TXEN_PAD, ADC2_CHANNEL0 |
| 78 | GPIO50 | GPIO50, GMAC_RMII_CLK_PAD, ADC2_CHANNEL1 |
| 79 | GPIO51 | GPIO51, GMAC_PHY_RXDV_PAD, ADC2_CHANNEL2, ANA_COMP0 |
| 80 | GPIO52 | GPIO52, GMAC_PHY_RXD0_PAD, ADC2_CHANNEL3, ANA_COMP0 |
| 81 | GPIO53 | GPIO53, GMAC_PHY_RXD1_PAD, ADC2_CHANNEL4, ANA_COMP1 |
| 82 | GPIO54 | GPIO54, GMAC_PHY_RXER_PAD, ADC2_CHANNEL5, ANA_COMP1 |
| 83 | GND | Power ground |
| 84 | RTC_VBAT | The backup power supply pin must not be left floating; the voltage range is 2.3V to 3.6V (can be connected to a 3.3V supply) |
| 85 | ESP_3V3 | Power supply (3.3V input from the core board) |
| 86 | ESP_3V3 | Power supply (3.3V input from core board) |
| 87 | CHIP_PU | Enable ESP32-P4 chip (no internal RC reset; external reset required) |
| 88 | GPIO0 | GPIO0, LP_GPIO0, XTAL_32K_N |




Pin mapping between ESP32C5HF4 and ESP32P4

## 3.3. Boot options configuration

### 3.3.1. Strapping

Upon power-up or hardware reset, the following boot parameters can be configured via the Strapping pins and eFuse bits without the involvement of the microprocessor:

- Chip boot mode

- Strapping Pins: GPIO35, GPIO36, GPIO37, GPIO38

' ROM Logging

- Strapping pins: GPIO36

- eFuse bit: EFUSE UART PRINT CONTROL

' JTAG Signal Source

-Strapping pins: GPIO34

- eFuse bits: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG and EFUSE_JTAG_SEL_ENABLE The default values for the above eFuse

bits are all set to 0 by default, meaning they have not been programmed.

eFuses can only be programmed once; once set to 1, they cannot be restored to 0.

If the aforementioned strapping pins are not connected to any circuit or the connected circuit is in a high-impedance state, their default value (i.e. logic level) depends on the state of the internal weak pull-up/pull-down resistor at reset.

Default configuration of strapping pins

| Strapping Pins | Default Configuration | Value |
|---|---|---|
| GPIO34 | Floating | - |
| GPIO35 | Weak pull-up | 1 |
| GPIO36 | Floating | - |
| GPIO37 | Floating | - |
| GPIO38 | Floating | - |

To change the value of the strapping pins, external pull-down or pull-up resistors can be connected. If the ESP32-P4 is used as a slave device to a host MCU, the level of the strapping pins can also be controlled via the host MCU.

All strapping pins have latches. Upon system reset, the latch samples and stores the value of the corresponding strapping pin, which is retained until the chip is powered down or switched off. The state of the latch cannot be altered by any other means. Consequently, the value of the strapping pin remains readable whilst the chip is active, and the strapping pin functions as a standard I/O pin after the chip is reset.

### 3.3.2. Chip Start-up Mode Control

After reset is released, GPI035 to GPI38 collectively determine the start-up mode. See the table below for details.

| Start-up Mode | GPIO35 | GPIO36 | GPIO37 | GPIO38 |
|---|---|---|---|---|
| SPI Boot* | 1* | Any value | Any value | Any value |
| Joint Download Boot | 0 | 1 | Any value | Any value |

Indicates the default value and default configuration.

The following download methods are supported in Joint Download Boot mode: USB Download Boot:

- USB-Serial-JTAG Download Boot
- USB 2.0 OTG Download Boot

- UART Download Boot
- SPI Slave Download Boot

### 3.3.3. ROM- Log Printing Control

During system boot, the ROM code log can be printed to:

- (default) UART0 and USB serial/JTAG controller
- USB serial port/JTAG controller
- UARTO

EFUSE_UART_PRINT_CONTROL and GPIO36 control UARTO ROM log printing; see the table below

| UART ROM log output | EFUSE_UART_PRINT_CONTROL | GPIO37 |
|---|---|---|
| Enable | 0* | Ignore |
| | 1 | 0 |
| | 2 | 1 |
| Close | 1 | 1 |
| | 2 | 0 |
| | 3 | Ignore |

* Indicates default values and default configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls USB serial/JTAG controller ROM logging; see the table below for details.

| USB Serial/JTAG ROM Logging Control | EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT |
|---|---|
| Enable* | 0* |
| Disabled | 1 |

*Indicates default value and default configuration

# 4. Electrical characteristics

## 4.1. Absolute Maximum Limits

Exceeding the absolute maximum ratings may result in permanent damage to the device. These are merely highlighted ratings and do not imply functional operation of the device under these or other conditions beyond the specifications. Prolonged exposure to absolute maximum conditions may affect the reliability of the ESP32-P4C5-Core.

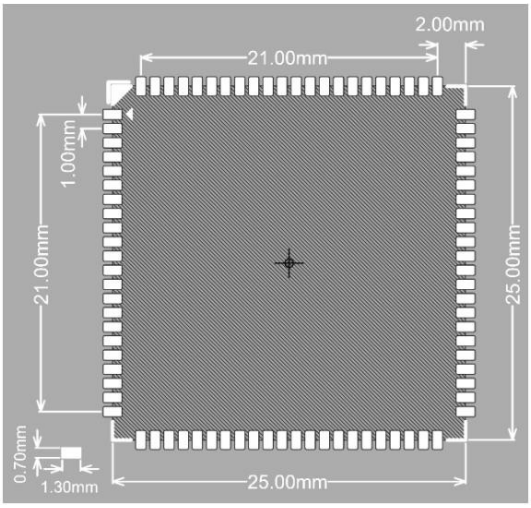
### 4.2. Power Consumption Characteristics

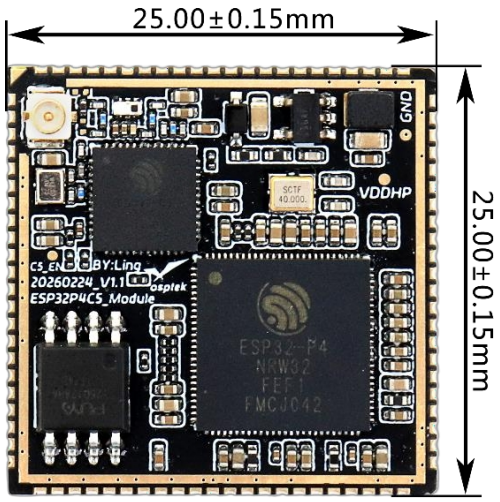
| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| VCC | Power supply pin voltage | 3.0 | 3.3 | 3.6 | V |
| IVCC | External power supply current | - | 1 | - | A |
| TA | Operating temperature | -40 | - | 85 | ℃ |

## 5. Schematic

Not available

## 6. Product dimensions




## 7. Storage Conditions

| Conditions | Specifications |
|---|---|
| Storage conditions | In a sealed MBB, in a non-condensing atmospheric environment at <40°C/90% RH |
| Operating conditions | At 25±5 °C and 60% RH for 168 hours |
| Moisture sensitivity | Grade 3 |

## 8. Reflow soldering profile