

Osptek Display

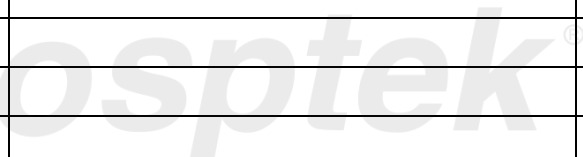
AMOLED SPECIFICATION

Model No:

E1394AC63.A

osptek[®]

Version History



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1 Scope

This Specification defines AMOLED manufactured by EverDisplay Optonics(Shanghai) Limited, from here on refer as Ospitek. In the case of any unspecified item, it may require both Ospitek and the party designs this module into its product to work out a solution.

2 Features

2.1 Product Applications

Smart Watch(On-cell)

2.2 Product Features

- 1) Display color: 16.7M (RGB x 8bits)
- 2) Display format: 1.4"(454RGBx454)
- 3) Pixel arrangement: Real RGB arrangement
- 4) Interface: MIPI/SPI
- 5) Driver IC: ICNA3310/3311 TP IC:ZT622

0400h	0401h	0402h
-	01	-

3 Mechanical Specifications

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	5.5	V	-
I/O voltage	VDDIO	-0.3	-	5.5	V	-
Operating temperature	Top	-20	-	60	°C	-
Storage temperature	Tstg	-30	-	70	°C	-

4 Maximum Rating

Item	Specification	unit
Panel outline	38.46(V) x 38.62(W) x 0.78(T)	mm
LTPS Glass outline	38.46(V) x 38.62(W)	mm
Encapsulation Glass outline	37.71(V)x38.62(W)	mm
Number of dots	454(W) x RGB x 454(H)	dots
Active area	φ35.41	mm

Diagonal size	1.39	inch
Pixel pitch	78 x 78	μm
Glass thickness (LTPS/encapsulation glass)	0.3 (up) + 0.2 (under)	mm
Weight	TBD	g

5 Electrical Specifications

5.1 Electrical Characteristics

5.1.1 Power Characteristic:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	4.55	4.6	4.65	V	-
AMOLED power Negative	ELVSS	-2.45	-2.4	-2.35	V	Ref
Digital Power supply	VDDIO	1.65	1.8	1.95	V	Ref
Analog Power supply	VCI	3.2	3.3	3.4	V	Ref

1) Normal Mode

Power Supply: IOVCC=1.8V VCI=3.3V

Frame Frequency: F_{frame} =60HZ @ 25degC, Brightness 400 nits, Command Mode,

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
100% Pixel On 400nits	IELVDD /ELVSS	-	35	55	mA	Ref
	IVCI	-	6	7.2	mA	Ref
	IVDDIO	-	4	5	mA	Ref

2) Idle Mode

Power Supply: IOVCC=1.8V VCI=3.3V

Frame Frequency: F_{frame} =15HZ @ 25degC, Brightness:30nits, OPR:10%,Command Mode

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
10% Pixel On 30 nits	IELVDD /ELVSS	-	-	-	mA	Supplied by Driver IC
	IVCI	-	3	3.6	mA	Ref
	IVDDIO	-	1.2	1.5	mA	Ref

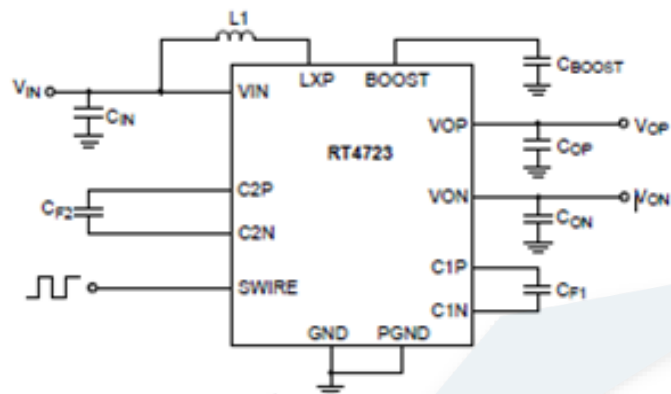
3) Deep Standby Mode

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
Deep Standby	IVCI	-	-	15	uA	-
	IVDDIO	-	-	4	uA	-

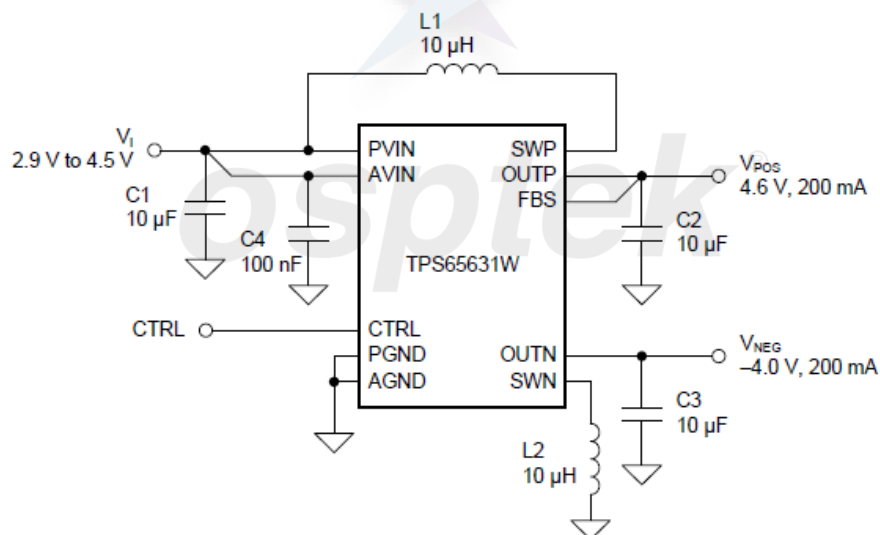
	Power Consumption	-	-	<50	uW	Ref
--	-------------------	---	---	-----	----	-----

5.1.2 Power supply circuit application (This is for reference only):

1) RT4723



2) TPS65631W



5.1.3 Power Characteristic for TP:

Power Supply:: TP_VCI=2.8V, IOVCC=1.8V

TP Report Rate: 80HZ @ AMOLED Frame Frequency =60Hz

	Work Mode	Symbol	Value		Unit	Remark
			Typ	Max		
Power Consumption	Active	P	-	7.5	mW	

5.2 I/O Connection and Block Diagrams

5.2.1 Main FPC connector pin Define

Pin No.	Symbol	I/O	Function Description
1	ELVSS	Power	AMOLED power Negative
2	ELVDD	Power	AMOLED power Positive
3	ELVSS	Power	AMOLED power Negative
4	ELVDD	Power	AMOLED power Positive
5	ELVSS	Power	AMOLED power Negative
6	ELVDD	Power	AMOLED power Positive
7	NC(OTP)	--	--
8	GND	Power	The power ground
9	SWIRE	O	Swire protocol setting pin of Power IC
10	MIPI_D0N	I/O	MIPI DSI data0-
11	VDDIO	Power	Driver IC digital I/O supply
12	MIPI_D0P	I/O	MIPI DSI data0+
13	VCI	Power	Driver IC analog supply
14	GND	Power	The power ground
15	TE	O	Tear effect output
16	MIPI_CLKN	I/O	MIPI DSI clock-
17	RST	I	OLED Device reset signal (0:enable;1:Disable)
18	MIPI_CLKP	I/O	MIPI DSI clock+
19	GND	Power	The power ground
20	GND	Power	The power ground
21	SPI_CSX	I	SPI interface
22	SPI_SCL	I	SPI interface
23	SPI_SDI	I	SPI interface
24	SPI_DCX	I	SPI interface
25	SPI_SDO	I	SPI interface
26	SAS	--	The power ground
27	GND	Power	The power ground
28	GND	Power	The power ground
29	NFC1	Power	NFC
30	NFC2	Power	NFC

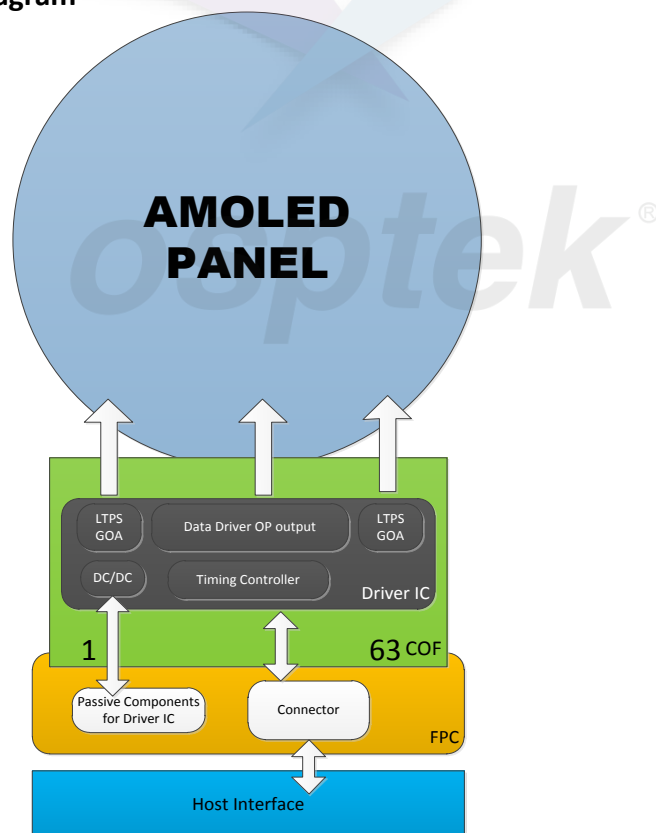
5.2.2 TP FPC connector pin Define

Pin No.	Symbol	I/O	Function Description	When not use
1	GND	-	GND	
2	GND	-	GND	
3	RESET	I/O	Interrupt	
4	VDD	Power	Power	
5	INT	I	IIC interface	
6	SCL	I	IIC interface	
7	VDDIO	I/O	IIC interface	
8	SDA	Power	Power	
9	GND	-	GND	
10	GND	-	GND	

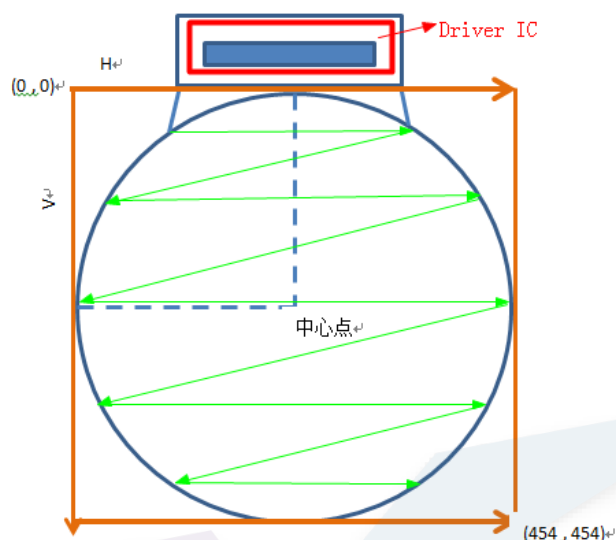
5.3 Initial CODE

TBD

5.4 System Block Diagram



5.4.1 Graphic memory writing direction



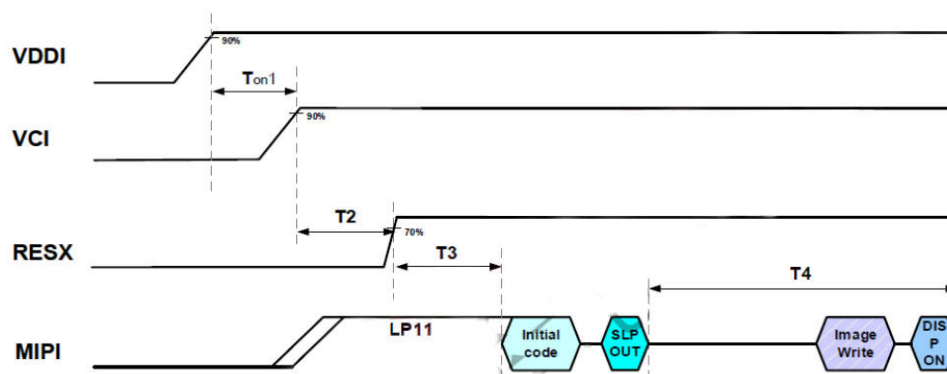
5.5 Recommended Operating Sequence

5.5.1 Power on sequence

Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T _{on1}	VDDI on to VCI on delay	>0			us	
T2	VDDI on to valid to RESET high	10			ms	
T3	RESET high to MIPI first commad	10			ms	
T4	Sleep-out command received to Display on command received.	120			ms	

The Power on sequence is shown as below.

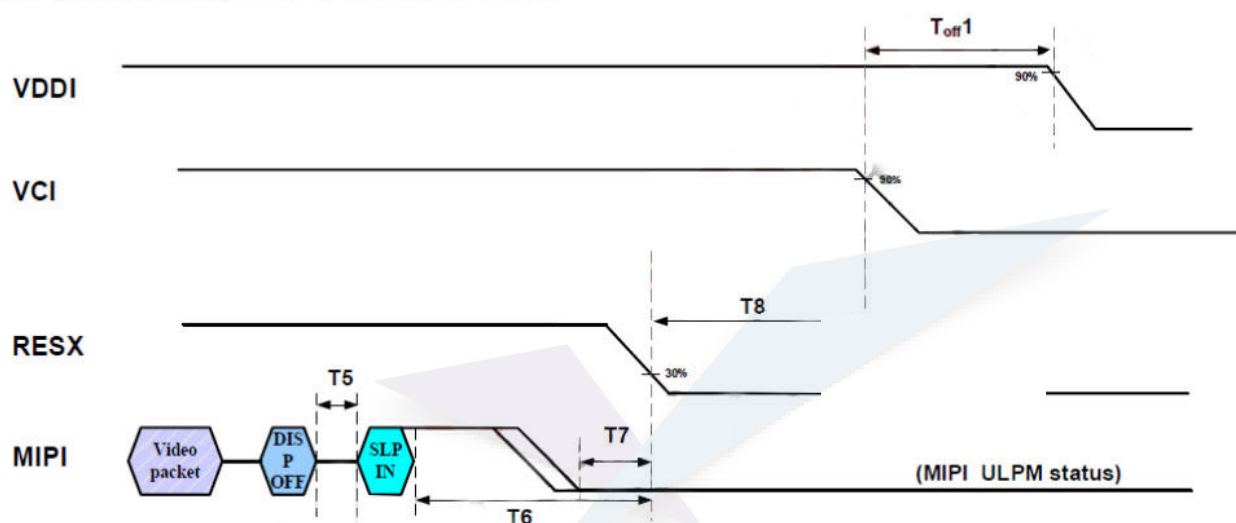


5.5.2 Power off sequence

Power OFF Sequence Timing

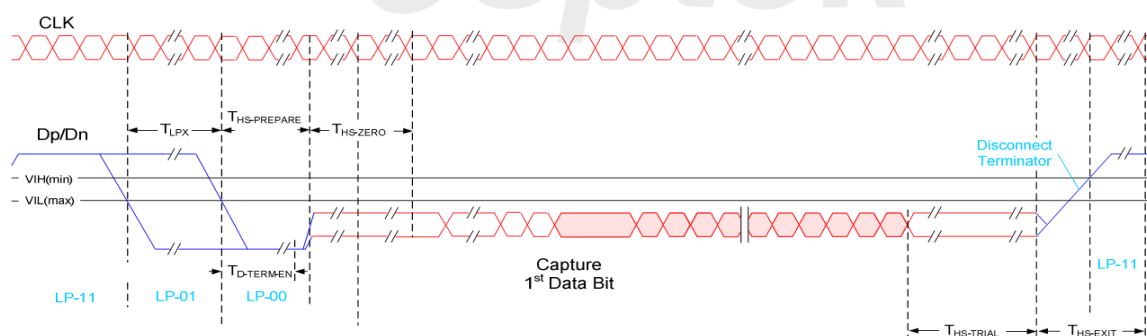
Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T _{off1}	VCI off to VDDI off delay	>0			us	
T5	Display-off command received to Sleep-in command delay	>0			us	
T6	Sleep-in command received to valid to RESET low	100			ms	
T7	MIPI ultra low power mode to valid to RESET low	0			us	
T8	RESET low to VCI off delay	0			us	

The power off sequence is shown as below:

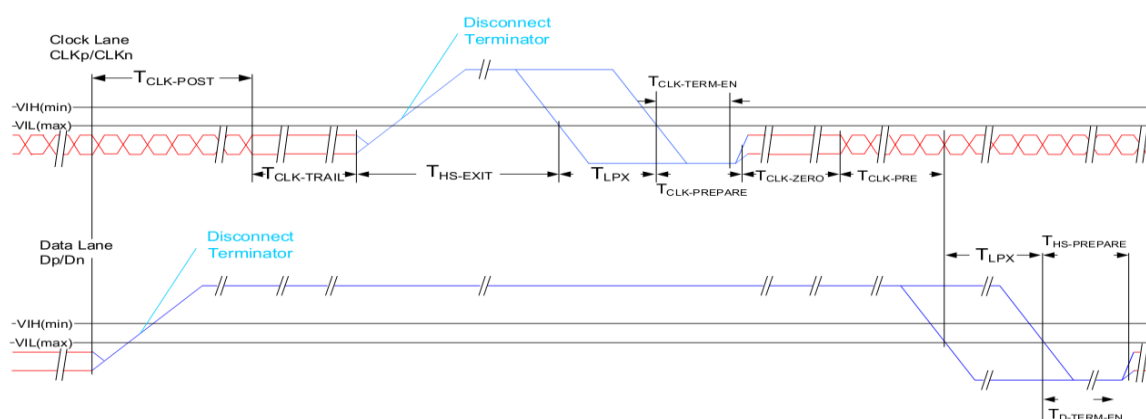


5.6 AC Characteristics (MIPI)

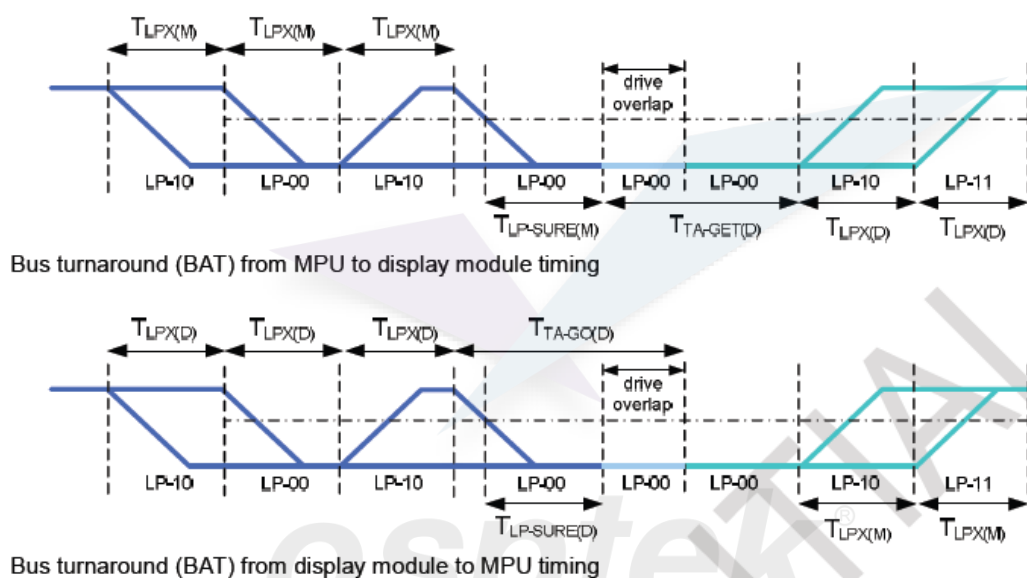
5.6.1 HS Data Transmission Burst



5.6.2 HS Clock Transmission



5.6.3 Turnaround Procedure



5.6.4 Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
TREOT	30%-85% rise time and fall time	-	-	35	ns
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
TCLK-POST*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to	60ns + 52*UI (For DCS)	-	-	ns

	LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.				
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE.	95	-	300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX.	Time for Dn to reach VTERM-EN		38	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THSPREPARE.	$85 \text{ ns} + 6 \cdot \text{UI}$		$145 \text{ ns} + 10 \cdot \text{UI}$	ns
TEOT	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	-	-	$105 \text{ ns} + 48 \cdot \text{UI}$	ns
THS-EXIT(1)	time to drive LP-11 after HS burst	100	-	-	ns
THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	$40 \text{ ns} + 4 \cdot \text{UI}$	-	$85 \text{ ns} + 6 \cdot \text{UI}$	ns

THS-PREPARE + THS-ZERO	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
TLPX	Length of any Low-Power state period	50	-	-	ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side	2/3	-	3/2	ns
TTA-GET	Time to drive LP-00 by new TX	5*TLPX	5*TLPX	5*TLPX	ns
TTA-GO	Time to drive LP-00 after Turnaround Request	4*TLPX	4*TLPX	4*TLPX	ns
TTA-SURE	Time-out before new TX side starts driving	TLPX	-	2*TLPX	ns

5.6.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.

When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, TA=-20°C~+70°C)

Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table: Reset timing

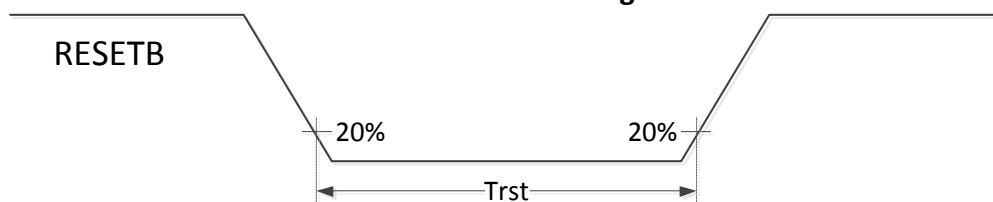
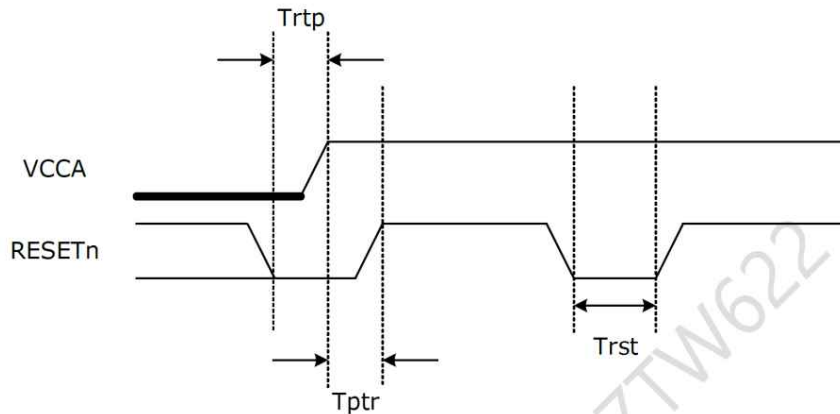


Figure: Reset timing

5.6.5 TP Reset Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{rtp}	Reset to low time before power-on	0	-	us
T_{ptr}	Reset time after power-on	1	-	ms
T_{rst}	Reset time	1	-	ms

6 Electro-Optical Specification

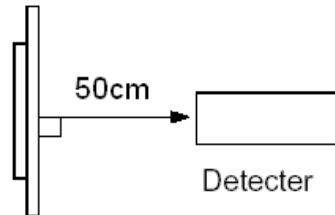
Test condition: IOVCC=1.8V , VCI=3.3V ,Ta=25°C

Item		Symbol	Condition	Value			Unit	Note
				Min	Typ	Max		
Luminance			$\theta=0^{\circ}$	350	400	450	cd/m2	Note 1
Uniformity			$\Phi=0^{\circ}$	85		-	%	Note 2
Viewing Angle	Left	θ_L	$Cr\geq 200$	80	85	-	Deg.	Note 3
	Right	θ_R		80	85	-		
	Top	ψ_T		80	85	-		
	Bottom	ψ_B		80	85	-		
Contrast Ratio		CR	$\theta=0^{\circ}$	10000	100000	-	-	Note 4
Response Time		Tr+Tf	$\Phi=0^{\circ}$	-	2	3	ms	Note 5
Color Coordinate of CIE1931	Red	X	$\theta=0^{\circ}$ $\Phi=0^{\circ}$	0.656	0.686	0.716	-	-
		Y		0.283	0.313	0.343		
	Green	X		0.185	0.235	0.285		
		Y		0.670	0.720	0.770		
	Blue	X		0.103	0.143	0.183		
		Y		0.004	0.044	0.084		
	White	X		0.28	0.30	0.32		
		Y		0.29	0.31	0.33		
NTSC Ratio		NTSC	DCI-P3	97	100	-	%	-
Flicker		-	-	-	-	-30	dB	-
Gamma		-	-	1.9	2.2	2.5		Note 6
Crosstalk		ΔCT	-	-	-	1.1		Note 7

Note 1: Luminance measurement

The test condition is measured on the surface of AMOLED module at 25°C.

- Measurement equipment CS2000 or similar equipment (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25°C.
- Adjust operating voltage to get optimum contrast at the center of the display.



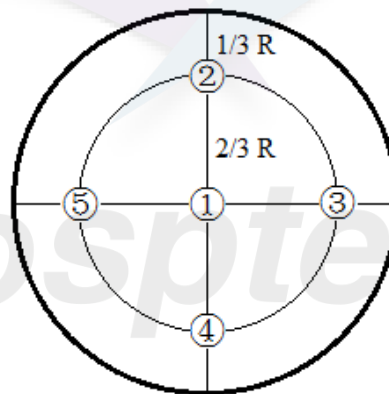
Note 2: Uniformity

The luminance uniformity is calculated by using following formula:

$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

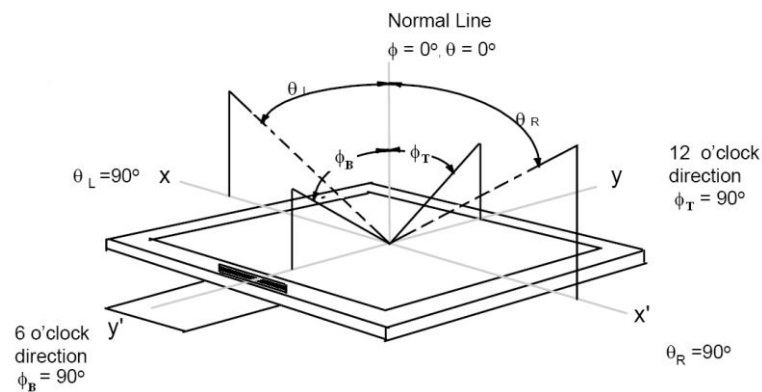
Bp (Max.) = Maximum brightness in 5 measured spots

Bp (Min.) = Minimum brightness in 5 measured spots.



Note 3: The definition of Viewing Angle

Refer to the graph below marked by ϑ and ϕ

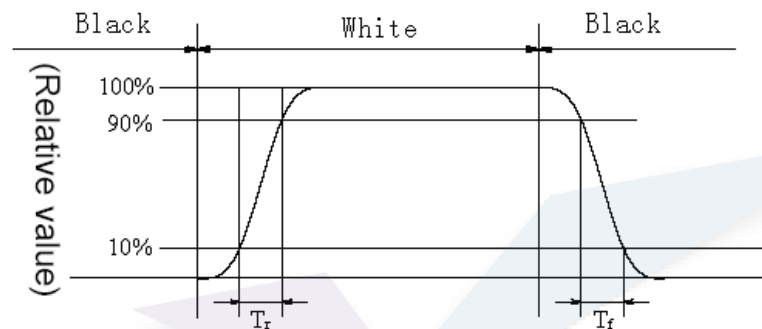


Note 4: The definition of Contrast Ratio:

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When AMOLED is at "White" state}}{\text{Luminance When AMOLED is at "Black" state}}$$

Note 5: Definition of Response time.

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (Voltage falling time) and from "white" to "black" (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 6: Gamma curve

The whole curve's tolerance must control within +/-0.3, test the gray scale below:

8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197, 206, 214, 222, 230, 239, 255

Note 7: Crosstalk

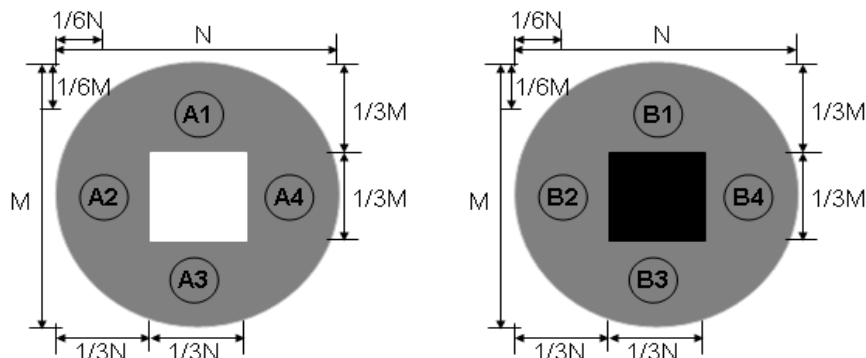
There should be no visible cross-talk in normal direction of the display when the two "Cross-talk Test Patterns" below are loaded.

ΔBp (Max.) = Maximum value in $\Delta Bp1 \sim \Delta Bp4$.

ΔBp (Min.) = Minimum value in $\Delta Bp1 \sim \Delta Bp4$.

$\Delta CT = \Delta Bp$ (Max.) / ΔBp (Min.).

ΔCT must be less than 1.10



Cross-talk Test Pattern

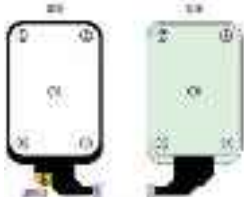
7 Reliability

7.1 Environmental Test

Item	Main spec	No. of failures / No. of examinations	Note
High Temperature Operation	70°C / 240hours	0/5	
Low Temperature Operation	-20°C / 240hours	0/5	
High Temperature Storage	80°C / 240hours	0/5	
Low Temperature Storage	-40°C / 240hours	0/5	
High Temperature Humidity Operation	60°C/90%RH 240hours	0/5	
Thermal Shock	-40°C~80°C 0.5hr, 100 cycles	0/5	
Lifetime	T95 > 240hrs	0/5	
Image sticking	6*6 棋盘格 12hrs 切 127 灰阶 3min 内 ND04 不可见	0/5	

7.2 Electrical Test

Item(Display)	Main spec	No. of failures / No. of examinations	Note
Air Discharge	±4kV , 150pF/330Ω (C class) ±6KV,150pF/330Ω (except IC,C	0/5	5Points (正面1、2、4、5、6; 反面7、8、9、10、11) , Each 2times. No degradation of OLED performance after this test.

	class)		
Contact Discharge	±4kV, 150pF/330Ω (C class)	0/5	B class: Sample 在实施静电放电时，画面有横线，闪烁，画异，无显等异常，但在不实施静电放电时回复正常显示。 C class: Sample 在实施静电放电时，画面有横线，闪烁，画异，无显等异常，且在不实施静电放电时不能恢复，但信号Reset后能恢复正常显示。

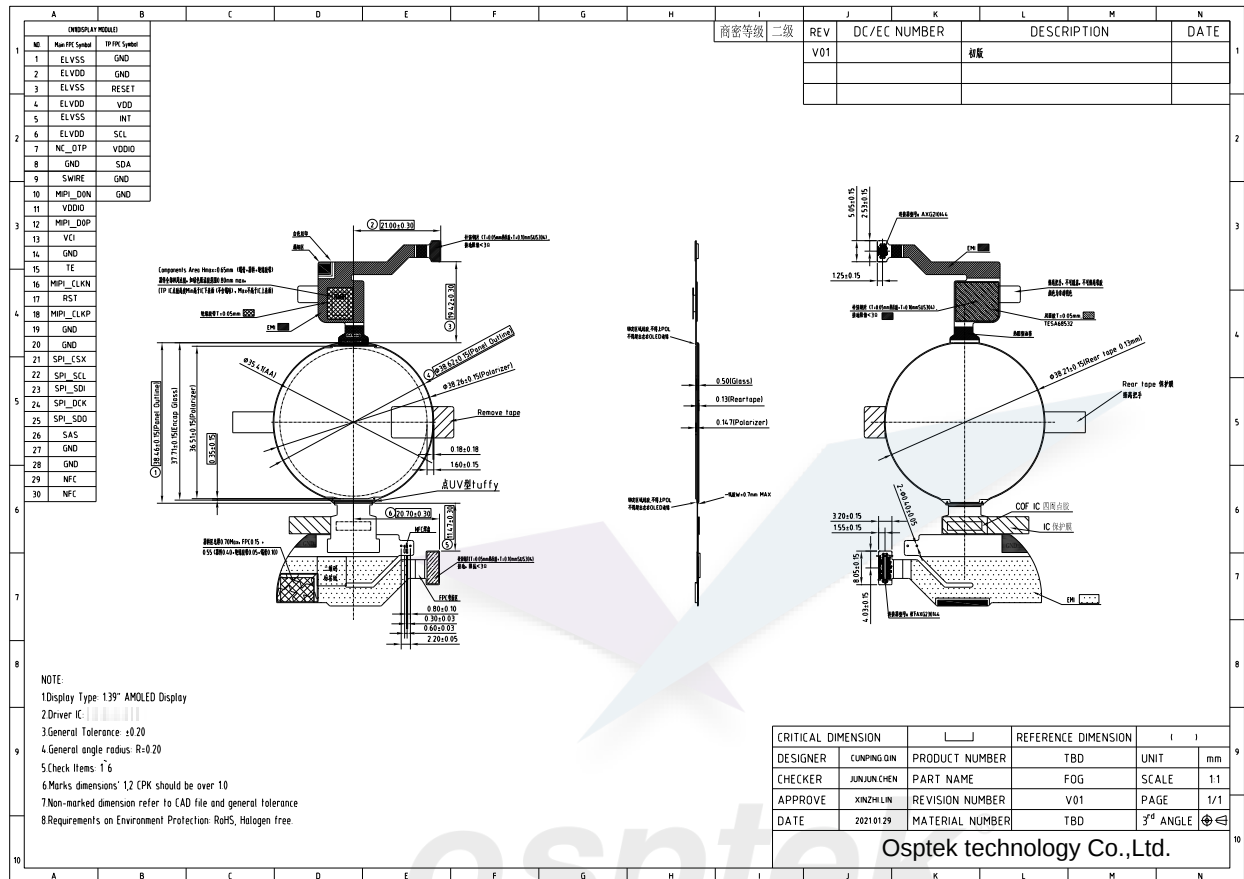
7.3 Mechanical Test

Item	Main spec	Note
Drop Test	Drop the packing from 75cm height, 1times for 6-faces, 3-edges and 1-corner	Package
Vibration-proof test	2g, f=10->55->10Hz apply in each of X, Y, and Z direction for 30 min	Package

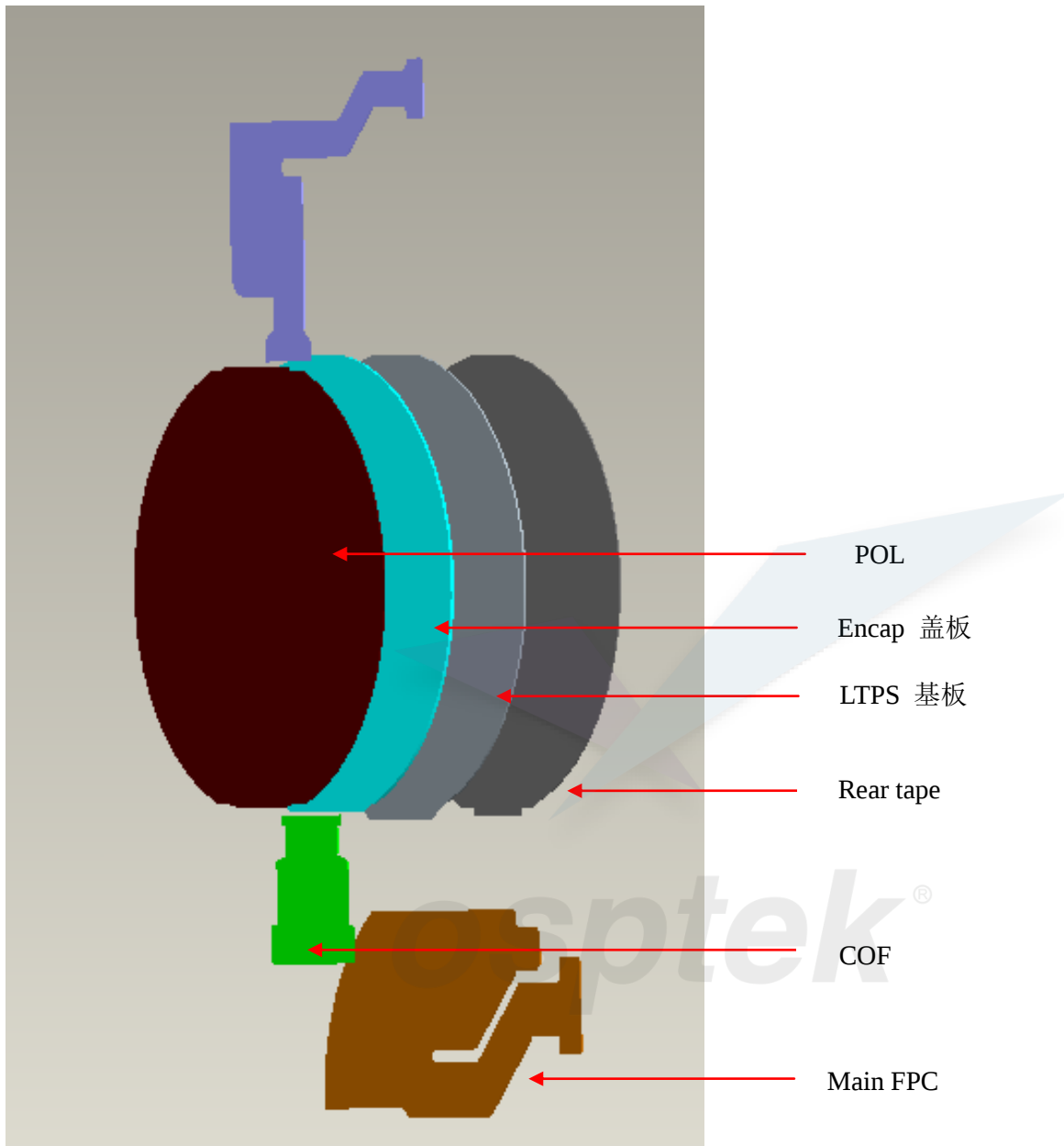
8 Handling Precautions

1. When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution
2. Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity
3. Strong impact & pressure on module and packing is prohibited
4. Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display
5. Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available
6. Image sticking may occur if an image displays for an extended period of time
7. When interfered by system's overall mechanical design, an abnormal display may occur
8. After considering emitting energy, you should plan your design to satisfy EMI standards.
9. Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

9 Outline Dimension Drawing



3D Exploded Views:



10 Packing Specification

1、整箱材料说明						
NO	料号	品名	材质	尺寸(mm)	数量(个)	备注
1	TBD	E1394AC63. A	Glass	87.55*40.31*1.00	288	
2	LA000001A	外箱标签	纸	52.00*100.00*0.10	1	
3	LA000002A	内箱标签	纸	52.00*100.00*0.08	2	
4	PK40212LA	吸塑盘	PET	455.00*290.00*14.00	20	
5	PK50193LA	EPE 填充物	EPE	393.00*235.02*1.00	36	
6	PK500001A	EPE 缓冲物	EPE	457.00*292.00*10.00	4	
7	PK100001B	纸箱	纸	516.00*338.00*248.00	1	
8	PK200001A	纸盒	纸	459.00*294.00*115.00	2	
9	PK700001A	干燥剂	干燥剂	55.00*75.00	4	
10	PK300001A	防尘袋	PE	660.00*440.00*0.28	2	
11	PK600001A	PP 板	PP	457.00*292.00*5.00	2	
12	PK500002A	EPE 缓冲物	EPE	120.00*244.00*15.00	4	
13	TBD	栈板	木材	TBD	1/30	
2、整栈板产品数量说明:						
(1) 整个吸塑盘的产品包装数量		每列的产品数量 4 个乘以每行的产品数量 4 个=16 个				
(2) 整个纸盒的产品包装数量		整个吸塑盘的产品数量 16 个乘以吸塑盘的数量 9 个=144 个				
(3) 整个纸箱的产品包装数量		整个纸盒的产品数量 144 个乘以纸盒数量 2 个=288 个				
(4) 整个栈板的产品包装数量		整个纸箱产品数量 288 个乘以纸箱的数量 30 个=8640 个				

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