DATASHEET

AXS15260

In-Cell IC Integrates 810-channel 8-bit Source Driver and GIP Gate Driver and Touch Panel Controller Into a Single Chip with TP Controller Supports Real Multi-Touch Capability

Version V0.5
2023-07-12

Table of Contents

REVISION HISTORY

Date	Version	Description	Page	Author
2022/09/09	V0.0	draft	12	paulson
2023/01/05	V0.1	Preliminary version	179	Sand
2023/03/07	V0.2	improve all diagram	173	Sand
2023/04/24	V0.3	Improve diagram of MCU;Pad assignment	162	Sand
2023/05/09	V0.4	6.1 Absolute Operation Range：VCI（max）=7.8V	162	Sand
2023/07/12	V0.5	Update the VGH voltage;Update the display resolution information	162	Sand

GENERAL DESCRIPTION

The AXS15260 highly integrates a-Si/LTPS TFT LCD driver and Super in-cell Touch controller, is a 16,777,216-color System-on-Chip (SOC) driver LSI designed for small and medium size TFT LCD display, and is capable of supporting up to 540RGBx1600(Dual gate) pixels in resolution. The 810-channel source driver can provide true 8-bit resolution and generate 256 Gamma-corrected values with an internal D/A converter.

The AXS15260 is able to operate with low IO interface power supply. Incorporating with several charge pumps, the AXS15260 can generate various voltage levels by an on-chip power management system for gate and source driver. Moreover, PWM for LED backlight, wake up-button enabling, respiratory lights and other functions, to provide customers with better experience.

In addition, the external Flash of AXS15260 can store not only the firmware used for Touch controller, but also the Initial code of LCD driver. After loading the initial code through the external Flash, the HOST only needs to send out "Sleep out" and "Display on" to turn on the LCD.

The built-in timing controller in the AXS15260 can support several functions to meet a wide variety of requirements for portable display applications. It provides several system interfaces, including MIPI/QSPI/DSPI/SPI/RGB/MCU, which can be used to configure the system. Furthermore, it can also archive high speed display data transmission by using the MIPI interface.

1 Features

1.1 Display

- One-chip solution for color amorphous a-Si TFT-LCD with incell
  Display Resolution
  - Dual gate: 540RGB(up to 540,2 Columns/step) x 1600(up to 2048, 2 lines/step)
  - Single gate:270RGB(up to 270,2 Columns/step) x 1600(up to 2048,2 lines/step)
- Frame rate 60Hz/90Hz
- Support LTPS TFT-LCD:60Hz/90Hz,540RGB*1350
- Support IGZO TFT-LCD
- Display Data Memory: external PSRAM
- Support in-chip OTP
  - 2K*8 bit
  - OTP can stores trimming、ID1，ID2（factory ID，3bit）data
- System Interfaces
  - MIPI DSI (1/2/3/4 data lane,1.25Gbps/lane):
  - MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01).
  - SPI/DSPI
  - QSPI
  - Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit, 18bit)
  - 16bit/18bit/24bit RGB(60Hz) interface
- Display Features
  - Colour depth 888，666，565
  - Analog gamma，256 gray level
  - Support 8-color and 2-color mode
- On Chip Function
  - RAM-less driver with MIPI video mode
  - Column Inversion & Dot Inversion
  - Support loading FLASH to driver registers & TP registers
  - Support 0 Flash
  - Support SPR communication protocol
  - Support 810 source channel
  - Built-in 17 GOUT signals(CGOUTL1-L17,CGOUTR1-R17) on each side of the chip,providing directly the driver signals to the GIP circuit on the LCD panel
  - Built-in internal oscillator

1.2 Touch

- 8-bit embedded MCU
- 480 SX channels
- Support five-point detection

- Point reporting rate 60Hz(frame rate 60Hz)/Point reporting rate 90Hz(frame rate 90Hz)/Point reporting rate 120Hz(frame rate 60Hz)
- Super self-capacitance detection technology
- Support wake up gesture function
- Anti-RF interference
- Automatic frequency hopping
- Water proof
- I2C/SPI data communication interface
- Internal ESD detection
- Power saving mode
- VDDI_TP and VDDI supplied independently
- Center area ≤1.0mm, edge ≤1.5mm@5mm copper column

1.3 Power

- Supply Voltage Range

3-power mode

- VSP：4.5V~6.5V，typ ： 5.5V
- VSN：-6.5V~-4.5V，typ：-5.5V
- VDDI：1.65V ~ 1.95V typ：1.8V or 2.8V~3.6V，typ：3.3V

2-power mode

- VCI：2.5V~3.6V，typ ： 2.8V
- VDDI：1.65V ~ 1.95V typ：1.8V or 2.8V~3.6V，typ：3.3V

- Output Voltage Range

- Gamma Positive Voltage Range: VGSP~VGMP（VGMP≤VSP-0.3）

VGMP：2.55~5.7V
VGSP：0.05~2.5V

- Gamma Negative Voltage Range: VGMN~VGSN（VGMN≥VSN+0.3）

VGMN：-5.7~-2.55V
VGSN：-2.15~1V

- Source Output Range: VGSP~VGMP
- Positive Gate Driver Output Voltage Level(VGH):

IGZO：VGH1 12~16V
LTPS：VGH2 6.5~10.7V

- Negative Gate Driver Output Voltage Level(VGL):

IGZO：VGL1 -13~-7.6V
LTPS：VGL2 -10~-6V

- Common Electrode Output Voltage Level(VCOM): -2.5V~0V (10mv/step)

1.4 Others

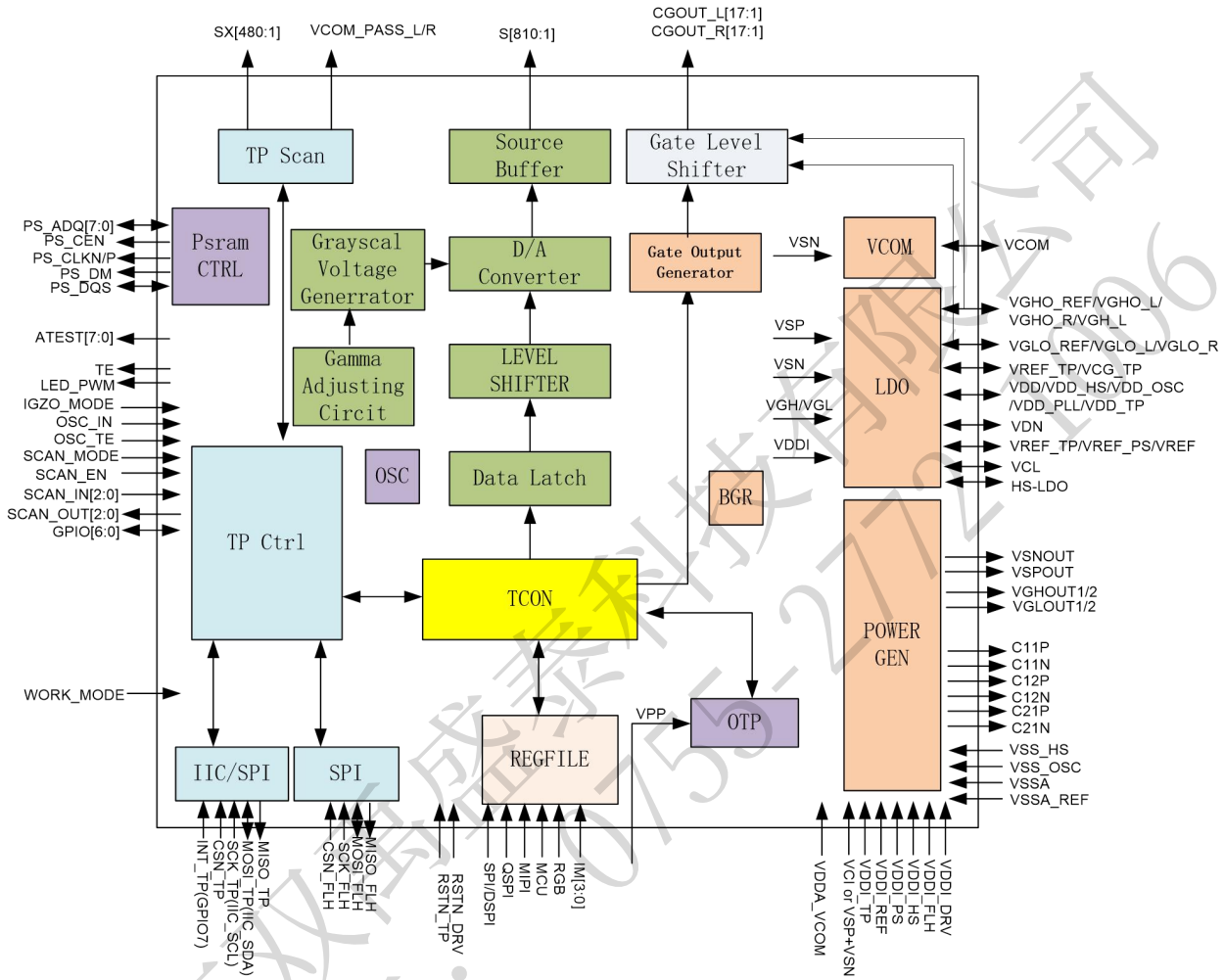
- ESD
  - HBM≥2000V

- MM≥200V
- Latch up≥±100mA

◆ COG Package

2 Block Diagram

2.1 Block Function



2.1.1 Touch Function

The touch part of AXS15260 mainly consists of the following components:

- AFE Controller

AFE controller completes the scanning of the sensors in the touch panel, and sends the data of touch sensors after scanning to the MCU for data processing.

- Embedded MCU

MCU and SOC subsystems complete the control, data processing, LCD operation and coordination, HOST communication and other functions of the whole touch systems.

- I2C/SPI serial interface

The Slave end of I2C/SPI in AXS15260 is the interface for touch communication with HOST. The control interface consists of two signals INT (is a GPIO, specified in the firmware) and RSTN (only one rstn-pin, shared by driver and touch). Whenever there is effective touch sensed on the touch

screen, Touch controller will send data transfer request to the HOST via INT port, and complete the point report to the HOST. HOST can communicate with AXS15260 via I2C or SPI. HOST can also reset Touch controller through RSTN port.

- External Flash

External Flash, used to store the Firmware, and LCD initialization code, can be added into the Touch controller.

- Watchdog

Watchdog is used to ensure the stability of the chip when in operation

- Internal voltage regulator

Internal voltage regulator generates power supply, which is to provide power to logic circuit.

2.1.2 Touch Operation Mode

Touch controller has the following three operation modes:

- Normal operating mode

In this mode, Touch controller scans the screen, and detects the touch actions.

- Monitor Mode

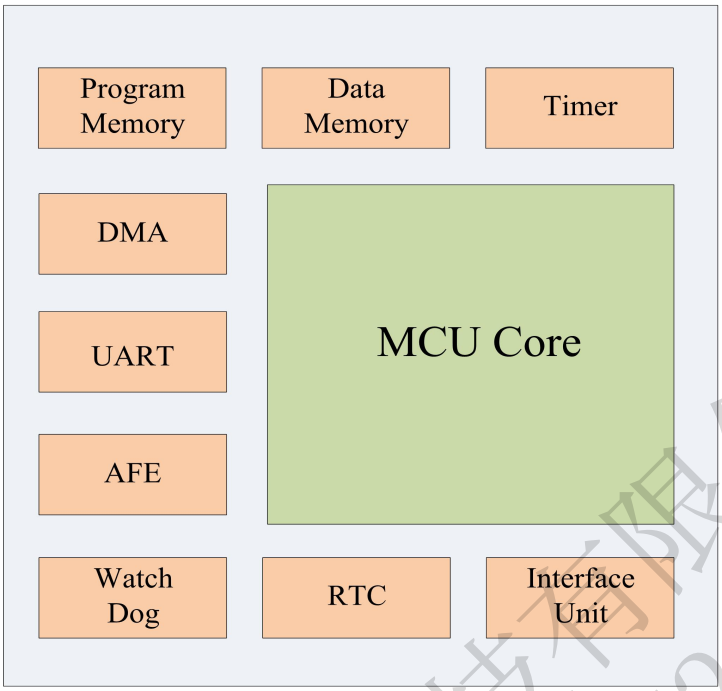
In this mode, Touch controller scans the screen intermittently to save power.

- Sleep mode

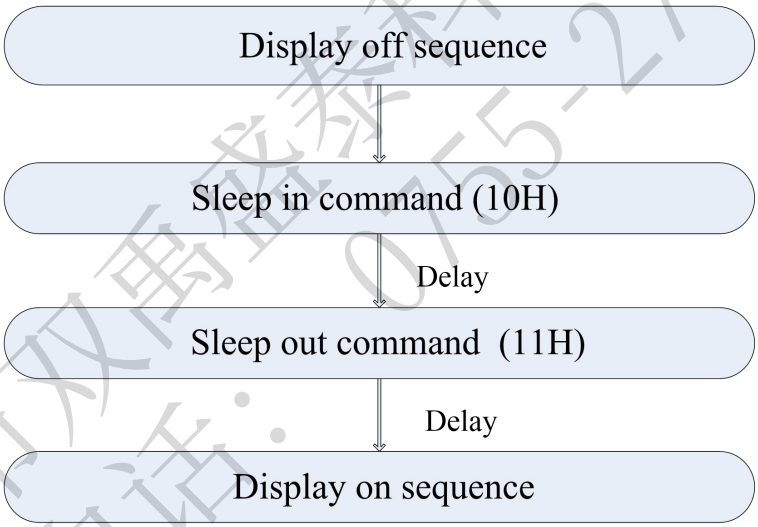
In this mode, Touch controller enters ultra low-power standby mode, HOST can only wake-up Touch controller via external signal to enter the normal operating mode. The power consumption in this mode is extremely small, and can greatly extend the standby time of mobile portable devices.

2.1.3 MCU

This section describes some critical features and operations supported by the MCU.The figure below shows the overall structure of the MCU block. In addition to the MCU core, we have added the following circuits.



2.1.4 Sleep In/Out Sequence



2.1.5 System interface

The AXS15260 supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor Interface).

2.1.6 Grayscale voltage generating circuit

AXS15260 has true 8-bit resolution D/A converter, digital gamma cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register and RGB can be adjusted separately.

2.1.7 Timing controller

AXS15260 has a timing controller, which can generate a timing signal for internal circuit

operation such as gate output timing, image data accessing timing, etc.

2.1.8 Oscillator (OSC)

The AXS15260 has an internal oscillator to generate system clock.

2.1.9 Source driver circuit

AXS15260 consists of a 810-output source driver circuit.

2.1.10 Gate driver circuit

AXS15260 consists of a gate driver control circuit. The gate driver circuit outputs gate driver signals level at either VGH or VGL level.

2.1.11 LCD driving power supply circuit

The LCD driving power supply circuit generates the voltage levels VDD, VSP, VSN, VGH, VGL, VCOM for driving a LCD. All these voltages can be adjusted by register setting.

3 Pin Description

3.1 Power Supply and Regulator pins

PIN	I/O	Default value	Description
VDDI	I	Digital Power	External input voltage.1.8V power supply for digital interface
VDDI_DRV	I	Digital Power	External input voltage.1.8V power supply for digital interface
VDDI_FLH	I	Digital Power	External input voltage for external spi-flash
VDDI_HS	I	Digital Power	External input voltage for mipi-ldo
VDDI_PS	I/O	Digital Power	Psram IO power supply,connect VDDI when VDDI=1.8V, connect 1uF cap to gnd when VDDI=3.3V
VDDI_REF	I	Analog Power	Bandgap power supply
VDDI_TP	I	Digital Power	Power supply for TP digital interface.
VSN	I	Analog Power	-5.7V voltage power supply
VSNOUT	O	Analog Power	Charge pump output
VSP	I	Analog Power	5.7V voltage power supply
VSPOUT	O	Analog Power	Charge pump output
VREF	O	Internal LDO	Output reference voltage.
VREF_PS	O	Internal LDO	Output reference voltage, need connect a stabilizing capacitor to VDDI_PS.
VREF_TP	O	Internal LDO	Regulator output voltage.
VGH	I	GIP power suuply	GIP power supply connect VGHOUT1 or VGHOUT2
VGH_L	O	GIP power suuply	Connect VGH
VGHO_L/R	O	GIP power suuply	GIP power supply,VGHO_L connect to VGHO_R

VGHO_REF	O	Charge pump	Connect a capacitor to VGHO_R
VGHOUT1	O	Charge pump	Charge pump output
VGHOUT2	O	Charge pump	Charge pump output
VGL	I	GIP power suuply	Power supply need connect a stabilizing capacitor to ground.
VGLO_L/R	O	GIP power suuply	GIP power supply,VGLO_L connect to VGLO_R
VGLO_REF	O	GIP power suuply	Connect a capacitor to VGLO_L
VGLOUT1	O	Charge pump	Charge pump output
VGLOUT2	O	Charge pump	Charge pump output
VDD	O	Internal LDO	Digital power supply, need connect a stabilizing capacitor to ground.
VDD_HS	O	Internal LDO	MIPI lower power circuit power supply, connect to VDD on FPC.
VDD_OSC	O	osc power supply	Osc power supply,conect to VDD
VDD_PLL	O	Internal LDO	Regulator output voltage for PLL.
VDD_TP	O	Internal LDO	Regulator output voltage. FPC Connect together.Connect a capacitor for stabilization.
VDN	O	Digital Power	Internal LDO output
HS_LDO	O	Internal LDO	MIPI high speed circuit power supply, need connect a stabilizing capacitor to ground.
VCG_TP	O	Internal LDO	Regulator output voltage. FPC Connect together.Connect a capacitor for stabilization.
VCI	I	analog power supply	VSPOUT/VSNOUT charge pump power supply
VCL	O	Internal LDO	LDO negative output.
VCOM	O	Analog	VCOM signal output for panel.Need connect a stabilizing capacitor to ground.
VPP	I	Digital Power	Power supply.
VDDA_VCOM	I	analog power	VCOM power supply,conect GND or VDN
VSS_HS	I	Ground	MIPI ground, connect to VSSD on FPC
VSS_OSC	I	Ground	OSC ground
VSSA	I	Ground	Analog ground
VSSA_REF	I	Ground	Bandgap ground
VSSD	I	Ground	Digital ground
C11N	O	Charge pump flying capacitor	Charge pump flying capacitor connection for VSPOUT charge pump.
C11P			
C12N			Charge pump flying capacitor connection for VSNOUT charge pump.
C12P			
C21N			Charge pump flying capacitor connection for VSNOUT charge pump.
C21P			

3.2 Drive interface

PIN	I/O	Default value	Description

DB<23:0>	I/O	Digital (VDDI)	DB[23:0] input data of rgb interface. DB[23:0] of 8080 mcu interface for command mode.
HSYNC	I	Digital (VDDI)	Line synchronizing signal of rgb interface. Used as d/cx of 8080 mcu interface for command mode.
VSYNC	I	Digital (VDDI)	Frame synchronizing signal of rgb interface. Used as csn of 8080 mcu interface for command mode. In QSPI mode, it used as QSPI_DIN2
PCLK	I	Digital (VDDI)	pixel clock signal of rgb interface. Used as rd of 8080 mcu interface for command mode.
DE	I	Digital (VDDI)	Data enable signal of rgb interface; wr of 8080 mcu interface for command mode; In QSPI mode, it used as QSPI_DIN3.
DIN_SDA_DUAL	I/O	Digital (VDDI)	The second data input pin in spi dual data lane of spi slave.pull down to avoid floating. (In QSPI mode::When cr_qspi_diomode=0, it used as QSPI_DIN1;When cr_qspi_diomode=1, it used as QSPI_DIN0.;In SPI 3wire/4wire mode-1, it used as MOSI)
DIN_SDA	I	Digital (VDDI)	The bidirectional data pin of SPI slave, pull down to avoid floating.(In QSPI mode:When cr_qspi_diomode=0, it used as QSPI_DIN0;When cr_qspi_diomode=1, it used as QSPI_DIN1;In SPI 3wire/4wire mode-0, it used as SPI_SDA;In SPI 3wire/4wire mode-1, it used as MISO)
SCL	I	Digital (VDDI)	Synchronous clock signal in SPI slave.
RS	I	Digital (VDDI)	command or parameter selection in spi 4wire 8bits.
CSX	O	Digital (VDDI)	Chip select input pin (“Low” enable) in SPI slave ,pull up to avoid floating.
SWIRE	O	Digital (VDDI)	Swire protocol setting pin (Note: “H” = VDDI level, “L” = VSSI level.)Output load 50pf.
TE	O	Digital (VDDI)	Output tearing effect signal from IC to phone,Default output hiz.
RSTN_DRV	I	Digital (VDDI)	Global reset, low active.

3.3 TP interface

PIN	I/O	Default value	Description
SX[480:1]	I/O	Analog	Separate COM Electrode(TP sensor PAD)
VCOM_PASS_L/R	I/O	Analog	Pass line for VCOM from ILB to OLB

RSTN_TP	I	Digital (VDDI_TP)	Reset, low active，weak pull up
WORK_MODE	I	Digital (VDDI_TP)	Selection of work interface;1:I2C , 0:spi；pull down
CSN_TP	I	Digital (VDDI_TP)	When WORK_MODE =1 ， floating，need weak pull up to avoid floating；when WORK_MODE =0，connect to phone spi interface chip selection signal, low active.
SCK_TP	I	Digital (VDDI_TP)	When WORK_MODE =1 ， connect to phone i2c slave interface clock signal , need open drain and extern pull up. when WORK_MODE =0，connect to phone spi interface clock signal.
MISO_TP	O	Digital (VDDI_TP)	Connect to phone spi interface data output signal, from SCK negative edge to MISO output need 6ns delay in digital internal, detail as followed spi timing. (phone input ,chip output, chip is spi_slv)
MOSI_TP	I/O	Digital (VDDI_TP)	Connect to phone I2C slave interface data input/output，need open drain and extern pull up. (chip is i2c_mst). connect to phone spi interface data input signal.(phone output ,chip input, chip is spi_slv)
CSN_FLH	O	Digital (VDDI_FLH)	Chip select of flash, low active，individual power for spi flash interface.Master output.
SCK_FLH	O	Digital (VDDI_FLH)	Clock output to flash，individual power for spi flash interface.
MISO_FLH	I	Digital (VDDI_FLH)	Data input from flash; need weak pull up to avoid floating, flash data output need 7ns delay from clock negative edge，individual power for spi flash interface.
MOSI_FLH	O	Digital (VDDI_FLH)	Data output to flash，individual power for spi flash interface.

3.4 MIPI Interface

PIN	I/O	Default value	Description
HS_CN	I	MIPI	MIPI-DSI clock Lane positive-end/ negative-end input pin.These pins are MIPI-DSI CLK+/- differential clock signals if MIPI interface is used.HS_CP/N are differential small amplitude signals. Ensure the trace length is shortest ,so that the COG resistance is less than 10 ohm.If not used, please connect these pins to VSSAM.
HS_CP			
HS_D0N	I/O	MIPI	MIPI-DSI data Lane 0 positive-end/ negative-end pin.These pins are MIPI-DSI D0+/- differential data signals if MIPI interface is used.HS_D0P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HS_D0P			

HS_D1N HS_D1P	I	MIPI	MIPI-DSI data Lane 1 positive-end/ negative-end input pin.These pins are MIPI-DSI D1+/- differential data signals if MIPI interface is used.HS_D1P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HS_D2N HS_D2P	I	MIPI	MIPI-DSI data Lane 2 positive-end input pin.These pins are MIPI-DSI D2+/- differential data signals if MIPI interface is used.HS_D2P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HS_D3N HS_D3P	I	MIPI	MIPI-DSI data Lane 3 positive-end input pin.These pins are MIPI-DSI D3+/- differential data signals if MIPI interface is used.HS_D3P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.

3.5 PSRAM interface

PIN	I/O	Default value	Description
PS_ADQ<7:0>	I/O	Digital (VDDI_PS)	Address/DQ bus [7:0]
PS_CEN	O	Digital (VDDI_PS)	Chip select,active low,when CE=1 chip is standby state
PS_CLKN/P	O	Digital (VDDI_PS)	Clock signals,they must always be complementary,even in standby
PS_DM	O	Digital (VDDI_PS)	Data mask,active high.DM=1 mens “do not write”
PS_DQS	I/O	Digital (VDDI_PS)	PSRAM DQ Strobe clock

3.6 Test/Dummy Signal/ Other

PIN	I/O	Default value	Description
ATEST0_NV ATEST1_PV ATEST2_LV ATEST3_LV ATEST4_NV ATEST5_PV ATEST6_PV ATEST7_NV	O	Analog (VSP/VSN)	Test pin
SWIRE	O	Digital (VDDI)	Swire protocol setting pin (Note: “H” = VDDI level, “L” = VSSI level.)Output load 50pf.
TE	O	Digital (VDDI)	Output tearing effect signal from IC to phone,Default output hiz.

TS_SEL	I	Digital (VDDI)	test pad

3.7 Panel driver Signals

PIN	I/O	Default value	Description
S[810:1]	O	Analog	Output source driver signals. The D/A converted 256-gray-scale analog voltage output.
CGOUT_L<17:1>	O	Analog (VGHO/VGLO)	Gate control signals for panel in left side of IC.
CGOUT1_R<17:1>	O	Analog (VGHO/VGLO)	Gate control signals for panel in right side of IC.

3.8 Logic Function Control

PIN	I/O	Default value	Description
OTP_EXT_EN	I	Digital	Conect VSP or floating.
IGZO_MOD	I	Digital (VDDI)	0:IGZO panel 1:normal panel
PMOD_SEL	I	Digital (VDDI)	power voltage set pin: 0:when VDDI=3.3v 1:when VDDI=1.8v
PSW_ENN	I	Digital (VDDI)	1:Power switching function enable 0:Some I/O power supplies are fixed to VDDI
PSW_PRIO_SEL	I	Digital (VDDI)	Select PIN for some IO power supplies 0:VDDI_TP is preferred 1:VDDI_DRV is preferred
LED_PWM	O	Digital (VDDI)	Used to adjust the brightness of panel backlight.
IM<3:0>	I	Digital (VDDI)	External interface select, pull down.
BS<3:0>	I	Digital (VDDI)	Polarity and order of MIPI selection, default 4'bXXX.

外部连接 BS[0]	外部连接 BS[3:1]	HS_ D3P	HS_ D3N	HS_ D0P	HS_ D0N	HS_ CP	HS_ CN	HS_ D1P	HS_ D1N	HS_ D2P	HS_ D2N
1	000	HS_ D2P	HS_ D2N	HS_ D3P	HS_ D3N	HS_ CP	HS_ CN	HS_ D1P	HS_ D1N	HS_ D0P	HS_ D0N
	001	HS_ D0P	HS_ D0N	HS_ D3P	HS_ D3N	HS_ CP	HS_ CN	HS_ D1P	HS_ D1N	HS_ D2P	HS_ D2N
	010	HS_ D3P	HS_ D3N	HS_ D2P	HS_ D2N	HS_ CP	HS_ CN	HS_ D0P	HS_ D0N	HS_ D1P	HS_ D1N
	011	HS_ D3P	HS_ D3N	HS_ D0P	HS_ D0N	HS_ CP	HS_ CN	HS_ D2P	HS_ D2N	HS_ D1P	HS_ D1N
	100	HS_	HS_	HS_	HS_	HS_	HS_	HS_	HS_	HS_	HS_

		D2P	D2N	D3P	D3N	CP	CN	D0P	D0N	D1P	D1N	
	101	HS_D0P	HS_D0N	HS_D3P	HS_D3N	HS_CP	HS_CN	HS_D2P	HS_D2N	HS_D1P	HS_D1N	
	110	HS_D3P	HS_D3N	HS_D2P	HS_D2N	HS_CP	HS_CN	HS_D1P	HS_D1N	HS_D0P	HS_D0N	
	111	HS_D3P	HS_D3N	HS_D0P	HS_D0N	HS_CP	HS_CN	HS_D1P	HS_D1N	HS_D2P	HS_D2N	默认
0	000	HS_D2N	HS_D2P	HS_D3N	HS_D3P	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D0N	HS_D0P	
	001	HS_D0N	HS_D0P	HS_D3N	HS_D3P	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D2N	HS_D2P	
	010	HS_D3N	HS_D3P	HS_D2N	HS_D2P	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P	
	011	HS_D3N	HS_D3P	HS_D0N	HS_D0P	HS_CN	HS_CP	HS_D2N	HS_D2P	HS_D1N	HS_D1P	
	100	HS_D2N	HS_D2P	HS_D3N	HS_D3P	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P	
	101	HS_D0N	HS_D0P	HS_D3N	HS_D3P	HS_CN	HS_CP	HS_D2N	HS_D2P	HS_D1N	HS_D1P	
	110	HS_D3N	HS_D3P	HS_D2N	HS_D2P	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D0N	HS_D0P	
	111	HS_D3N	HS_D3P	HS_D0N	HS_D0P	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D2N	HS_D2P	

外部连接 IM[3:0]	Interface	Connect Pin
1111	MIPI	HS_DN,HS_DP,HS_CN,HS_CP,RSTN
1110	RGB 16/18/24-bit	DB[15/17/23:0],VSYNC_QSPI_DIN2,HSYNC,DE_QSPI_DIN3,PCLK
1101	SPI 4wire/8bits RGB	DIN_SDA(MISO),DIN_SDA_DUAL(MOSI),RS(D/CX),SCL,CSX,RSTN
1100	spi 3wire 9bits	DIN_SDA(MISO),DIN_SDA_DUAL(MOSI),SCL,CSX,RSTN
1011	SPI 4wire 8bits dual data lane	DIN_SDA,DIN_SDA_DUAL,RS(D/CX),SCL,CSX,RSTN
1010	MCU 8080 8bits	DB[7:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN3(WRX),PCLK(RDX),RSTN
1001	MCU 8080 9bits	DB[8:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN3(WRX),PCLK(RDX),RSTN
1000	MCU 8080 16bits	DB[15:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN4(WRX),PCLK(RDX),RSTN
0111	MCU 8080 18bits	DB[17:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN
0110	SPI 3wire 9 bits dual lane	DIN_SDA,DIN_SDA_DUAL,SCL,CSX,RSTN
0101	QSPI	DE_QSPI_DIN3,VSYNC_QSPI_DIN2,DIN_SDA,DIN_SDA_DUAL,SCL,CSX,RSTN
0010	MCU 8080 8bits modeII	DB[17:10],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN
0001	MCU 8080 9bits modeII	DB[17:9],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_

		DIN5(WRX),PCLK(RDX),RSTN

4 INSTRUCTIONS

4.1 Outline

The AXS15260 supports high speed serial interface, MIPI, to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00. Updating command instructions can also be accomplished by using all supporting system interfaces.

The AXS15260 has the following major categories of instructions:

(1). User Command List and Description.

(2). Manufacturer Command List and Description.

Since updating these instructions is asynchronous to the internal clock of the AXS15260, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents of this chapter will describe the supported instructions in detail.

4.2 User Command List and Description

4.2.1 Introduction

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state. The commands 10h, 20h, 21h, 28h, 29h, 36h will be updated only during V-sync periods while the module is in the “Sleep Out” mode to avoid abnormal visual effects, and will be updated immediately in the “Sleep In” mode.

4.2.2 System Command List

Name	Hex	Write/Read Command	Description	Parameter Number	Transmission
NOP	00h	C	No operation	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
SWRESET	01h	C	Software reset	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDID	04h	R	Read display	4	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDNUMED	05h	R	Read Number of the Errors on DSI	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDST	09h	R	Read display status	4	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDPM	0Ah	R	Read display power	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDMADCTL	0Bh	R	Read memory data access control	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDIPF	0Ch	R	Read Interface Pixel Format	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDIM	0Dh	R	Read display image	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDSM	0Eh	R	Read display signal	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDSDR	0Fh	R	Read display self-diagnostic result	1	MIPI/QSPI/DSPI/SPI/RGB/MCU

SLPIN	10h	C	Sleep in	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
SLPOUT	11h	C	Sleep out	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
PTLON	12h	C	Partial mode on	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
NORON	13h	C	Partial mode off(Normal)	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
INVOFF	20h	C	Display inversion off	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
INVON	21h	C	Display inversion on	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
DISPOFF	28h	C	Display off	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
DISPON	29h	C	Display on	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
CASET	2Ah	W	Column address set	4	MIPI/QSPI/DSPI/SPI/MCU
RASET	2Bh	W	Row address set	4	MIPI/QSPI/DSPI/SPI/MCU
PTLAR	30h	W	Partial start/end address set	4	MIPI/QSPI/DSPI/SPI/RGB/MCU
PTLAR	31h	W	set_partial_columns	4	MIPI/QSPI/DSPI/SPI/RGB/MCU
VSCRDEF	33h	W	Vertical scrolling definition	6	MIPI/QSPI/DSPI/SPI/MCU
TEOFF	34h	C	Tearing effect line off	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
TEON	35h	W	Tearing effect line on	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
MADCTL	36h	W/R	Memory data access control	1	MIPI/QSPI/DSPI/SPI/MCU
VSCRSADD	37h	W	Vertical scrolling start address	2	MIPI/QSPI/DSPI/SPI/MCU
IDMOFF	38h	C	Idle mode off	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
IDMON	39h	C	Idle mode on	0	MIPI/QSPI/DSPI/SPI/RGB/MCU
IPF	3Ah	W	Interface pixel format	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
TESCAN	44h	W	Set tear scanline	4	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDTESCAN	45h	R	Get tear scanline	4	MIPI/QSPI/DSPI/SPI/RGB/MCU
WRDISBV	51h	W	Write display brightness value	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDDISBV	51h/52h	R	Read display brightness value	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
WRCTRLD	53h	W	Write CTRL display	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDCTRLD	54h	R	Read CTRL dsiplay	1	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDFCHKSUM	Aah	R	Read First Checksum	2	MIPI/QSPI/DSPI/SPI/RGB/MCU
RDCCHKSUM	Afh	R	Read Continue Checksum	2	MIPI/QSPI/DSPI/SPI/RGB/MCU

4.2.2.1 User Command Description

4.2.2.1.1 SWRESET (01H): Software Reset

8'H01	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters; Soft reset of the drv. If cr_soft_rstn_tp_opt=0, TP soft reset resets drv. If cr_soft_rstn_tp_opt=1, TP soft reset does not reset drv. When the TP register cr_soft_rstn_drv_opt=0, DRV soft reset can reset TP. When the TP register cr_soft_rstn_drv_opt=1, DRV soft reset non-resettable TP.								

4.2.2.1.2 ICI (04H): IC Information

8'HC0	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_manufacture_id								8'h00
Par1	-	↑	cr_driver_version_id								8'h00
Par2	-	↑	cr_driver_id								8'h00
Par3	-	↑	cr_id_dummy								8'h00
Description			cr_manufacture_id：the manufacture_id of the IC. cr_driver_version_id：the version_id of the IC. cr_driver_id：the IC id. cr_id_dummy：is cr_id_dummy_rev0,the dummy id0 that reserved. See the C0 command for details on the above registers.								

4.2.2.1.3 RDNUMED (05H): Read Number of the Errors on DSI

8'H05	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	dsi_err_overflow	dsi_err_num							8'h00
Description			The first parameter is telling a number of the errors on DSI. When register cr_ecc_en=1, enable the mipi ecc function. When register cr_mipi_crc_en=1, the mipi crc function is enabled. dsi_err_num：ecc error number +crc error num dsi_err_overflow：dsi err num Indicates the overflow flag bit.								
			Readable error status (ECC and CRC)								

4.2.2.1.4 RDDST (09H): Read Display Status

8'H09	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	booster_en	cr_my	cr_mx			cr_bgr	cr_ca	cr_gs	8'h40
Par1	-	↑		rgb_format_new			idle_mode	cr_partial_en	pwr_on	normal_dsp_en	8'h70
Par2	-	↑	cr_vscroll_en		src_inv			dsp_on	tear_on		8'h00

Par3	-	↑			cr_tear_mode						8'h00
Description	Read back command(21/20/36/10/11/28/29/3a) rgb_format_new: indicates the actual pixel format booster_en: charge pump Enables the booster function (vgh/vgl/vsp/vsn). idle_mode: 38/39h command flag. This bit is 1 when the 39h command is executed and 0 when the 38h command is executed. cr_partial_en: Part of the enable flag is displayed. The bit is 1 when the 12h command is executed and 0 when the 13h command is executed. normal_dsp_en: the opposite of cr_partial_en; pwr_on: indicates that the bit is 1 when the 11 command is executed, and the bit is 0 when the 10 command is executed. cr_vscroll_en: 33/37h Indicates that the running lamp function is enabled. 1 indicates that the running lamp function is enabled. src_inv: indicates the reverse flag bit of 0 and 1. If the flag bit is 1, the 21h command is executed. If the flag bit is 0, the 20 command is executed. dsp_on: indicates that the bit is 1 when the command is executed 29 and 0 when the command is executed 28. tear_on: This bit is set to 1 for issuing 35 and 0 for issuing 34. cr_tear_mode: 1 indicates that TE is H-blanking+V-blanking; 0 indicates that TE is V-blanking.										

4.2.2.1.5 RDDMADCTL (0AH): Read Display MADCTL

8'H0A	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	booster_en	idle_mode	cr_partial_en	pwr_on	normal_dsp_en	dsp_on	-	-	8'h00
Description	booster_en: Enables the charge pump function. idle_mode: 38/39h command flag. This bit is 1 when the 39h command is executed and 0 when the 38h command is executed. pwr_on: indicates that the bit is 1 when the 11 command is executed, and the bit is 0 when the 10 command is executed. cr_partial_en: Part of the enable flag is displayed. The bit is 1 when the 12h command is executed and 0 when the 13h command is executed. normal_dsp_en: the opposite of cr_partial_en; dsp_on: indicates that the bit is 1 when the command is executed 29 and 0 when the command is executed 28.										

4.2.2.1.6 RDDMADCTL (0BH): Read Display MADCTL

8'H0B	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_my	cr_mx			cr_bgr	cr_mh			8'h00
Description	Read back the parameters of command word 36h.										

4.2.2.1.7 RDDCOLMOD(0CH): Read Display Pixel Format

8'H0C	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	0	dpi_format			0	dbi_format			8'h77
Description	Read back the parameters of command word 3Ah. dpi_format: video format rgb/mipi pixel format. dbi_format: command format pixel format of dbi, spi, and qspi interfaces										

4.2.2.1.8 RDDMADCTL (0DH): Read Display MADCTL

8'H0D	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_vscroll_en		src_inv						8'h00
Description	Read back 21/20h cr_vscroll_en: 33/37h Indicates that the running lamp function is enabled. 1 indicates that the running lamp function is enabled. src_inv: indicates the reverse flag bit of 0 and 1. If the flag bit is 1, the 21h command is executed. If the flag bit is 0, the 20 command is executed.										

4.2.2.1.9 RDDSM (0Eh): Read Display Signal Mode

8'H0E	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	tear_on	cr_tear_mode	cr_hs_flag	cr_vs_flag	cr_pclk_flag	cr_de_flag	0	dsi_err_en	8'h00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,
HS	Horizontal Sync (RGB interface)	'1' = ON, '0' = OFF,
VS	Vertical Sync (RGB interface)	'1' = ON, '0' = OFF,
PixelClk	Pixel Clock (DOTCLK, RGB interface)	'1' = ON, '0' = OFF,
DataEn	Data Enable (DE, RGB interface)	'1' = ON, '0' = OFF,
ErrorDSI	Error On DSI (MIPI Interface)	'1' = Error, '0' = No Error

4.2.2.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

8'H0F	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par1	-	↑	otp_crc_done	ctn_crc_done	0					otp_crc_ok	8'h00
Description	This command indicates the current status of the display self-diagnostic result after sleep out command as described (test function) below: otp_crc_done: The otp is loaded and the crc check is complete ctn_crc_done: The host reconfigures the register and the crc check ends otp_crc_ok:otp Checksums Comparison, '0' = Checksums are same, '1' = Checksums are not same See sections: "Read First Checksum (Aah)" and "Read Continue Checksum (Afh)"										

4.2.2.1.11 POFF (10H): Power Off Command

8'H10	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description	power off command(10) with no parameter is used to turn off power										

4.2.2.1.12 PON (11H): Power On Command

8'H11	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			power on command(11) with no parameter is used to turn on power								

4.2.2.1.13 PTLON (12H): Partial Display Mode On

8'H12	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters; Enable the partial display function, that is, cr_partial_en =1. The upper and lower boundary positions of the local display area are determined by the 30H command word. The left and right boundary of the local display area is determined by 31H command word. Local display area (within the boundary position) shows normal picture content; The contents of the non-local display area (outside the boundary position) are configured by registers (cr_partial_value_r, cr_partial_value_g, cr_partial_value_b).								

4.2.2.1.14 NORON (13H): Normal Display Mode On（Partial mode off）

8'H13	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters; Disable the partial display function and switch to the normal display mode, that is, cr_partial_en =0.								

4.2.2.1.15 NSI (20H): No Src_Inv Command

8'H20	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			no src_inv command(20) with no parameter is used to exit the invertion of black and white picture								

4.2.2.1.16 SI (21H): Src_Inv Command

8'H21	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			src_inv command(21) with no parameter is used to enter the invertion of black and white picture								

4.2.2.1.17 DOFF (28H): Display Off Command

8'H28	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			display off command(28) with no parameter is used to turn off display								

4.2.2.1.18 DON (29H): Display On Command

8'H29	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			display on command(29) with no parameter is used to turn on display								

4.2.2.1.19 CWA (2AH): Column Windows Address Command

8'H2a	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-						cr_2a_sc_rx[10:8]			8'h00
Par1	↑	-	cr_2a_sc_rx[7:0]								8'h00

Par2	↑	-						cr_2a_ec_rx[10:8]	8'h00
Par3	↑	-	cr_2a_ec_rx[7:0]						8'h00
Description	When cr_win_en =1 of command table2, windowing functions 2a and 2b are effective; cr_2a_sc_rx: represent row/column start/stop address in command mode display cr_2a_ec_rx: represent row/column start/stop address in command mode display;								

4.2.2.1.20 RWA (2BH): Row Windows Address Command

8'H2b	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-					cr_2b_sr_rx[11:8]				8'h00
Par1	↑	-	cr_2b_sr_rx[7:0]								8'h00
Par2	↑	-					cr_2b_er_rx[11:8]				8'h00
Par3	↑	-	cr_2b_er_rx[7:0]								8'h00
Description	cr_2b_sr_rx: represent row/column start/stop address in command mode display; cr_2b_er_rx: represent row/column start/stop address in command mode display;										

4.2.2.1.21 PTLAR (30H):set_partial_rows

8'H30	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-					cr_partial_strrow[11:8]				8'h00
Par1	↑	-	cr_partial_strrow[7:0]								8'h00
Par2	↑	-					cr_partial_endrow[11:8]				8'h00
Par3	↑	-	cr_partial_endrow[7:0]								8'h00
Description	cr_partial_strrow [11:0]: Locally displays the start row. cr_partial_endrow [11:0]: locally displays the endrow.										

4.2.2.1.22 PTLAR (31H):set_partial_columns

8'H31	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-						cr_partial_strcol[10:8]			8'h00
Par1	↑	-	cr_partial_strcol[7:0]								8'h00
Par2	↑	-						cr_partial_endcol[10:8]			8'h00
Par3	↑	-	cr_partial_endcol[7:0]								8'h00
Description	cr_partial_strcol [10:0]: locally displays the start column; cr_partial_endcol [10:0]: locally displays the end column.										

4.2.2.1.23 SA (33H): Scroll Area Command

8'H33	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-	cr_33_tfa[15:8]								8'h00
Par1	↑	-	cr_33_tfa[7:0]								8'h00
Par2	↑	-	cr_33_vsa[15:8]								8'h00
Par3	↑	-	cr_33_vsa[7:0]								8'h00

Par4	↑	-	cr_33_bfa[15:8]	8'h00
Par5	↑	-	cr_33_bfa[7:0]	8'h00
Description			If command table2 is cr_vscroll_en =1, the running lamp function is effective. cr_33_tfa: indicates the top fix area. cr_33_vsa: vertical scroll area. cr_33_bfa: bottom fix area.	

4.2.2.1.24 TEOFF (34H): Tearing Effect Line OFF

8'H34	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters, Disables Tearing Effect output signal from TE signal line, i.e. tear_on = 0.								

4.2.2.1.25 TEON (35H): Tearing Effect Line On

8'H35	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-								cr_tear_mode	8'h00
Description			Issue 35h, i.e. tear_on = 1, Tearing Effect Line On. TEM Determining the Tearing Effect Output Line mode. 1. TEM =0: The Tearing Effect output line consists of V-Blanking information only. 2. TEM =1: The Tearing Effect output Line consists of both V-Blanking and H-Blanking information. The TE of H-blanking is determined by C5 of command table2: cr_te_gsps: start column position; cr_te_gspf: indicates the end column position.								

4.2.2.1.26 DCTR (36H): Display Control Command

8'H36	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑		MY	MX			BGR	MH	cr_ca	cr_gs	8'h00

Description

cr_gs: gip scan direction setting.

cr_gs	cr_fv	result
0	0	FW, select D7 and D8 register groups
0	1	BW, select D9 and DD register groups
1	0	FW, select D7 and D8 register groups
1	1	BW, select D9 and DD register groups

cr_ca: the data invert option for data_shift block.

dsh_shr = cr_dsh_shr ^ cr_ca ^ cr_mx ^ cr_mh

(when dsh_shr = 0, invert; when dsh_shr = 1, don't invert).

cr_dsh_shr	cr_ca	cr_mx=MX^ cr_36_opt[1]	cr_mh=MH^ cr_36_opt[4]	result
0	0	0	0	Normal
0	0	0	1	Left and right mirror
0	0	1	0	Left and right mirror
0	0	1	1	Normal
0	1	0	0	Left and right mirror
0	1	0	1	Normal

0	1	1	0	Normal
0	1	1	1	Left and right mirror
1	0	0（default）	0（default）	Left and right mirror
1	0	0	1	Normal
1	0	1	0	Normal
1	0	1	1	Left and right mirror
1	1	0	0	Normal
1	1	0	1	Left and right mirror
1	1	1	0	Left and right mirror
1	1	1	1	Normal

BGR：sub_pixel order of one pixel data setting，

cr_bgr_before_en	cr_bgr_en	BGR	cr_bgr_opt	result
0	0	0	0	RGB
0	0	0	1	RGB
0	0	1	0	RGB
0	0	1	1	RGB
0	1	0	0	RGB
0	1	0	1	BGR
0	1	1	0	BGR
0	1	1	1	RGB
1	0	0	0	RGB
1	0	0	1	BGR
1	0	1	0	BGR
1	0	1	1	RGB
1	1	0	0	RGB
1	1	0	1	RGB
1	1	1	0	RGB
1	1	1	1	RGB

MX：Left and right mirror, as cr ca, see cr ca for details.

MH：Left and right mirror, as cr ca, see cr ca for details.

MY：Up and down mirror

MY	cr_36_opt[0]	result
0	0（default）	Normal
0	1	Up and down mirror
1	0	Up and down mirror
1	1	Normal

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel
MH	Horizontal Refresh Order	Horizontal direction '0' = Left to Right '1' = Right to Left

4.2.2.1.27 SS (37H): Scroll Start Command

8'H37	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-	cr_37_vsp[15:8]								8'h00
Par1	↑	-	cr_37_vsp[7:0]								8'h00
Description			**cr_37_vsp**：vertical scroll position.								

4.2.2.1.28 IDMOFF (38H): Idle Mode Off

8'H38	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters, The Idle mode is displayed.								

4.2.2.1.29 IDMON (39H): Idle mode on

8'H39	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default

Description			Without parameters,
			The Idle mode is displayed, that is, the eight-color mode.
			Register configuration is as follows
			vedio mode: cr_idle_mode_en = 1
			command mode:
			cr_idle_mode_en=1;
			cr_corr_col_en = 0;
			cr_gray_high = 'h80.								

4.2.2.1.30 COLMOD (3AH): Interface Pixel Format

8'H3A	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-	-	dpi_format[2:0]			-	dbi_format [2:0]			8'h77
Description			This command is used to **define the format of RGB picture data**, which is to be transferred **via the MCU interface**. If the customized register cr_format_cmd3a_dpi_en=1 or cr_format_cmd3a_dbi_en=1, the pixel format is configured by the 3Ah command. Otherwise, the pixel format is configured by cr_pix_format For mipi format, cr_pix_sel is set to 1								

dpi_format[2:0]: DPI Pixel Format Definition（RGB）
dbi_format[2:0]: DBI Pixel Format Definition

The formats are shown in the table:

Bit	Description	
D7	-	Set to '0'
D6	RGB interface color format	'101' = 16bit/pixel '110' = 18bit/pixel
D5		
D4		
D3	-	Set to '0'
D2	Control interface color format	'101' = 16bit/pixel '110' = 18bit/pixel '111' = 24 bit/pixel
D1		
D0		

Deault: 16bits/pixel

4.2.2.1.31 STE (44H): Set Tear Scanline

8'H44	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-					cr_44te_str[11:8]				8'h00
Par1	↑	-	cr_44te_str[7:0]								8'h00
Par2	↑	-					cr_44te_end[11:8]				8'h00
Par3	↑	-	cr_44te_end[7:0]								8'h00
Description	-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV. -The tearing effect line on has one parameter that describes the tearing effect output line mode. -The tearing effect output line consist of V-blanking information only. Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0. The tearing effect output line shall be active low when the display module is in sleep mode。 cr_44te_str: start line; cr_44te_end: indicates the end line When the command table2 custom register cr_te_44en =1, the TE position is configured by the 44h command, otherwise it is determined by the cr_te_str and cr_te_end of command table2.										

4.2.2.1.32 GSCAN (45H): Get Scanline

8'H45	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑					cr_44te_str[11:8]				8'h00
Par1	-	↑	cr_44te_str[7:0]								8'h00
Par2	-	↑					cr_44te_end[11:8]				8'h00

Par3	-	↑	cr_44te_end[7:0]	8'h00
Description	-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. -When in sleep in mode, the value returned by get scanline is undefined. Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0. Read back the parameters of the 44 command			

4.2.2.1.33 BL (51H): Back Light Command

8'H51	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	↑	cr_bl_usr								8'h80
Description	**cr_bl:**Adjust the backlight. cr_bl [7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0' cr_bl [7:0] is manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1' ; This function is to adjust the duty ratio of PWM.										

4.2.2.1.34 RBL (52H): Read Display Brightness Value

8'H52	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_bl								8'h80
Description	This command returns the brightness value of the display.										

4.2.2.1.35 WRCTRLD (53H): Write CTRL Display

8'H53	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-			cr_blctrl_en		cr_dd	bl_en			8'h00
Description	This command is used to control display brightness. cr_blctrl_en: Brightness Control Block On/Off, BCTRL=1 indicates that the brightness control function is enabled. cr_dd: Display Dimming On/Off. DD=1 indicates that the backlight climbing function is enabled. bl_en: Backlight Control On/Off, BL=1 indicates turn on the backlight. BL=0 means turn off the backlight immediately										

4.2.2.1.36 RDCTRLD (54H): Read CTRL value Display

8'H54	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑			cr_blctrl_en		cr_dd	bl_en			8'h00
Description	This command returns ambient light and brightness control values. Read back the 53H command.										

4.2.2.1.37 RDFCS (AaH):Read First Checksum

8'HAa	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default

Par0	-	↑	fst_chk_sum[15:8]	8'hff
Par1	-	↑	fst_chk_sum[7:0]	8'hff
Description			This command returns the **first checksum** what has been calculated from **User's area registers** and **OTP** after the write access to those registers and/or has been done.	

4.2.2.1.38 RDCFCS (AfH):Read Continue Checksum

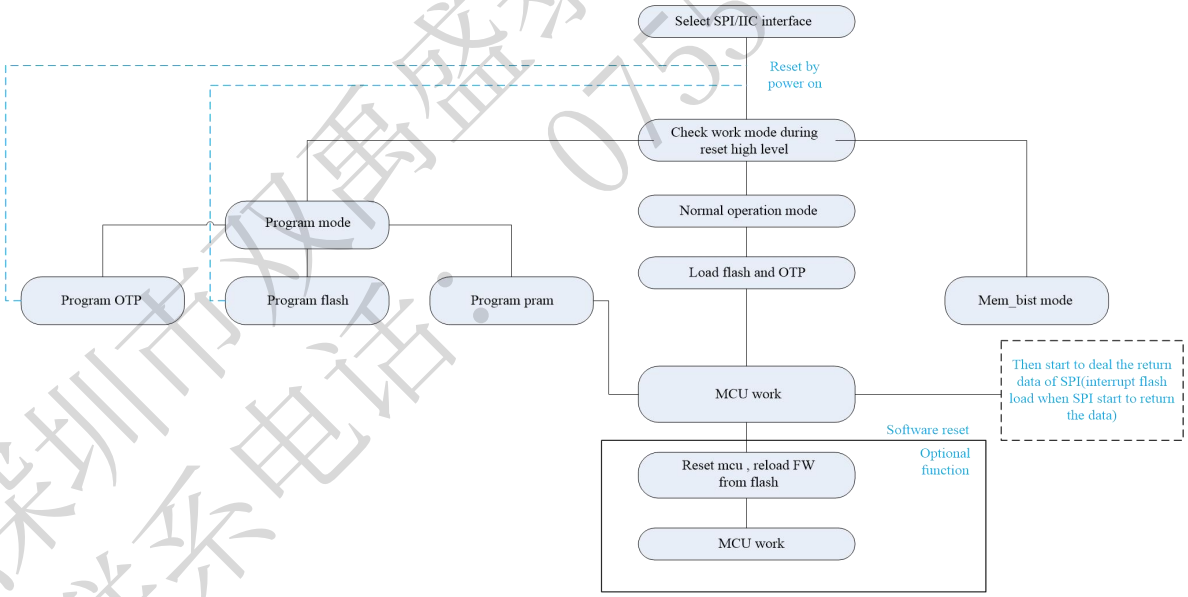
8'HAf	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	ctn_chk_sum[15:8]								8'hff
Par1	-	↑	ctn_chk_sum[7:0]								8'hff
Description			This command returns the **continue checksum** what has been **calculated continuously** after the first checksum has calculated from User's area registers and OTP after the write access to those registers and/or has been done.								

5 FUNCTIONS

5.1 Touch

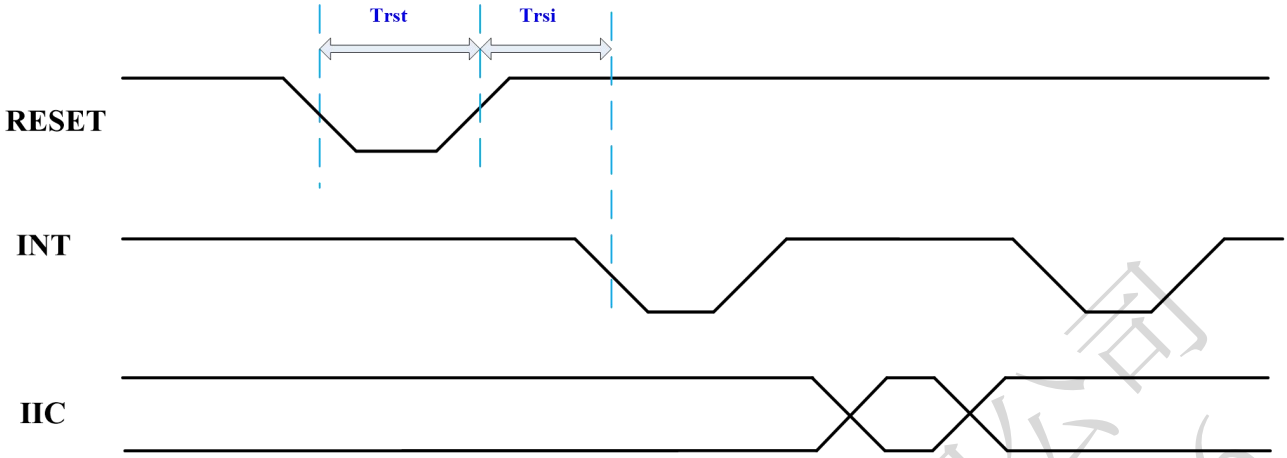
5.1.1 TP work flow

First, select the SPI or I2C interface to work through the work mode PIN. Then Write program into flash or pram with a different interface; Finally, please reset if writing program into flash or otp, and directly enter into MCU work mode if writing program into pram.



5.1.2 Touch Reset (RSTN) input timing

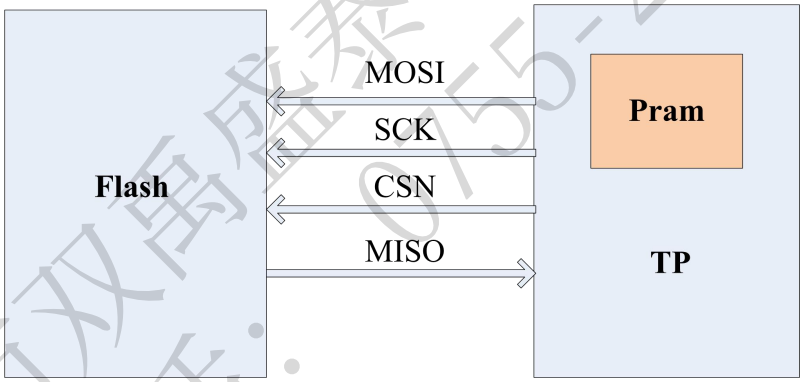
Reset time must be enough to guarantee reliable reset.



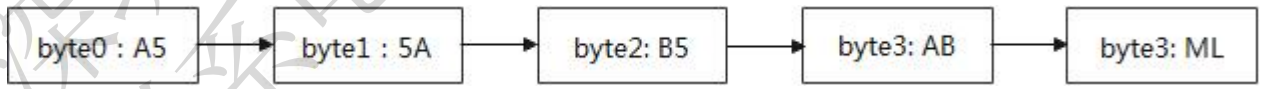
Parameter	Descrlption	Min	Max	Units
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	5	--	ms

5.1.3 Firmware booting

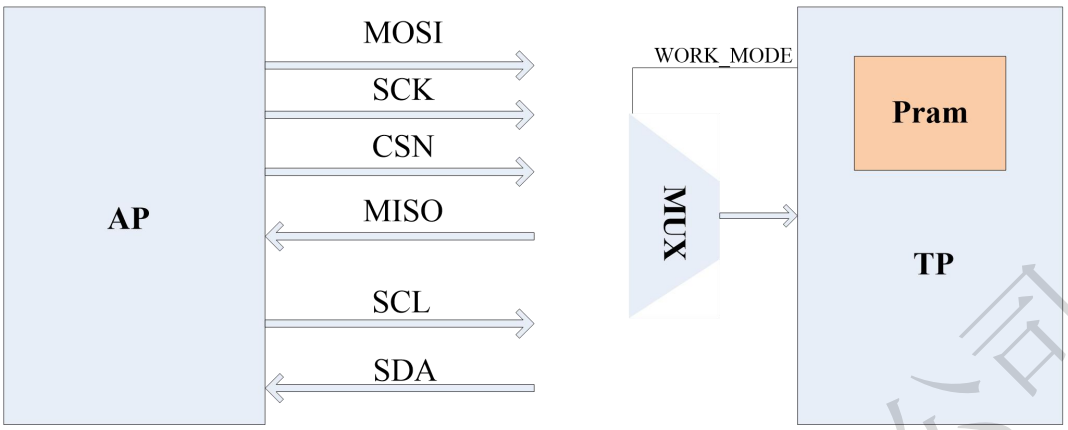
Touch firmware can boot from external flash or from AP optional, default is from external flash. Boot block diagram as follows.



Touch controller can also boot firmware from AP through I2C or SPI interface. booting firmware protocol as follows,



byte0~byte3 is character string, it means enable booting. and ML is mode flag. when ML=1, select boot firmware from the host. it is an optional to select I2C or SPI interface through WORK_MODE pin. When WORK_MODE = 1, I2C active, otherwise, SPI active.



5.2 Configure the color format of each interface

Color format				
Interface	cr_format_cmd3a_dpi_en=1 cr_format_cmd3a_dbi_en=X	cr_format_cmd3a_dpi_en=0 cr_format_cmd3a_dbi_en=1	cr_format_cmd3a_dpi_en=0 cr_format_cmd3a_dbi_en=0	
QSPI	iformat[2:0]=dpi_format (3ah: par0 的[6:4])	format[2:0]=dbi_format (3ah: par0 的[2:0])	format[2:0]=cr_pix_format (command table2)	format[2:0]=3'b111/3'b100:RGB88 format[2:0]=3'b101:RGB565 format[2:0]=3'b010:RGB332 format[2:0]=3'b001:RGB111 format[2:0]=3'b000:gray mode else：reserved
SPI				format[2:0]=3'b111:RGB888 else:RGB565
DBI				format[2:0]=3'b111/3'b110:RGB88 format[2:0]=3'b101:RGB565 format[2:0]=3'b100:RGB666 else：reserved
RGB				format[2:0]=3'b101:RGB565 format[2:0]=3'b100:RGB666 esle:RGB88

MIPI				format[2:0]=3‘b111:RGB888 format[2:0]=3‘b101:RGB565 format[2:0]=3‘b100:RGB666 else：reserved

5.3 MIPI-DSI Interface

Connect Pin:HS_DN,HS_DP,HS_CN,HS_CP,RSTN.The MIPI Interface is selected by setting the IM[3:0] pins as “1111” level.

5.3.1 General description

The communication can be separated into two different levels between the host and the display module:

– Interface Level: Low level communication, low power

– Packet level: High level communication, high speed

5.3.2 Interface level communication

5.3.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane can be drivern in Low Power (LP) or High Speed (HS) mode.

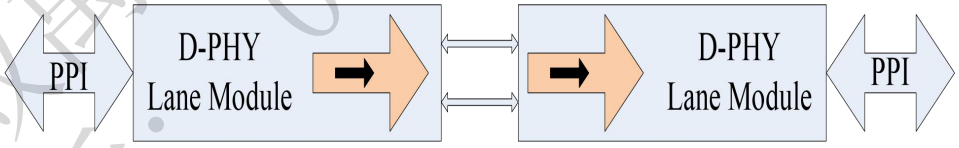
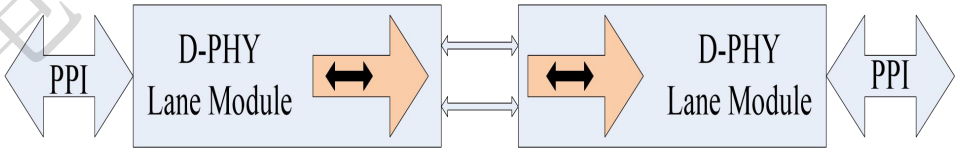
-	Lane support mode	MPU(Host) AXS15231(Slave)
Clock Lane	Unidirectional lane •High-Speed Clock only •SimplifiedEscape Mode (ULPS Only)	
Data Lane	Bi-directional lane • Forward high-speed only •Bi-directional Escape Mode •Bi-direction LPDT	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disabled (The termination resistor of the receiver is disable) and it can be drivern into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is

enabled) are not used in the single end mode.

There are different modes and protocols in each mode when transferring information from the HOST to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

5.3.2.2 DSI-CLK lanes

DSI-CLK+/- lanes can be drivern into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

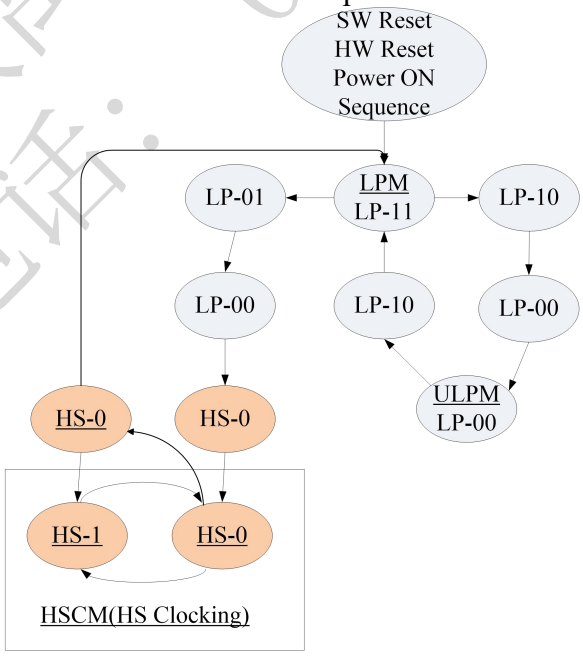


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be drivern to the Low Power Mode (LPM), when DSI-CLK lanes are entering the LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

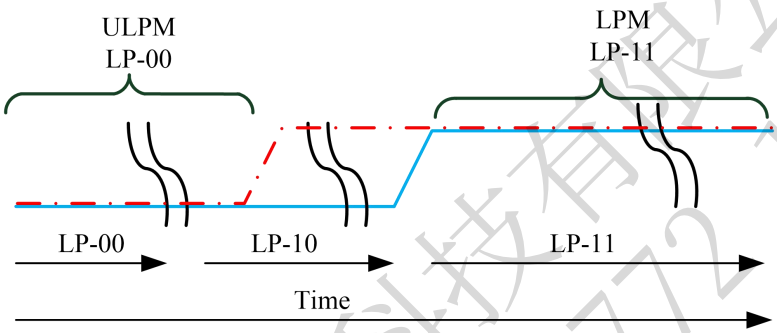


Figure:From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

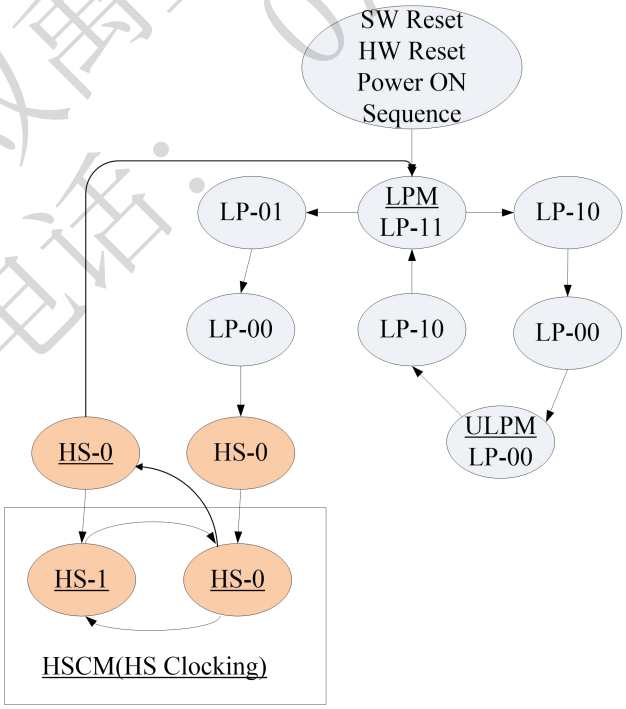


Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

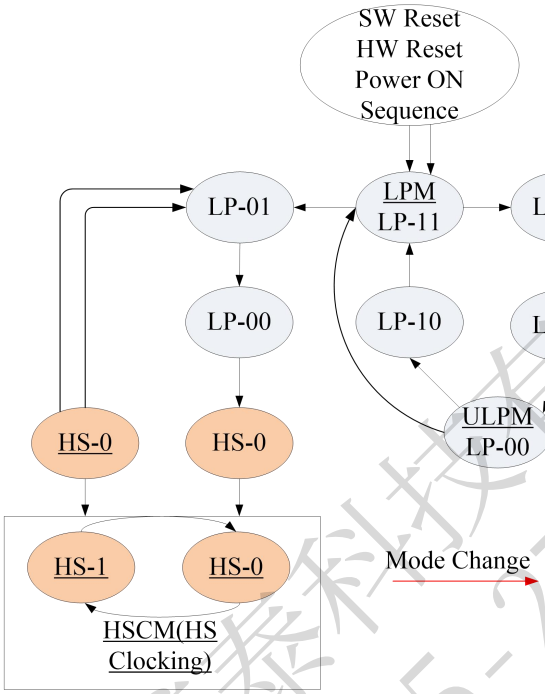


Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be drivern to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

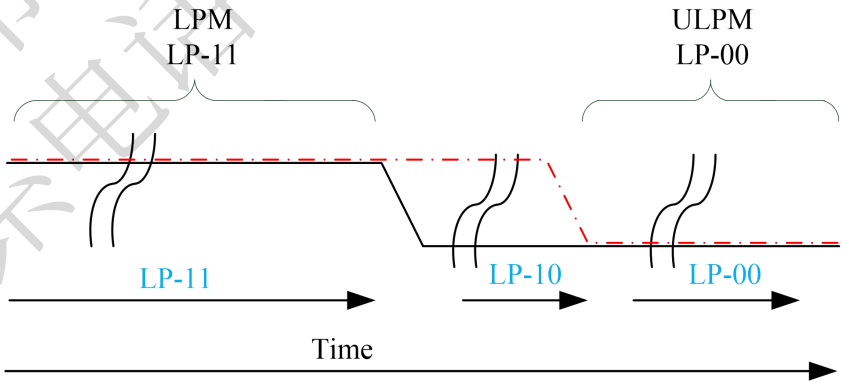


Figure: From LPM to UPLM

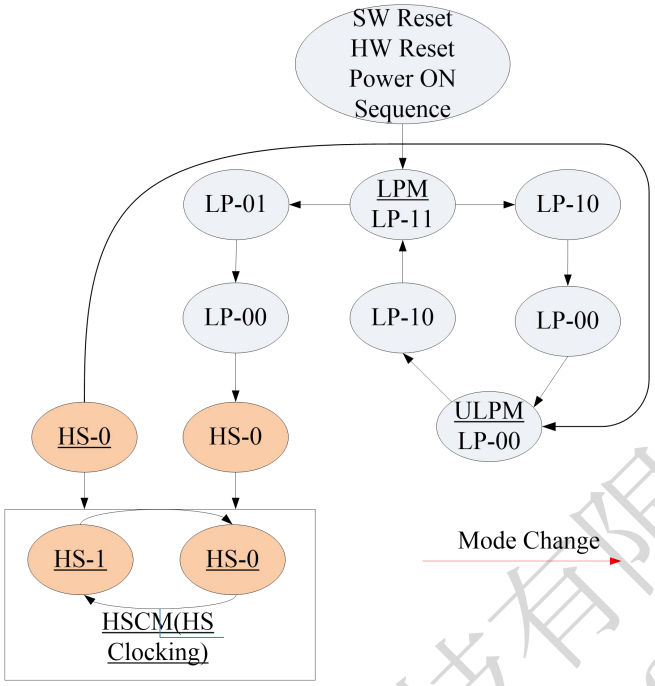


Figure:The mode change from LPM to UPLM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be drivern to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

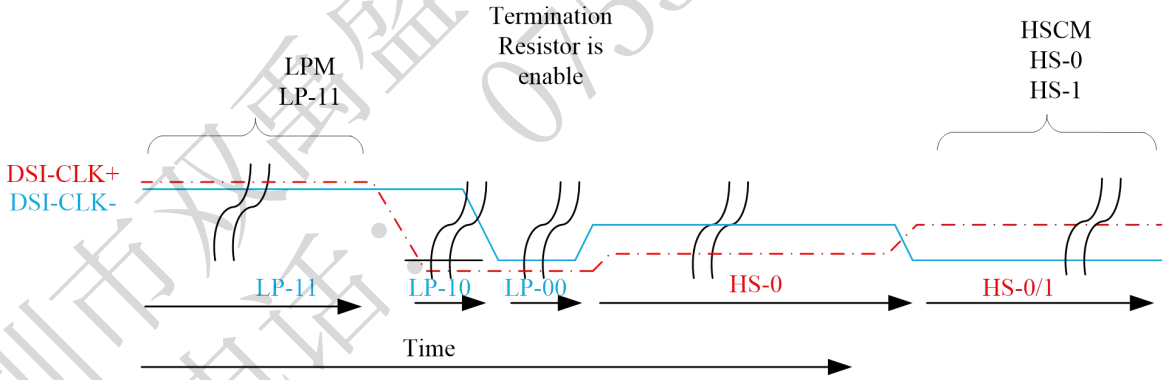


Figure: From LPM to HSCM

The mode change is also illustrated below:

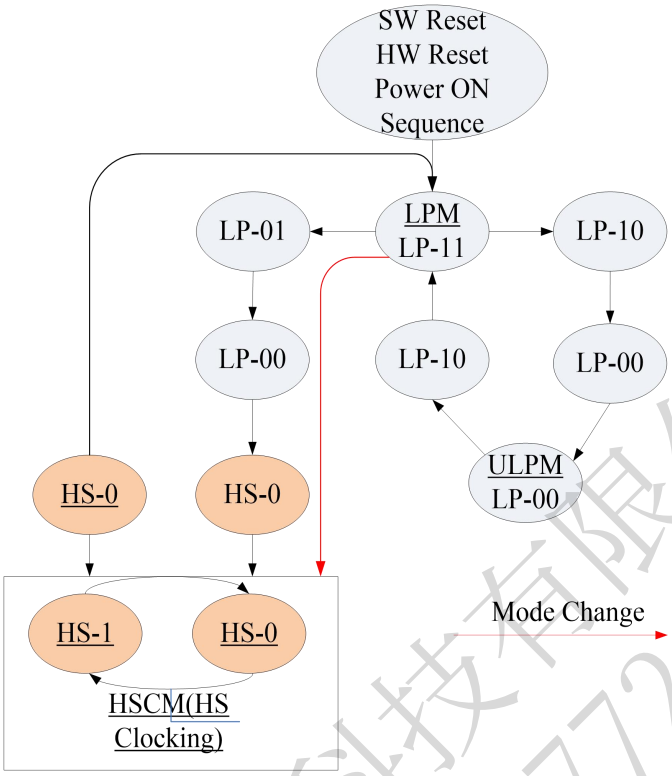


Figure:Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

– Even the number of transitions

– Start state is HS-0

– End state is HS-0

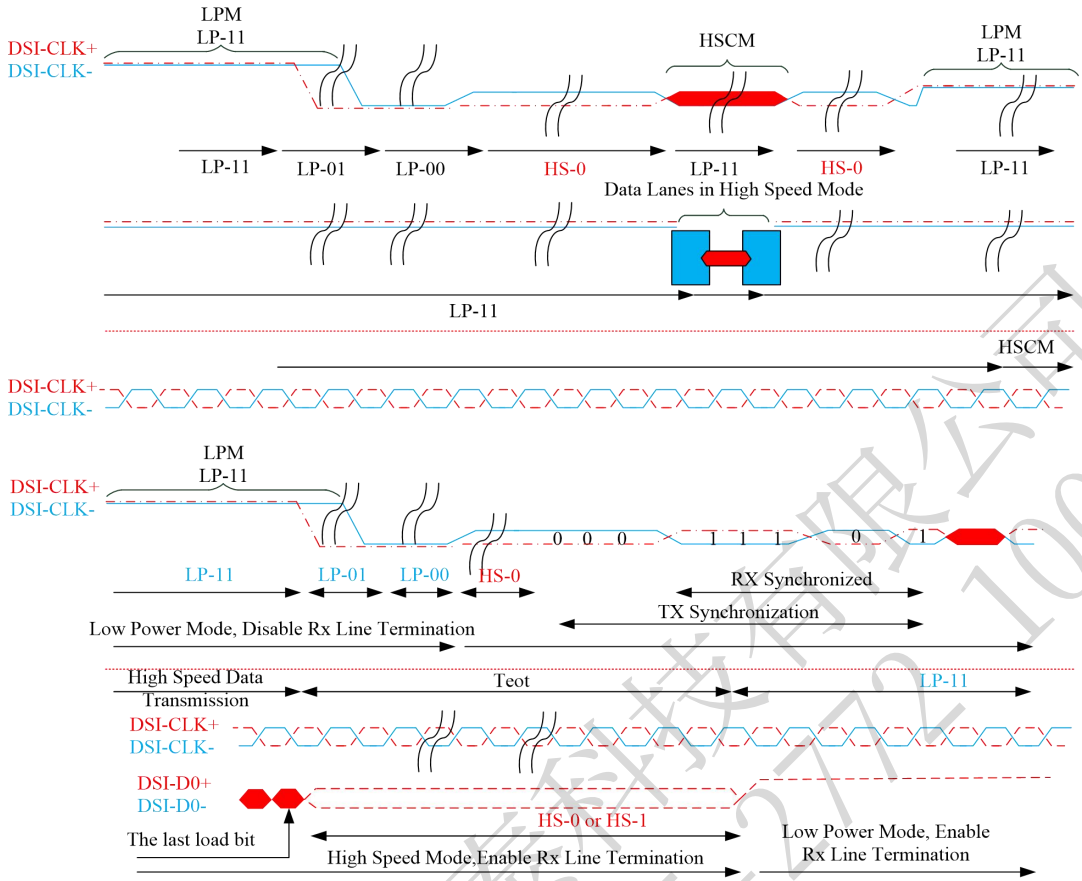


Figure: High speed clock burst

5.3.3 DSI data lanes

5.3.3.1 General

DSI-Dn+/- Data Lanes can be drivern in different modes which are:
– Escape Mode (only support DSI_D0 data lane pair)
– High-Speed Data Transmission (support all data lane pairs)
– Bus Turnaround Request (only support DSI_D0 data lane pair)
These modes and their entering codes are defined in the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	L P-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

5.3.3.2 Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode, some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follows

• Start: LP-11.

• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00.

• Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low, then this changed data lane is presenting a value of the current data bit.

• A payload stream if it is needed.

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11.

• End: LP-11.

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. All currently available Escape mode commands and actions are listed below.

• Send or receive “Low-Power Data Transmission” (LPDT).

• Driver data lanes to “Ultra-Low Power State” (ULPS).

• Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function).

• Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the HOST.

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the HOST.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn’t match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state. For Data Lane1 and 2, only support ULPS Escape mode commands.

• Driver data lanes to “Ultra-Low Power State” (ULPS).

The basic construction is illustrated below:

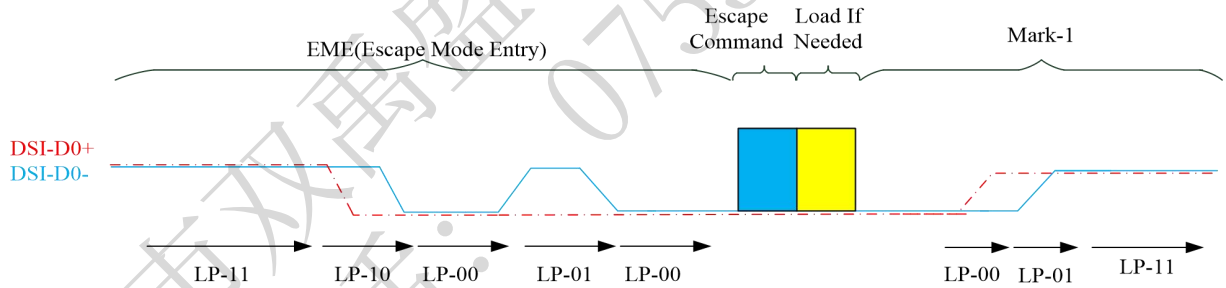


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided to 2 different groups: Mode or Trigger. Escape command and groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin

Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The HOST is inform the display module that it is controlling data lanes (DSI-D0+/-) with the Mode e.g. The HOST can inform the display module that it can put data lanes in the low power mode.

The HOST is waiting from the display module event information, which has been set by the HOST , with the Trigger e.g. when the display module reaches a new V-synch, the display module sent the HOST a TE trigger (TEE), if the HOST has been requested it.

Low-Power Data Transmission (LPDT)

The HOST can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the HOST .

The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Payload (Data):

- One or more bytes

- Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

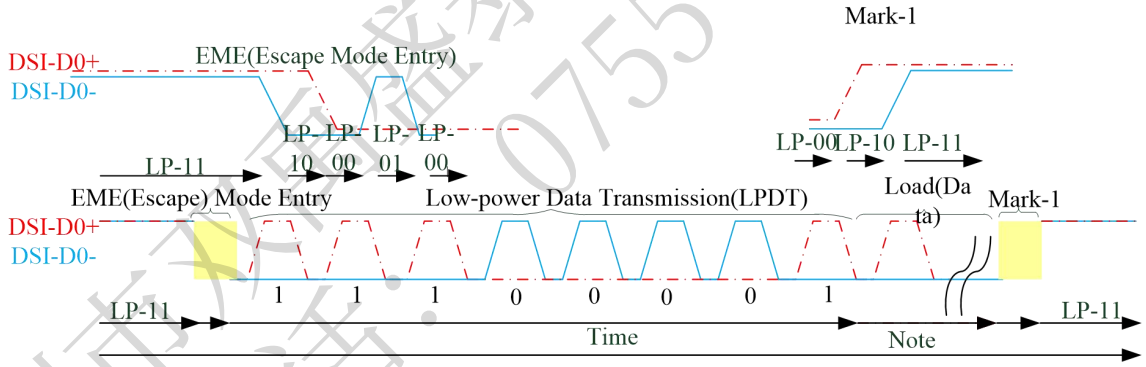


Figure: Low-power data transmission

Note: Load(Data) is presenting the first bit is logical “1” in this example

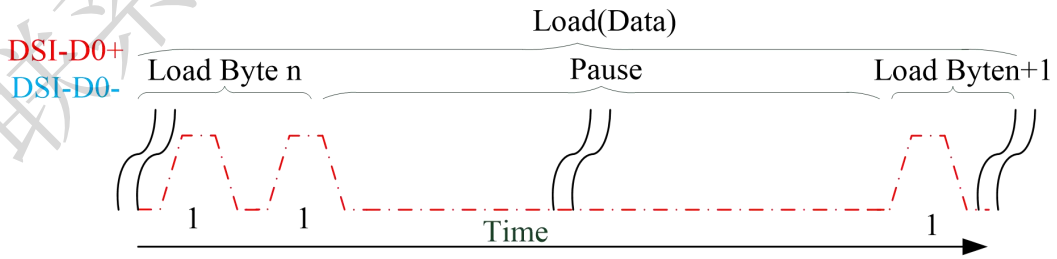


Figure: Pause (example)

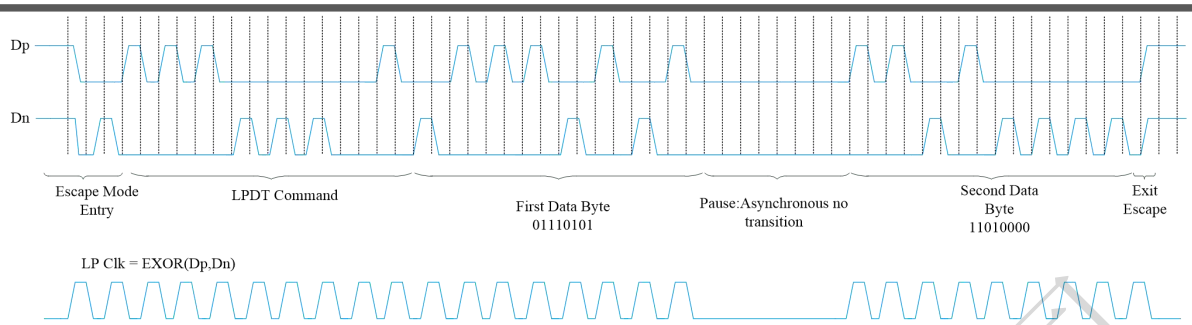


Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The HOST can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS)used/uses(?) the following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the HOST is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

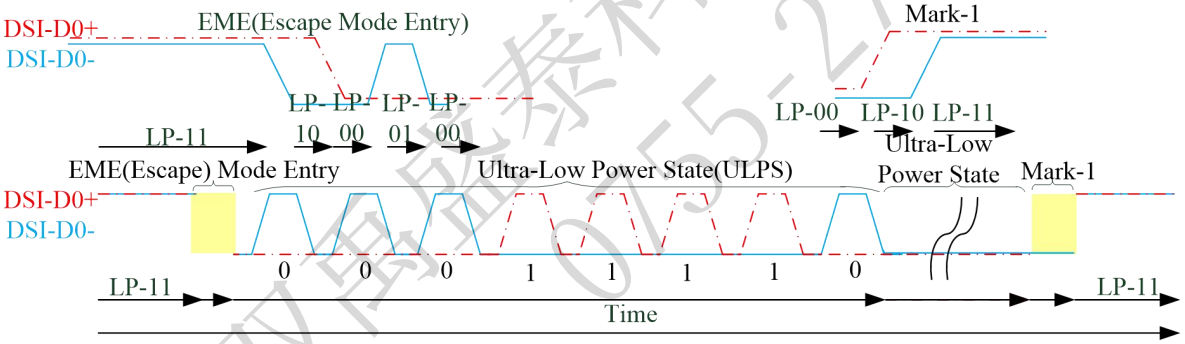


Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The HOST can inform the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset using the following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

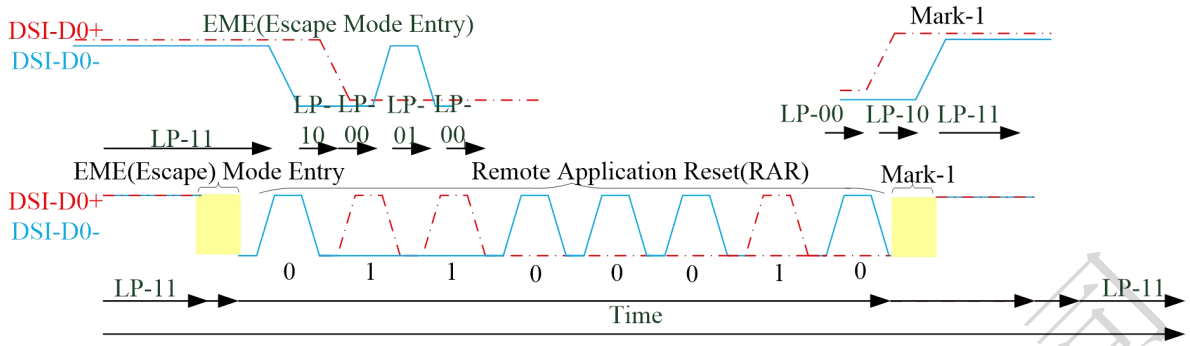


Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform the HOST when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

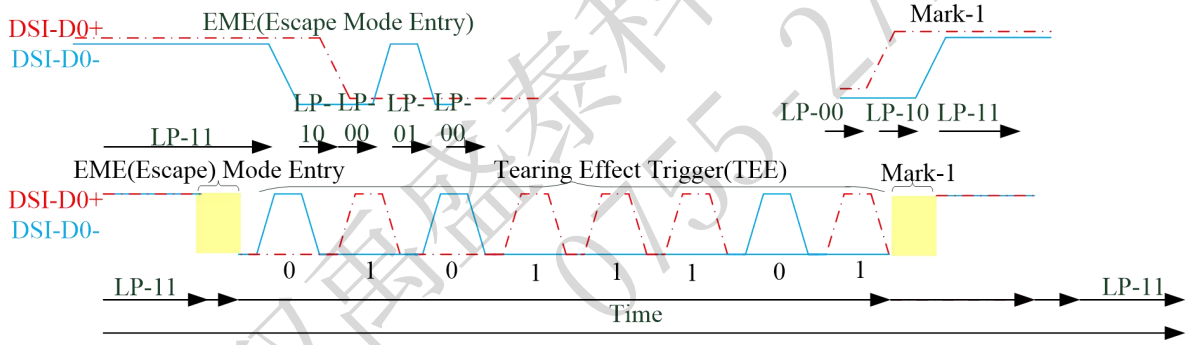


Figure: Tearing effect(TEE)

Acknowledgement (ACK)

The display module can inform the HOST when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) used/uses(?) the following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

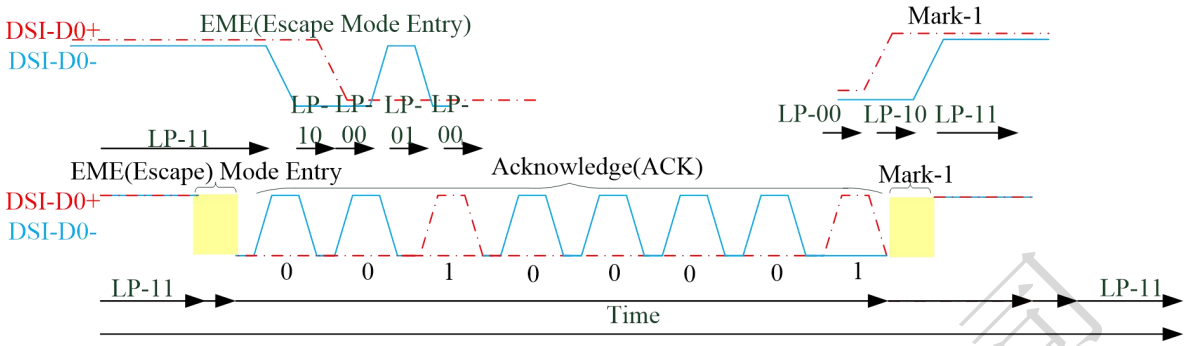


Figure: Acknowledgement (ACK)

5.3.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (Tsot of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the HighSpeed Clock Mode (HSCM) by the HOST. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follow

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= HOST) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

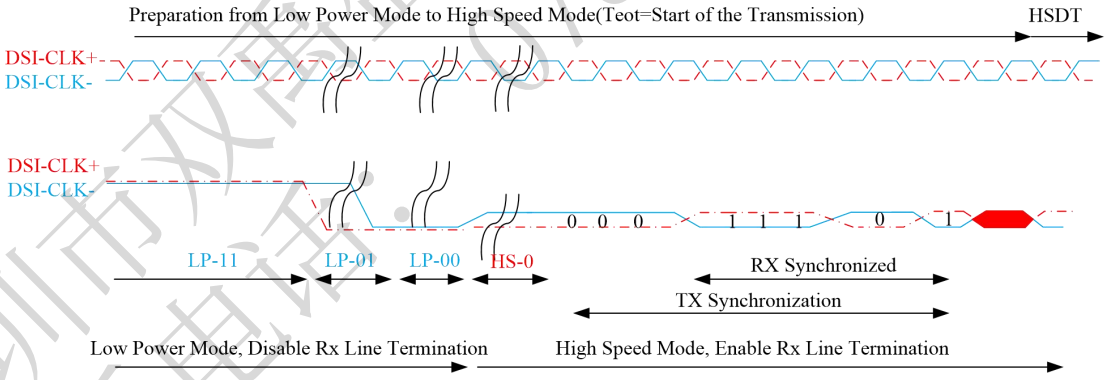


Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the HOST and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”. Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follow

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission

-HOST changes to HS-1, if the last load bit is HS-0

-HOST changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

The same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

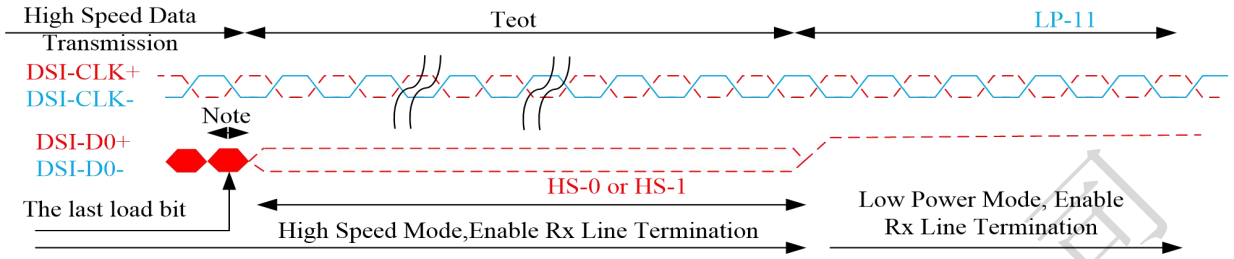


Figure: TEOT of HSDT

Note:
If the last load bit is HS0, the transmitter changes from HS0 to HS-1.
If the last load bit is HS1, the transmitter changes from HS1 to HS-0.

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "Short Packet (SPa) and Long Packet (LPa) Structures". These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

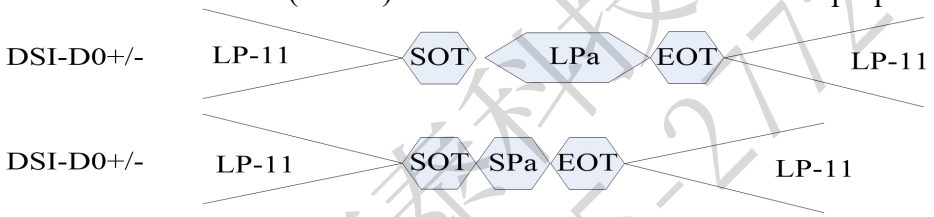


Figure: Single packet in HSDT

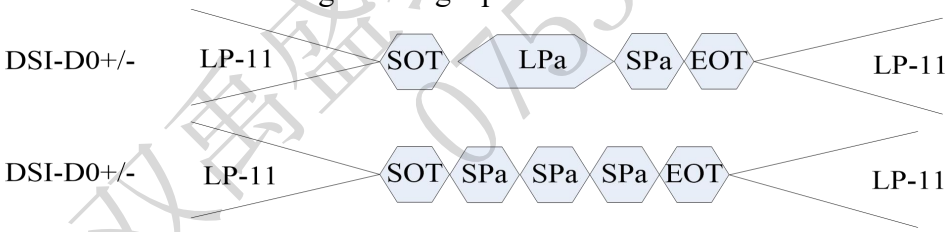


Figure: Multiple packets in HSDT

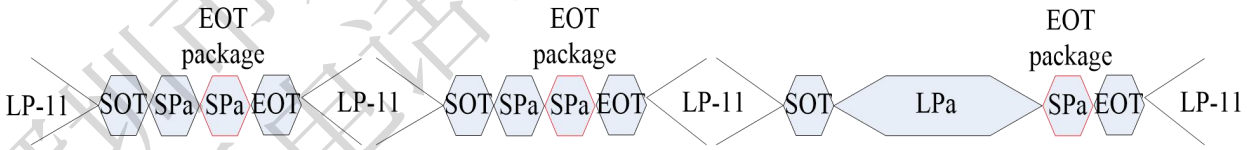


Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

5.3.3.4 Bus Turnaround (BTA)

The HOST or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information to a receiver.

The HOST and display module can use the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the HOST wants to do the bus turnaround procedure to the display module, as follows.

• Start (HOST): LP-11

• Turnaround Request (HOST): LP-11 =>LP-10 =>LP-00

• The HOST waits until the display module is starting to control DSI-D0+/- data lanes and the HOST stops to control DSI-D0+/- data lanes (= High-Z)

• The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the HOST to the display module) is illustrated below.

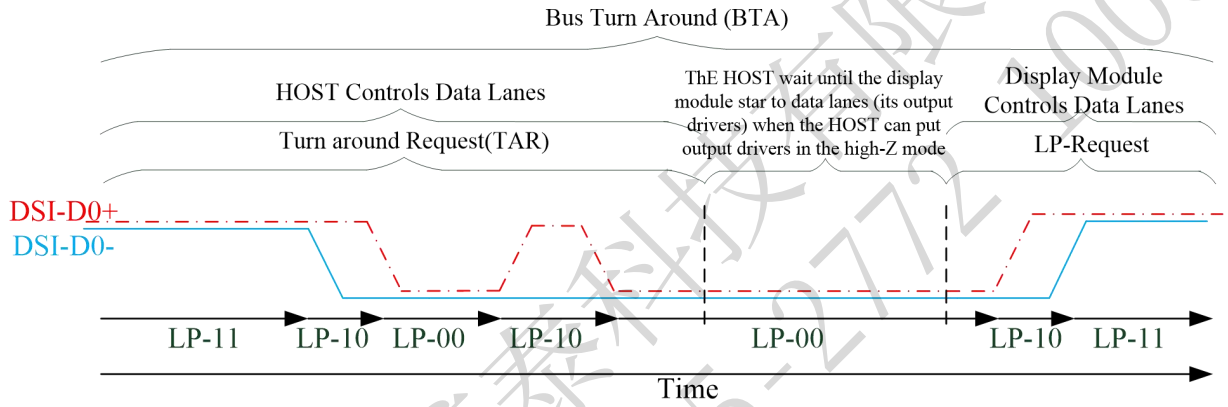


Figure: Bus turnaround procedure

5.3.4 Packet level communication

5.3.4.1 Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

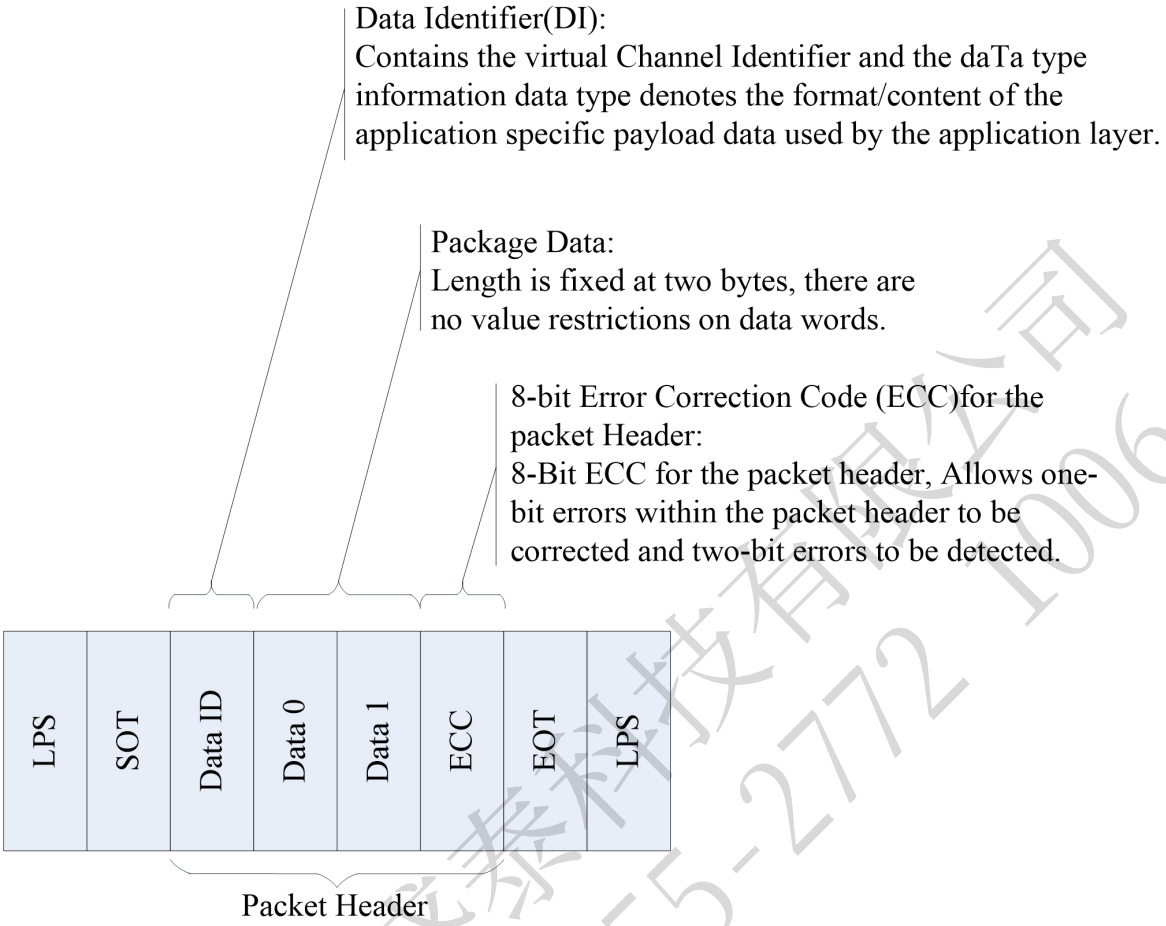


Figure: Short packet structure

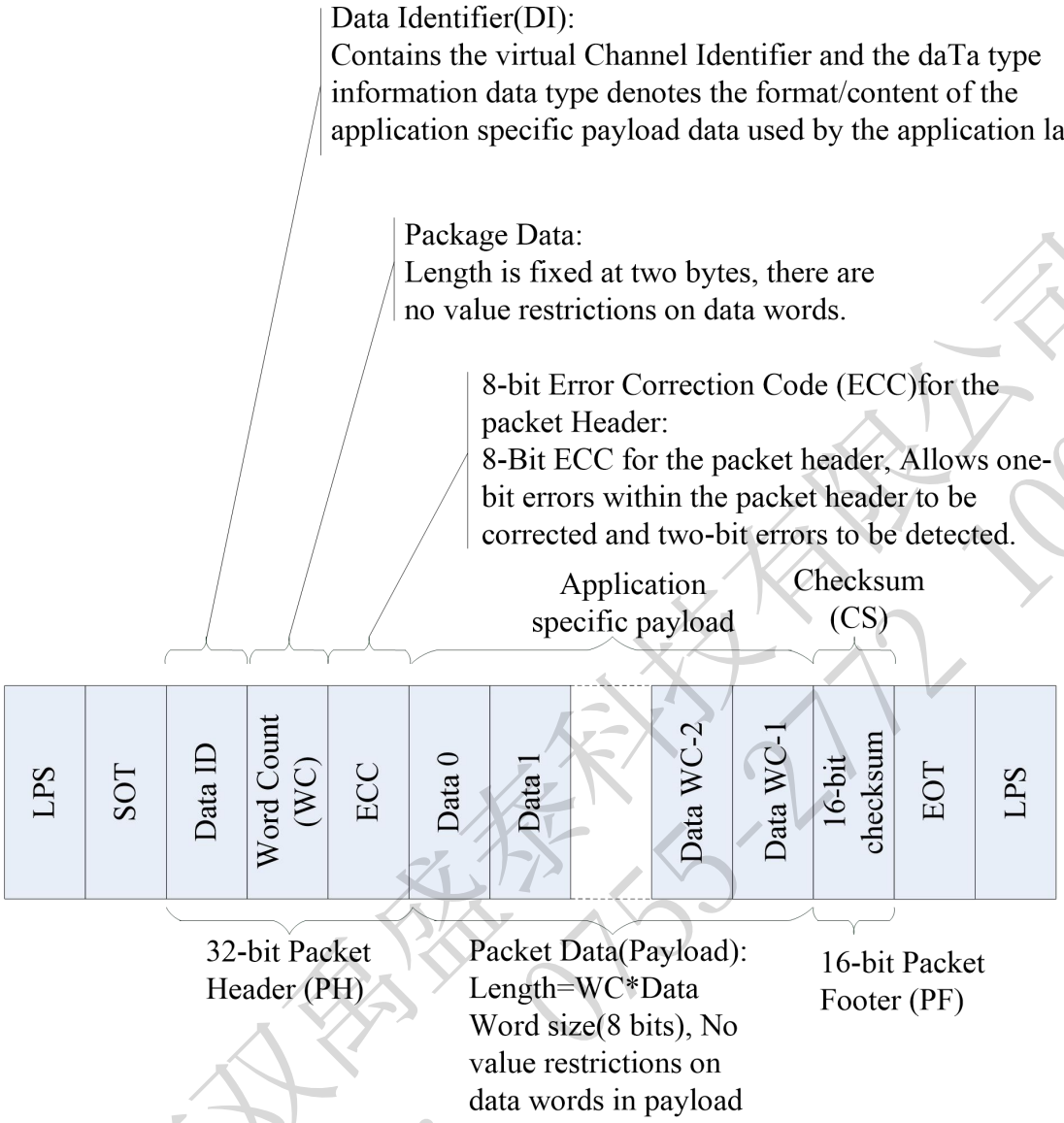


Figure:. Long packet structure

Note: Short Packet (SPa) Structure" and Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

Bit Order of the Byte on Packets

A byte is the smallest transmission unit of a packet. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure below shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

DI	WC(Least Significant Byte)	ECC	Data	CRC(LS Byte)	CRC(MS Byte)

39hex								01hex								15hex								01hex								0Ehex								1Ehex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

WC(Least Significant Byte)								WC(Most Significant Byte)							
01hex								00hex							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
LSB							MSB	LSB							MSB

Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different when it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

DI								Data 0								Data 1								ECC							
15hex								3Ahex								07hex								18hex							
1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet head on short packet

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

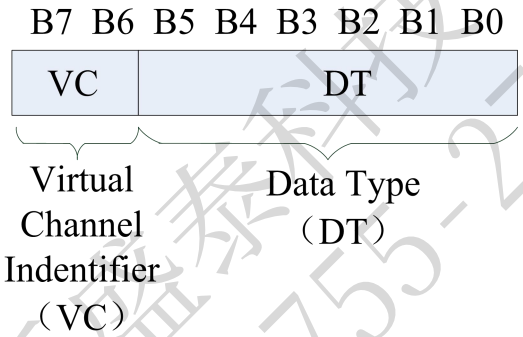


Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are

illustrated for reference purposes below.

AXS15260 only support VC code=00, package with other VC code(01/10/11) will be filter out.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Virtual channel on the packet head

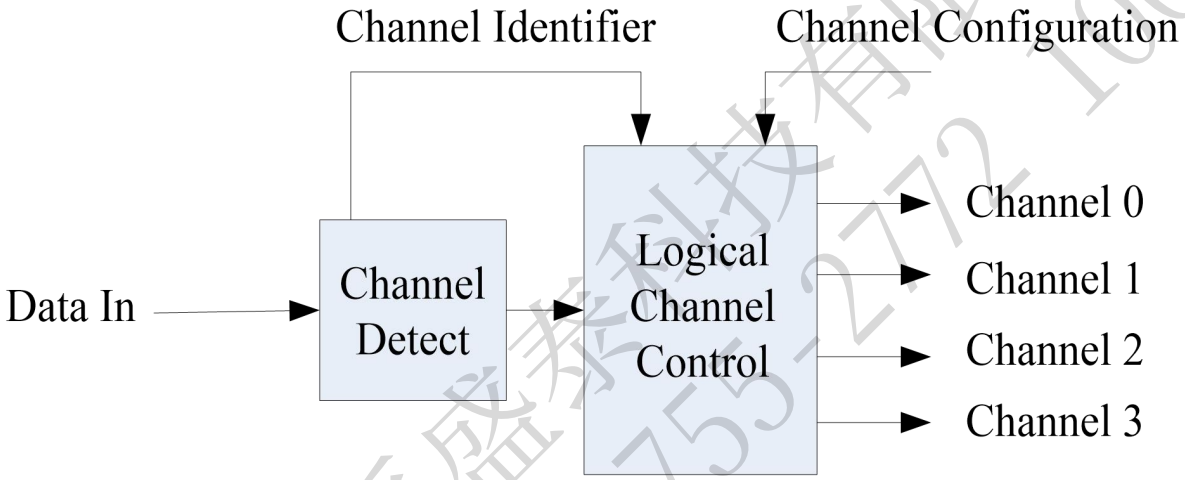


Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

From the MCU to the Display module		
Data Type(HEX)	Data Type(Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT)packet
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
3Eh	11 1110	Packet Pixel Streem, 24-bit RGB, 8-8-8 Format
0Eh	001110	Packed Pixel Stream,16-bit RGB,5-6-5 Format
1Eh	011110	Packed Pixel Stream,18-bit RGB,6-6-6 Format
2Eh	101110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format

Table: Data type from the MCU to the display module

From the Display module to the MCU		
Data Type(HEX)	Data Type(Binary)	Description
1Ch	01 1100	DCS Long Read Response
21h	10 0001	DCS Short Read Response, 1 Byte returned
22h	10 0010	DCS Short Read Response, 2 Byte returned
1Ah	011010	Genaric Long READ Response
11h	01 0001	Generic Short Read Response, 1 Byte returned
12h	01 0010	Generic Short Read Response, 2 Byte returned

Table: Data type from the display module to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables above. Host send "Generic Read" data type, AXS15260 will return Generic Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to 00h, if the information length is 1 byte. Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

DI								Data 0								Data 1								ECC							
15hex								35hex								01hex								1Ehex							
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

DI								Data 0								Data 1								ECC							
05hex								10hex								00hex								2Chex							
1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet data on the short packet, 1 bytes information

Word count on the long packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI)has indicated that Long Packet (LPa) is wanted to send. Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.

DI								Data 0								Data 1								ECC							
05hex								10hex								00hex								2Chex							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	P0	P1	P2	P3	P4	P5	P6	P7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: D[23:0] and P[7:0] on the short packet

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	P0	P1	P2	P3	P4	P5	P6	P7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

ecc_parity = {P7,P6,P5,P4,P3,P2,P1,P0};

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

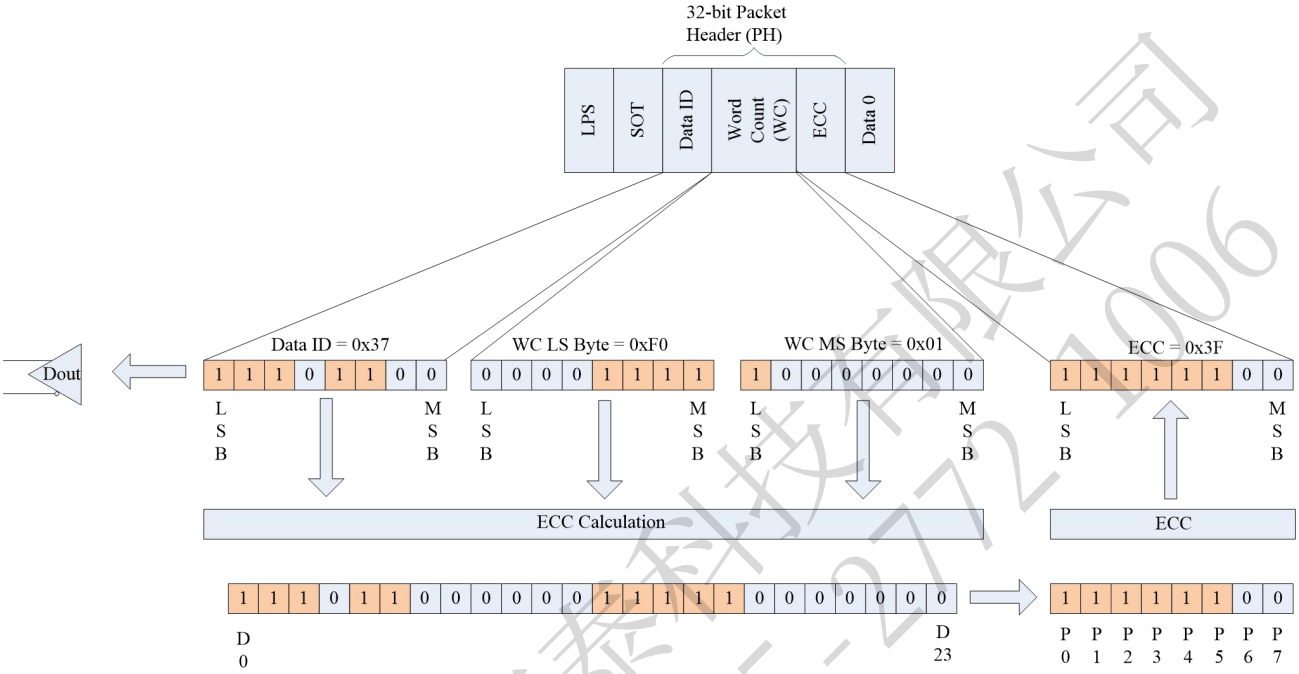


Figure: 24-bit ECC generation on TX side (Example)

Packet footer on the long packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

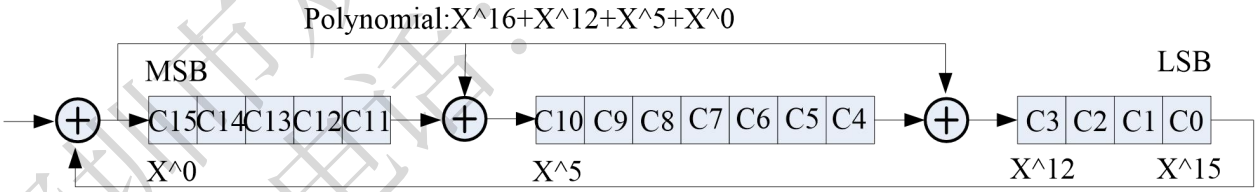


Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC). The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.3.4.2 Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

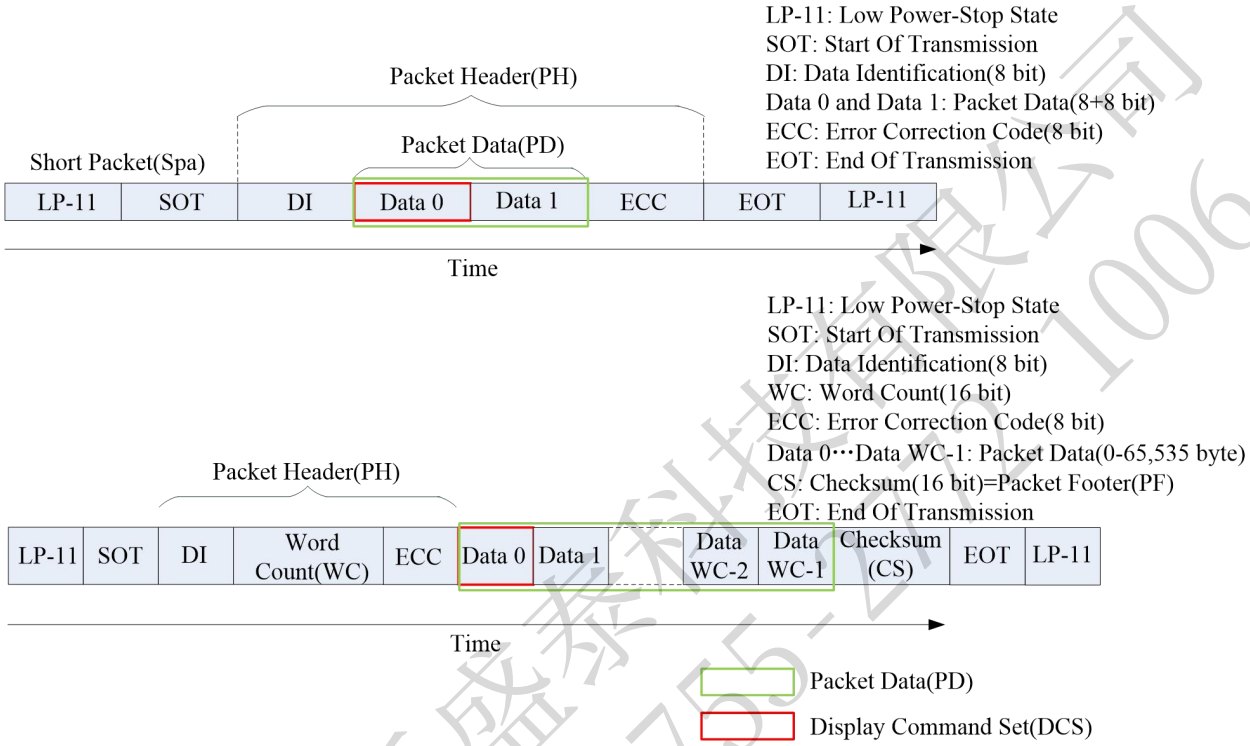


Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

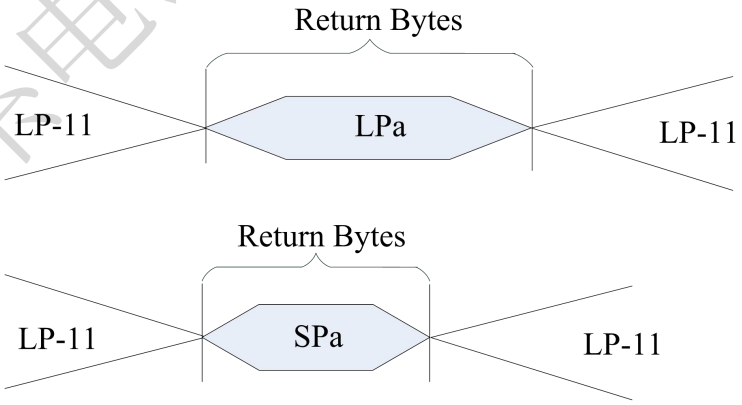


Figure: Return bytes on single packet

5.3.5 Customer-defined generic read data type format

The short packet of Data Type 14h (Generic READ, 1 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 14h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

Packet Structure(processor → peripheral)

		P 0	P 1		
	Data Type 24h	Manufacturer Command	Start Parameter N	ECC	

Low Power Data Transfer(peripheral → processor)

					Data 0	Data 1		Data WC-1		
	Data Type 1Ah	WC 0	WC 1	WC 2	1th Parameter	2th Parameter		Nth Parameter	CRC 0	CRC 1

Figure: Generic read data type format

5.3.6 MIPI video parameter

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

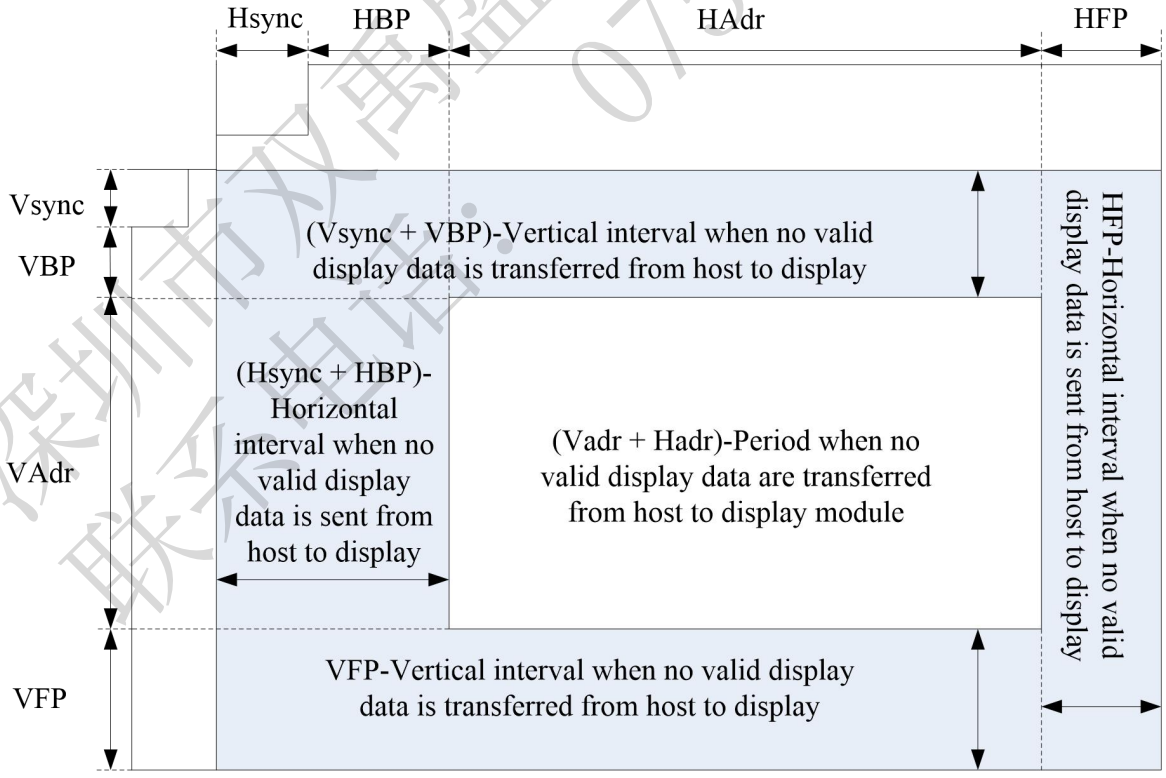


Figure 6.2.6.1 define timing parameter for MIPI video operation.

(Resolution for 320 horizontal x 480 vertical display with Frame-Rate of 60 Hz)

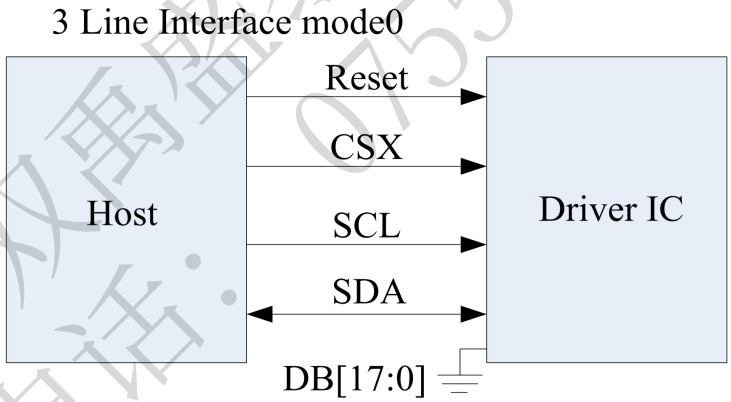
Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	Hsync	2	2	-	PCLK
Horizontal Back Porch	HBP	2	60	-	PCLK
Horizontal Front Porch	HFP	2	60	-	PCLK
Hsync+ HBP+ HFP	-	6	122	-	PCLK
Horizontal Address (Display area)	HAdr	-	320	-	PCLK

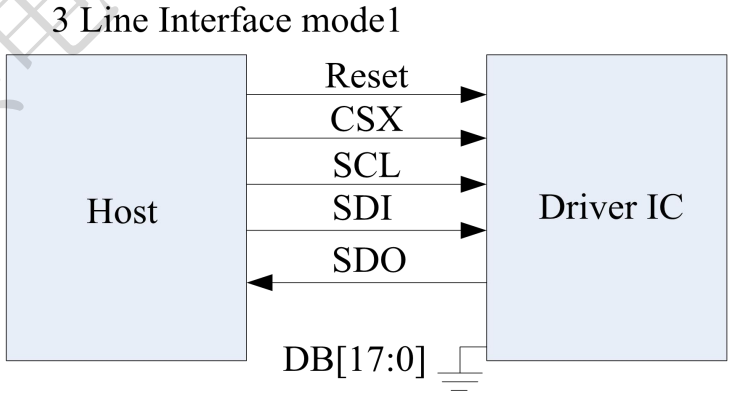
5.4 Serial Interface (SPI)

5.4.1 3-Line Interface

Connect Pin:DIN_SDA(SDI),DIN_SDA_DUAL(SDO),SCL,CSX,RSTN.

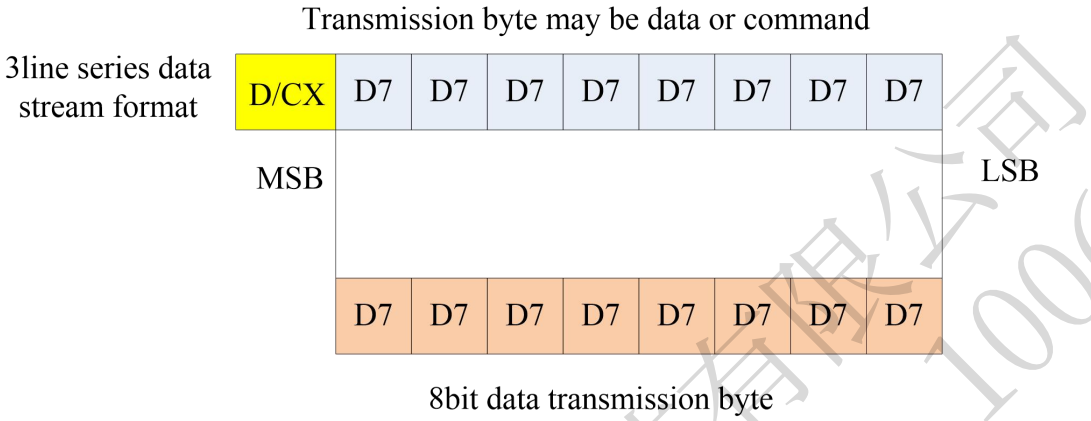
The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “1100” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input /output pin (SDA or SDI/SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[23:0] pins, which are not used, must be tied to GND.



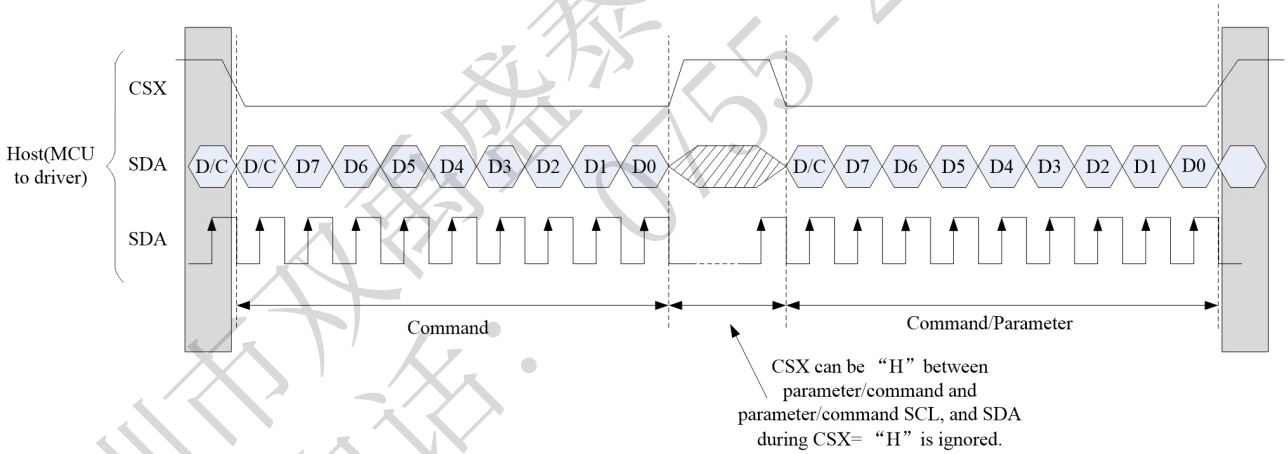


5.4.1.1 Write Sequence.

In the write mode of 3-line serial interface contains a D/CX (data/command) select bit and a transmission byte. If the D/CX bit is “0”, the transmission byte is interpreted as a command byte. If the D/CX bit is “1”, the transmission byte is display data, or stored in the command register as parameter data.



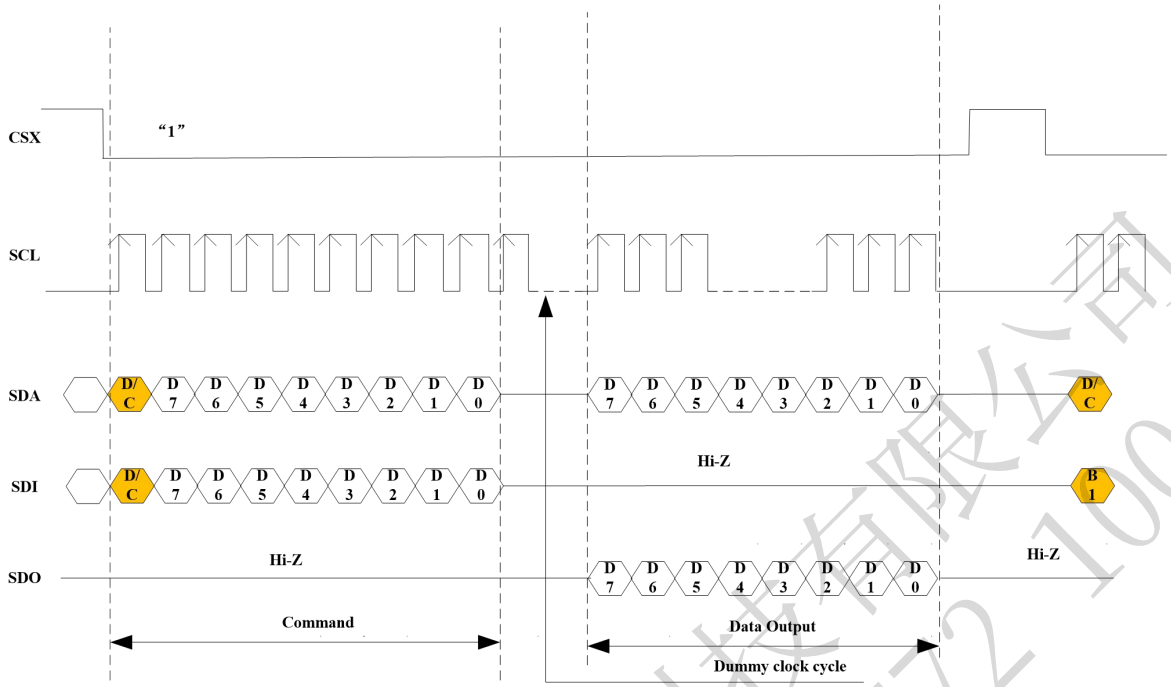
The instruction of AXS15260 can be sent in any order, and the MSB is transmitted first. The 3-line serial interface is initialized when the CSX keeps high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



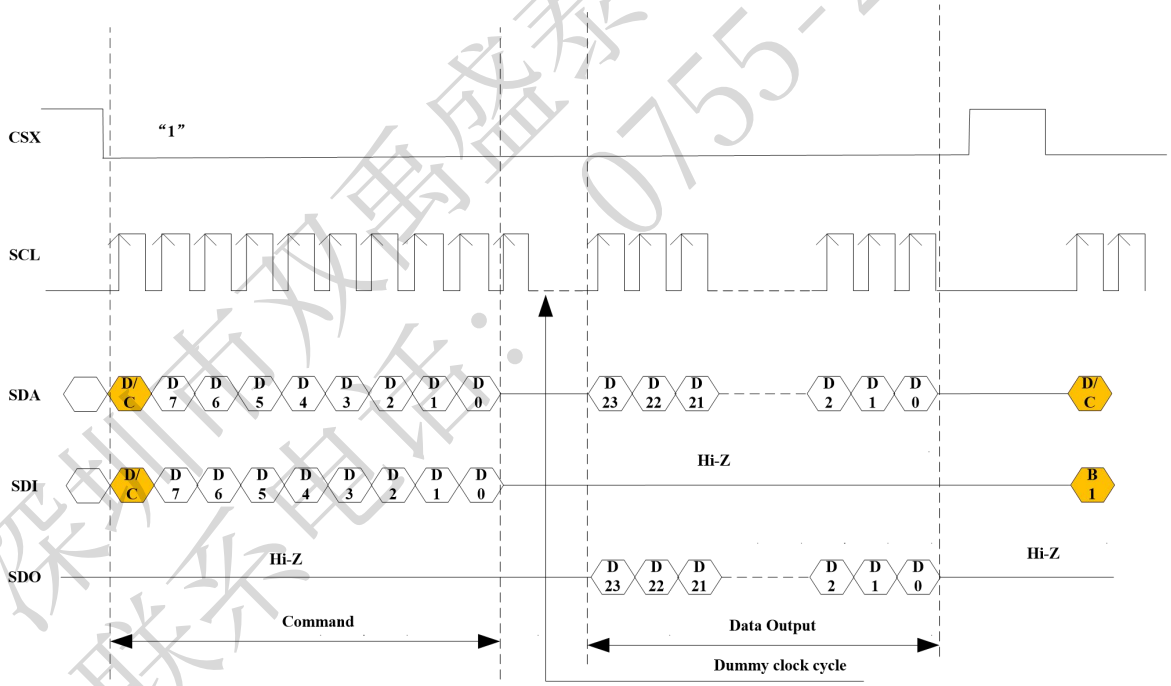
5.4.1.2 Read Sequence

In the read mode of the interface, the host reads the register value from the AXS15260. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The AXS15260 samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

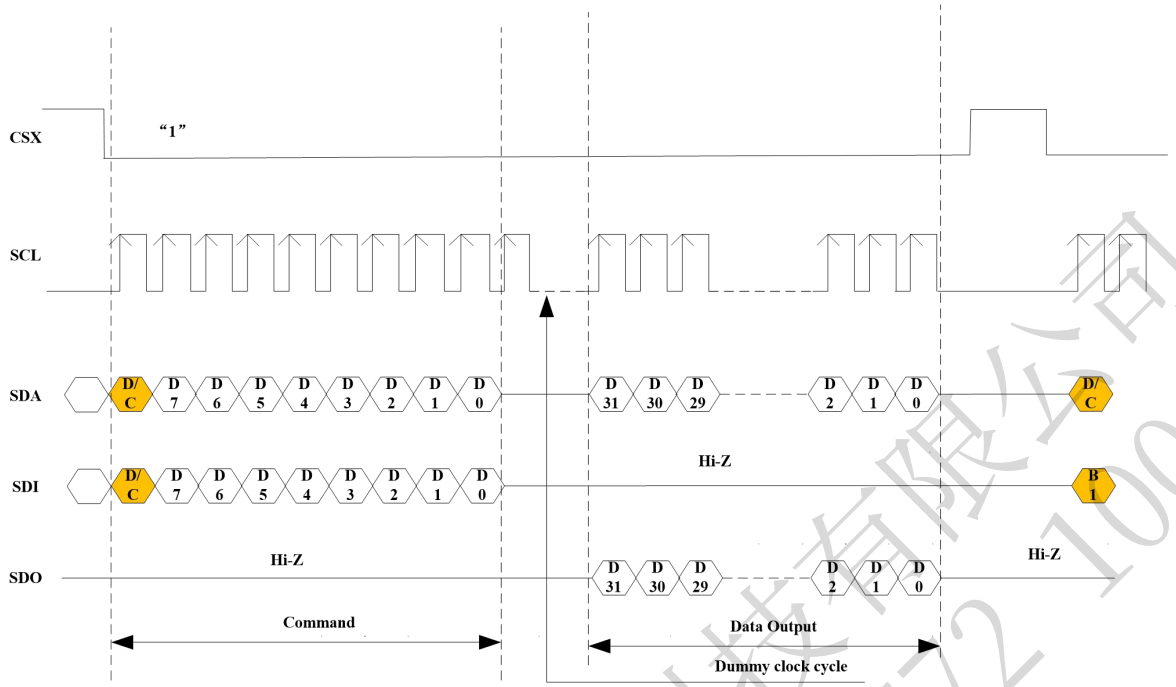
5.4.1.2.1 3-line serial protocol (8-bit read, cr_spi_rd_en=1)



5.4.1.2.2 3-line serial protocol (24-bit read, cr_spi_rd_en=1)



5.4.1.2.3 3-line serial protocol (32-bit read, cr_spi_rd_en=1)

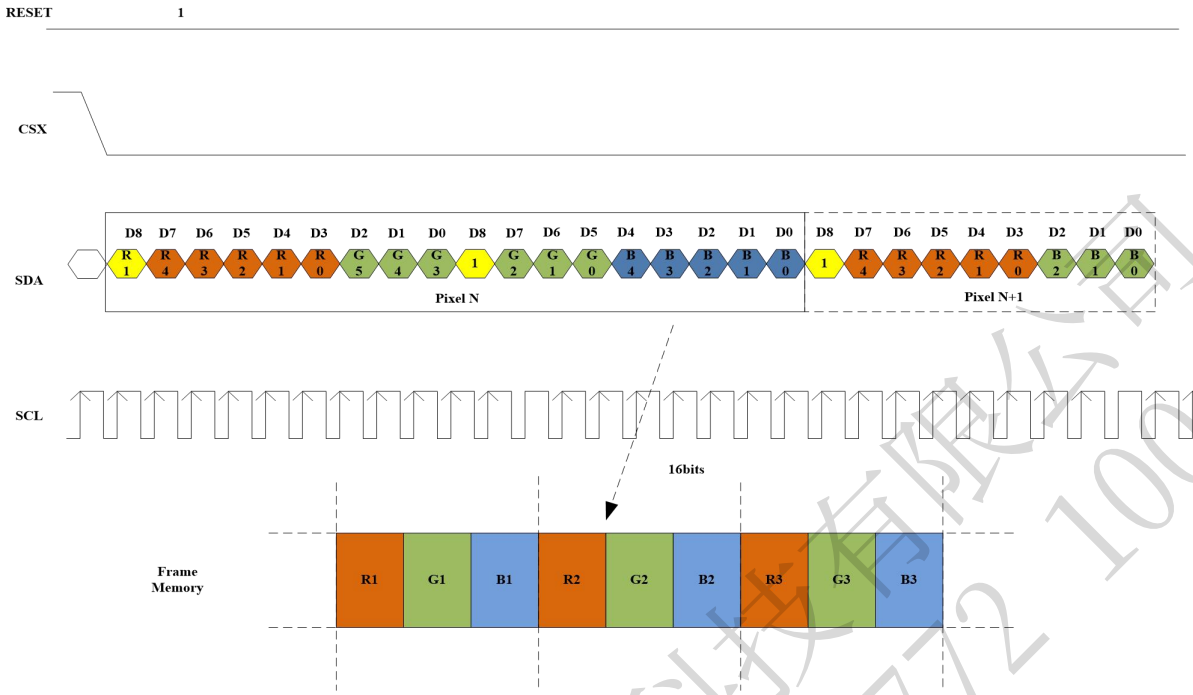


5.4.1.3 3-SPI Color format

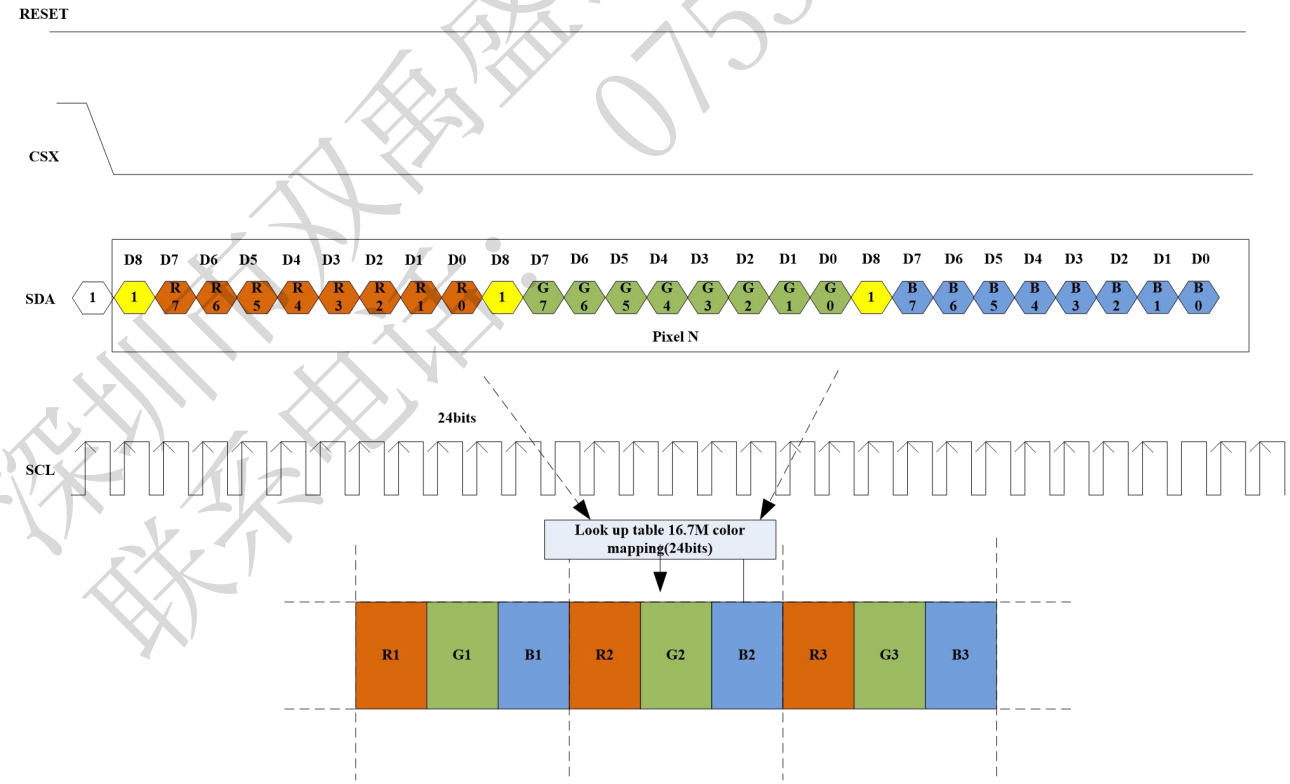
Different display data formats are available for three colors depth supported by the LCM listed below.：

65k colors, RGB 5-6-5-bit input
16.7M colors, RGB 8-8-8-bit input

5.4.1.3.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



5.4.1.3.2 Write data for 24-bit/pixel (RGB 8-8-8-bit input), 16.7M-Colors



5.4.1.4 2-data-line mode(3-Line)

Connect Pin:DIN_SDA,DIN_SDA_DUAL,SCL,CSX,RSTN.

The 2-data-line mode Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “0110” level.

This mode is active when 2data_en set to “1” in 3-wire. Only frame pixel data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

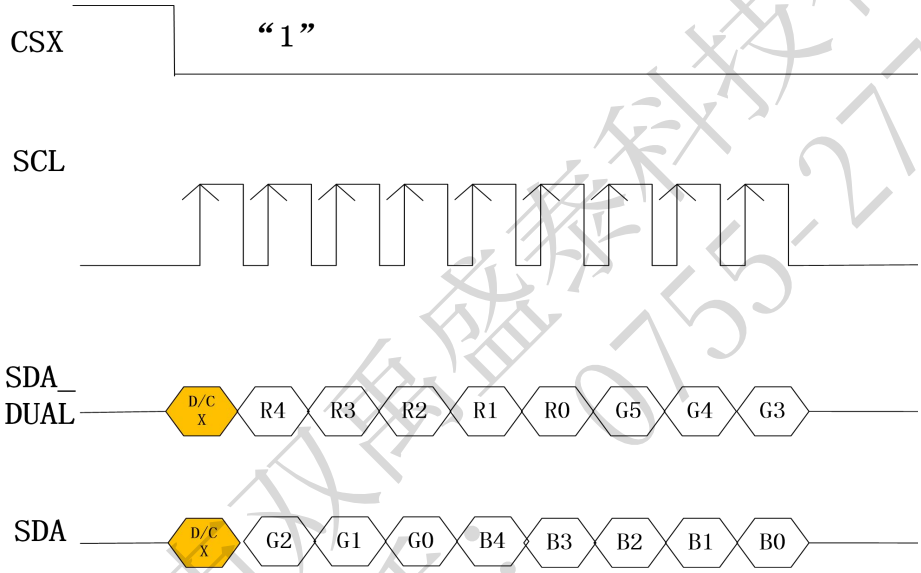
The chip-select CSX (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and SDA_DUAL are serial data lines.

The AXS15260 reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. It must be set to "1", D23 to D0 bits are display RAM data,When the cr spi diomode parameter is set differently, data is exchanged between the SDA and SDA DUAL(The following figure shows the cr_spi_diomode=1).

5.4.1.4.1.1 3-line write data

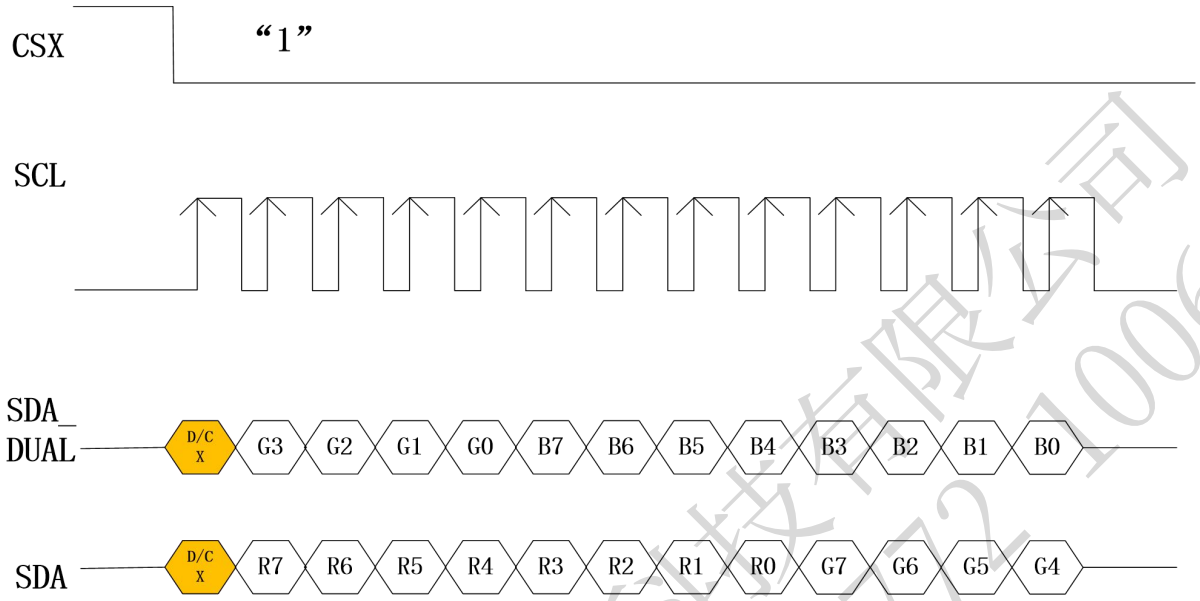
5.4.1.4.1.1.1 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors

Cr_spi_dual_opt=11,cr_spi_format=1.

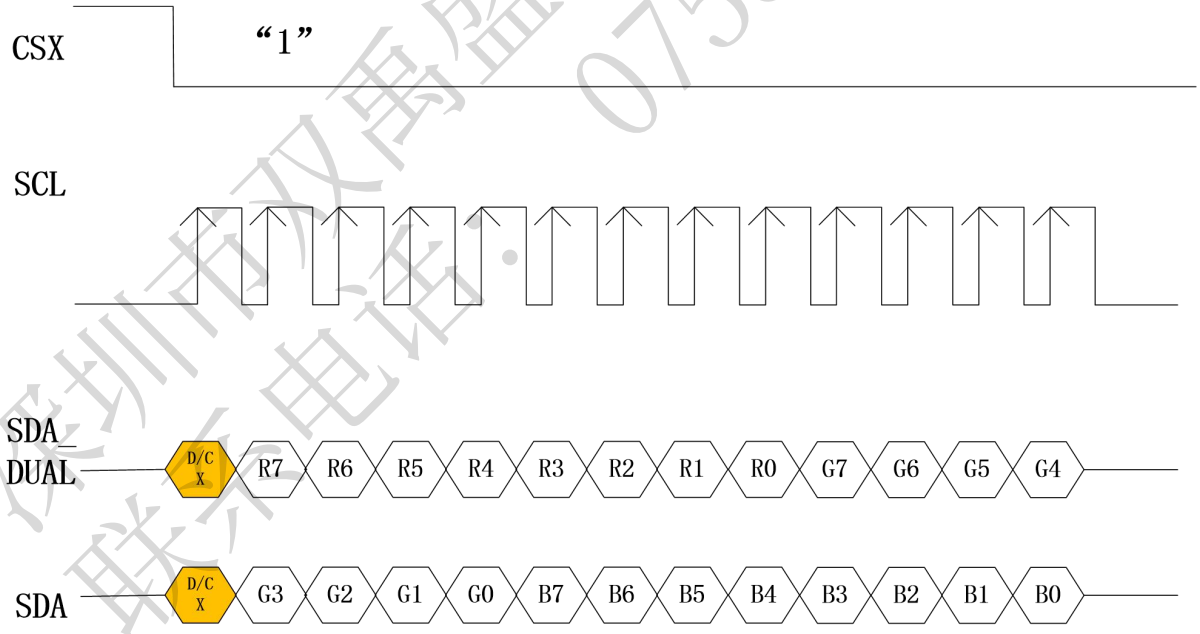


5.4.1.4.1.1.2 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors

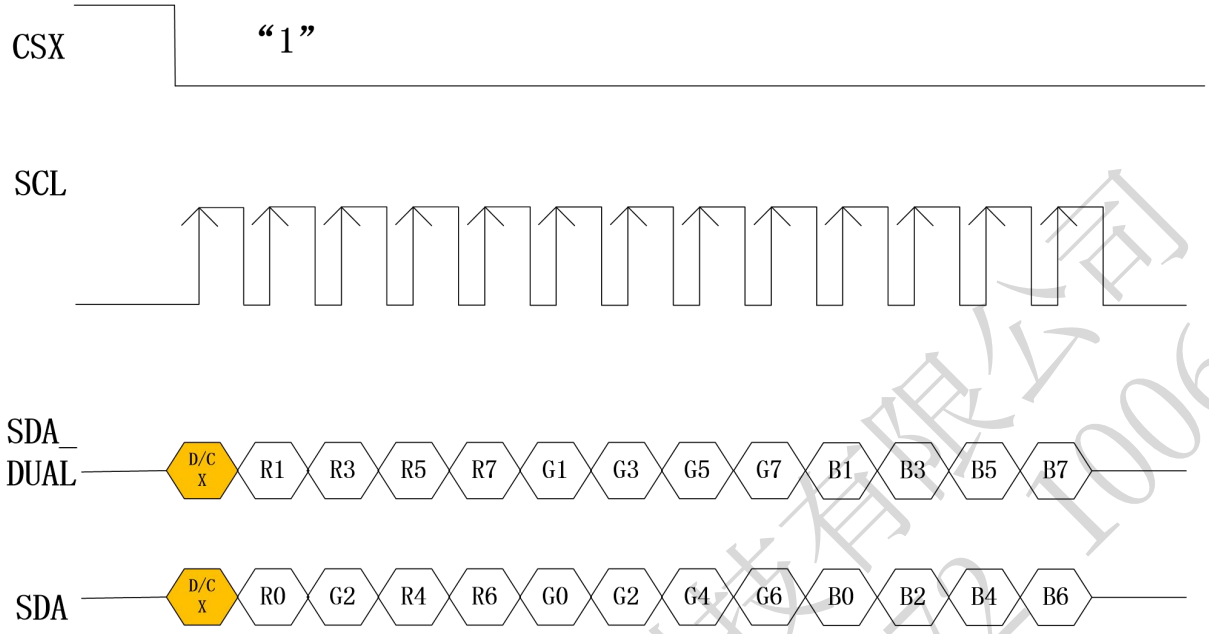
5.4.1.4.1.1.2.1 Mode1:Cr_spi_dual_opt=00



5.4.1.4.1.1.2.2 Mode2:Cr_spi_dual_opt=01



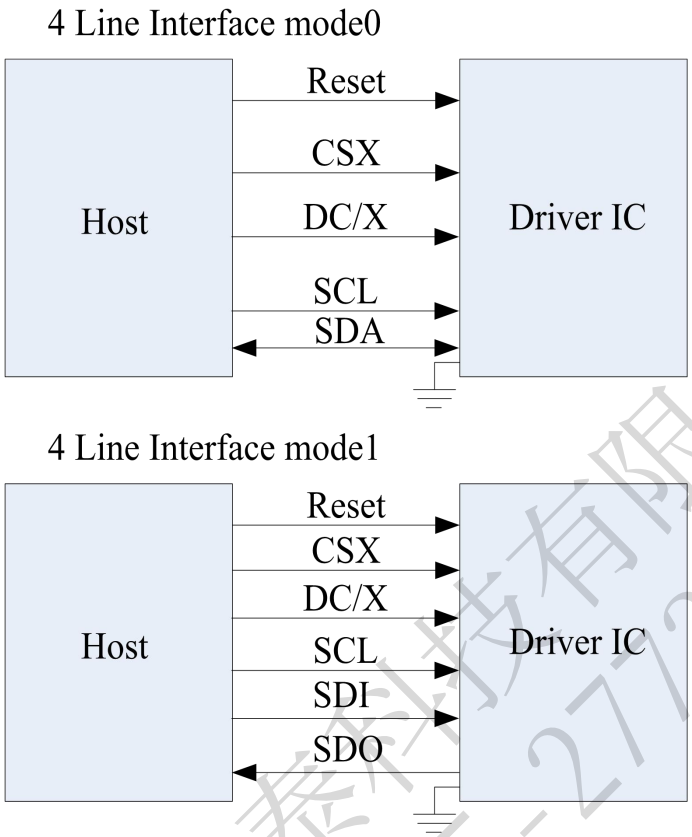
5.4.1.4.1.1.2.3 Mode3:Cr_spi_dual_opt=10



5.4.2 4-Line Interface

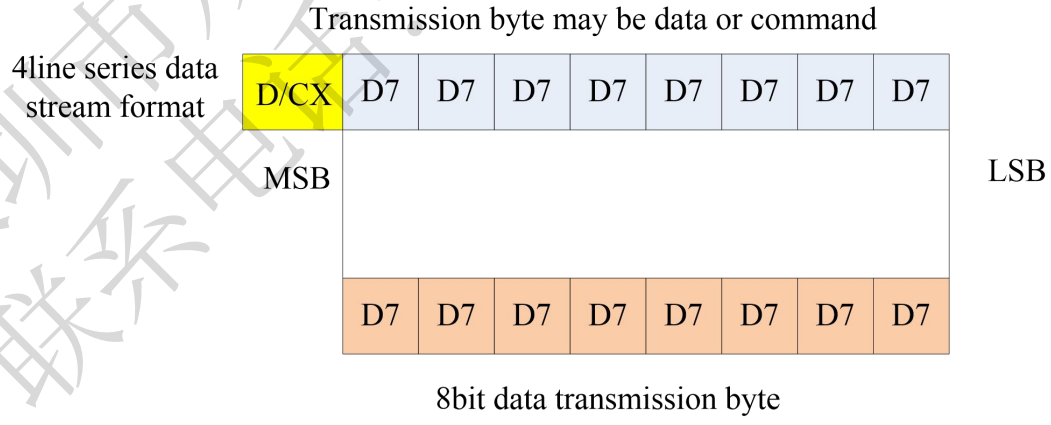
Connect Pin:DIN_SDA(SDI),DIN_SDA_DUAL(SDO),RS(D/CX),SCL,CSX,RSTN

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “1101” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the display data/command selection (D/CX), the serial data input/output pin (SDA or SDI/SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[23:0] pins, which are not used, must be tied to GND

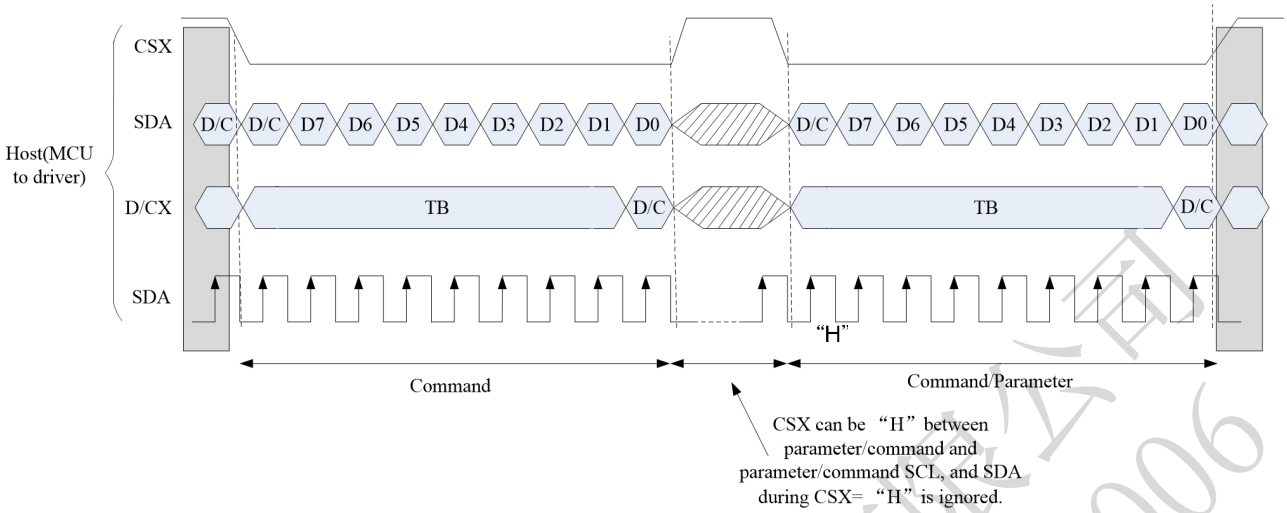


5.4.2.1 Write Sequence

The write mode of the interface means the host writes commands and data to AXS15260. The 4-lines serial data packet contains a data/command and a transmission byte. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.



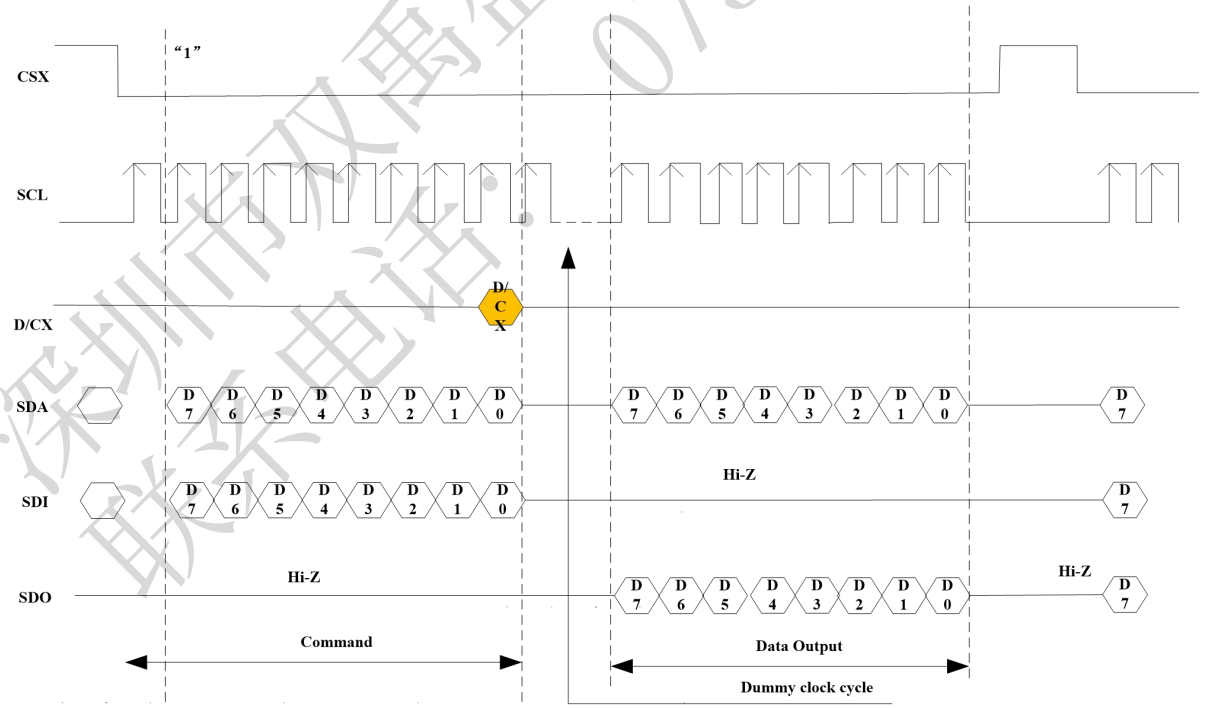
The host drives the CSX pin to low and the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle long. The 4-line serial interface writes sequence described in the Figure as below.



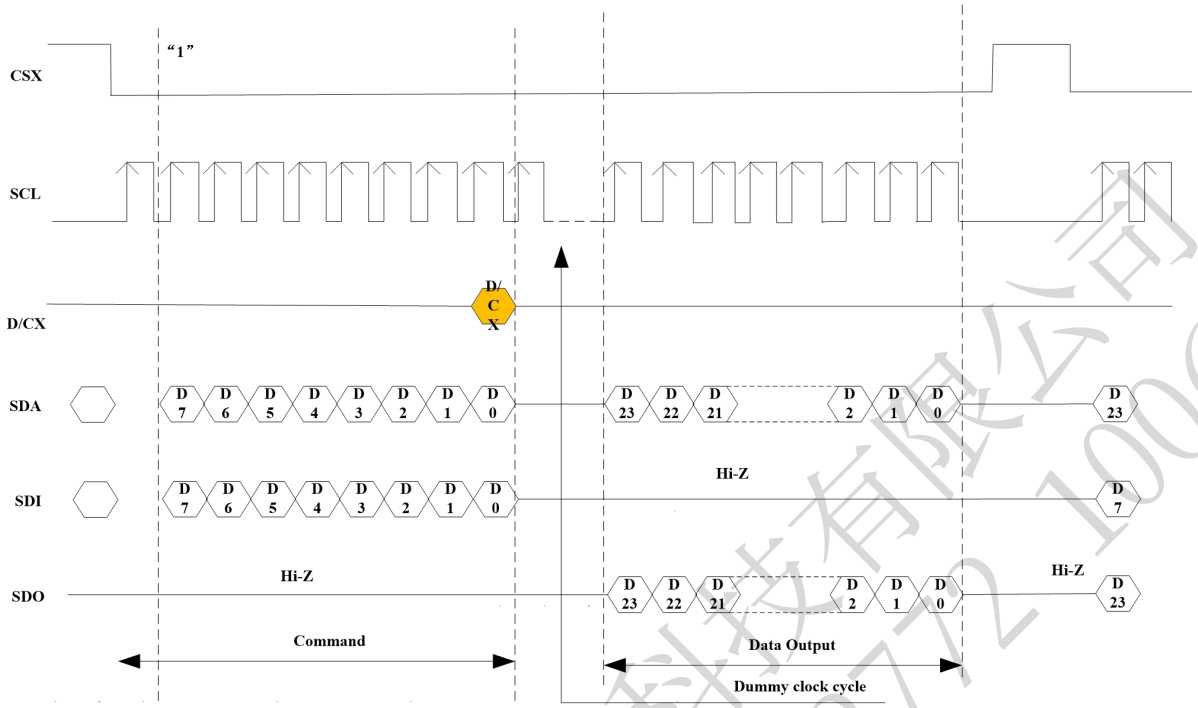
5.4.2.2 Read Sequence

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

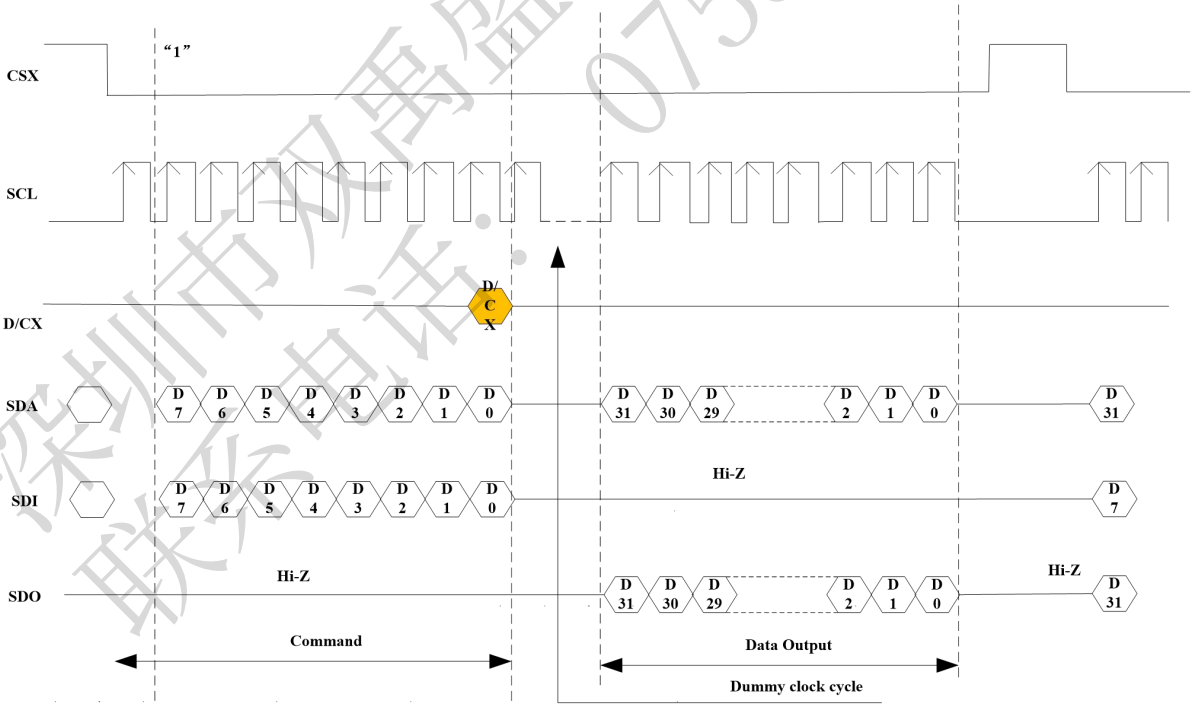
5.4.2.2.1 4-line serial protocol (8-bit read, cr_spi_rd_en=1):



5.4.2.2.2 4-line serial protocol (24-bit read,cr_spi_rd_en=1)



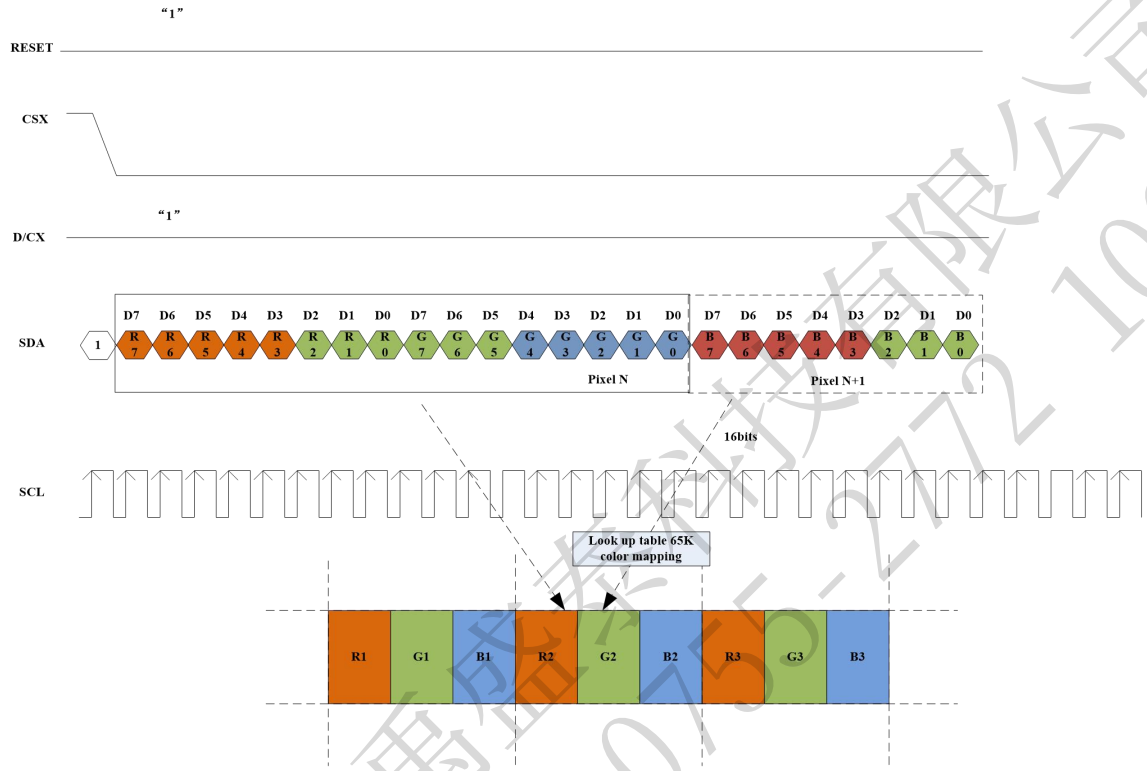
5.4.2.2.3 4-line serial protocol (32-bit read,cr_spi_rd_en=1)



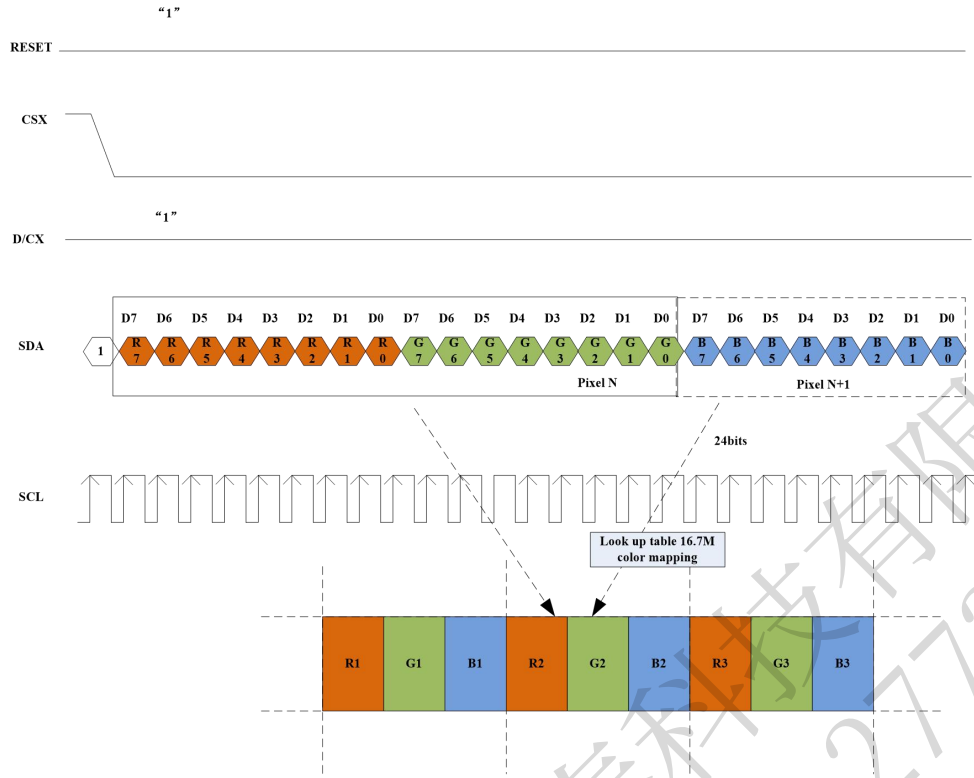
5.4.2.3 4-SPI Color format

Different display data formats are available for three colors depth supported by the LCM listed below. 65k colors, RGB 5-6-5-bit input
16.7M colors, RGB 8-8-8-bit input

5.4.2.3.1 Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors



5.4.2.3.2 Write data for 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors



5.4.2.4 2-data-line mode(4-Line)

Connect Pin:DIN_SDA,DIN_SDA_DUAL,RS(D/CX),SCL,CSX,RSTN.

The 2-data-line mode Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as "1011" level.

This mode is active when 2data_en set to "1" in 4-wire. Only frame pixel data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

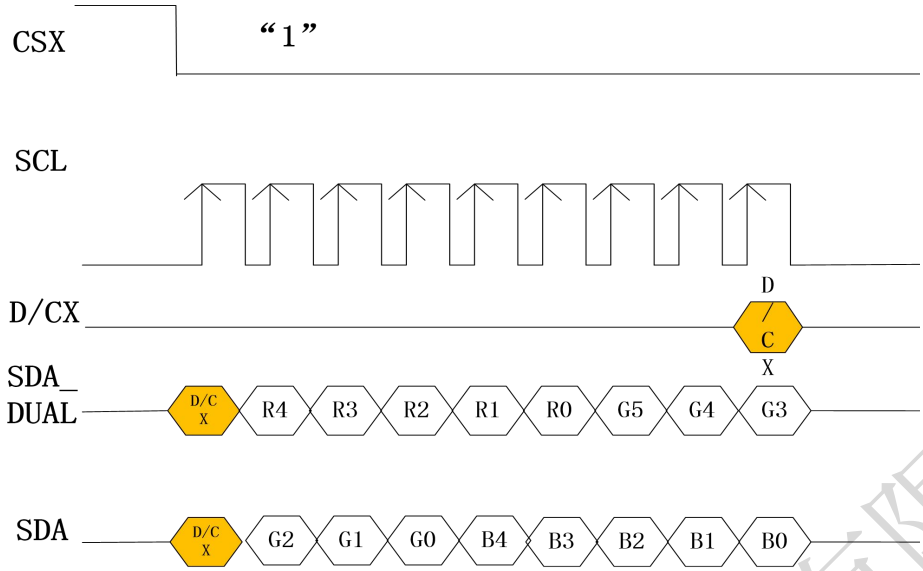
The chip-select CSX (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and SDA_DUAL are serial data lines.

The AXS15260 reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. It must be set to "1", D23 to D0 bits are display RAM data. , When the cr spi diomode parameter is set differently, data is exchanged between the SDA and SDA DUAL(The following figure shows the cr_spi_diomode=1).

5.4.2.4.1.1 4-line write data

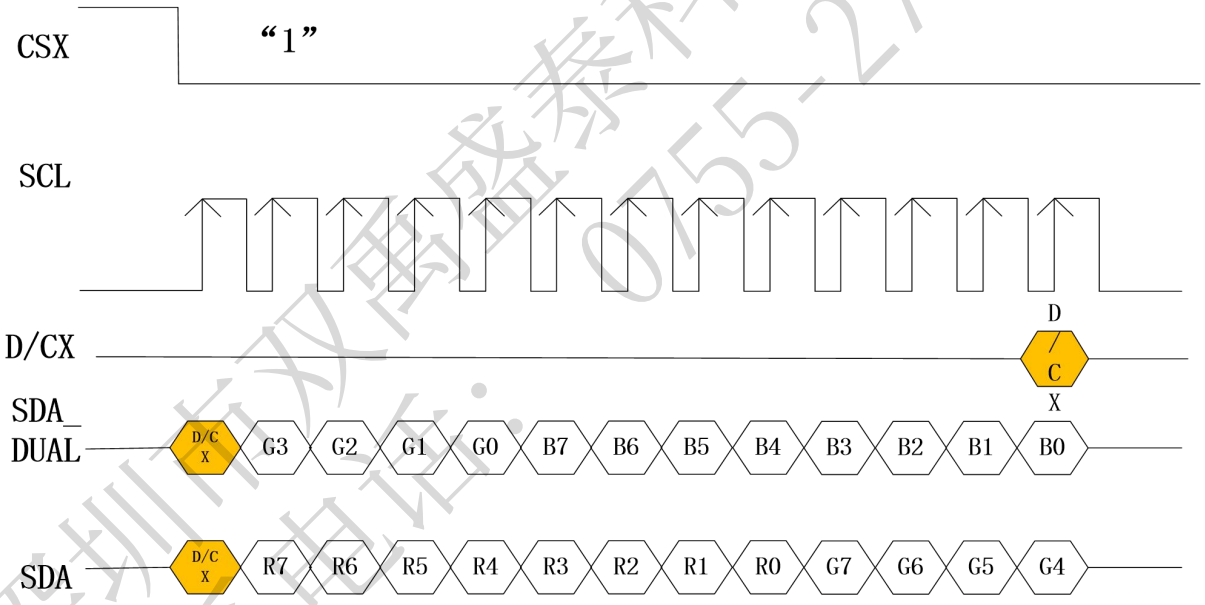
5.4.2.4.1.1.1 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors

Cr_spi_dual_opt=11,cr_spi_format=1.

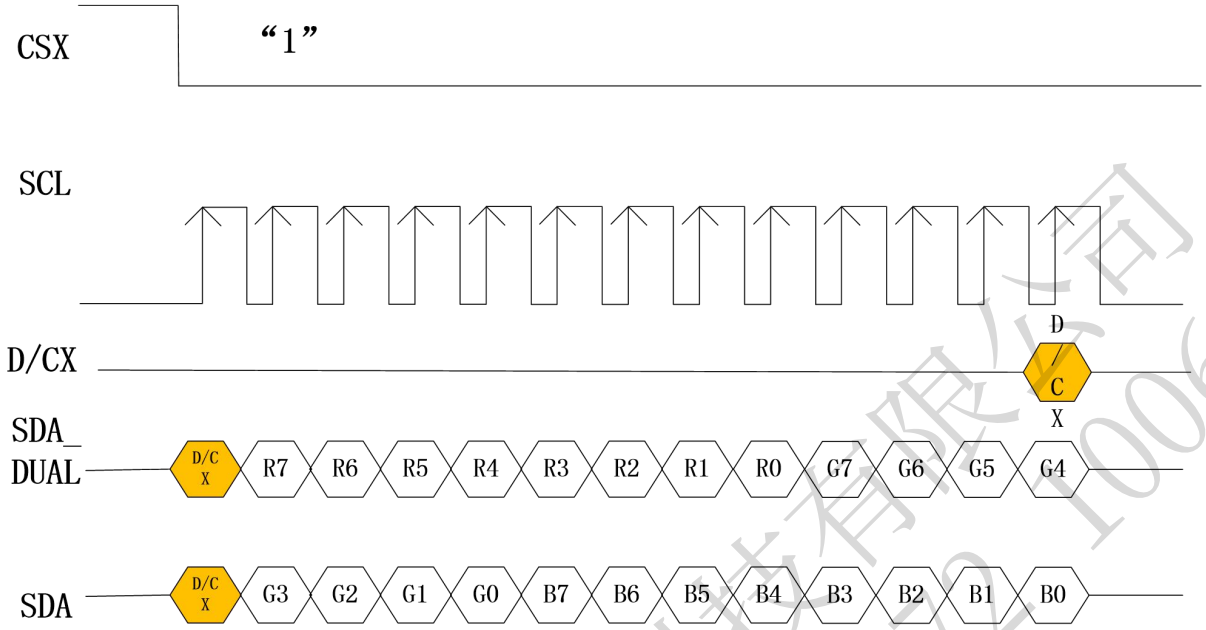


5.4.2.4.1.1.2 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors

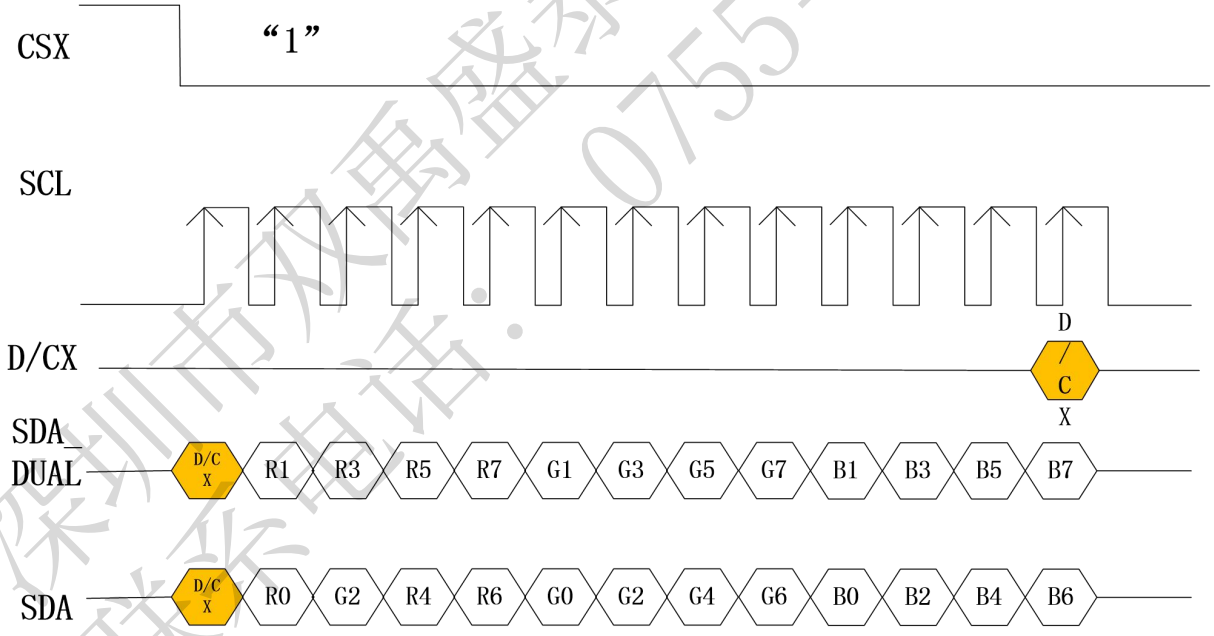
5.4.2.4.1.1.2.1 Mode1:Cr_spi_dual_opt=00



5.4.2.4.1.1.2.2 Mode2:Cr_spi_dual_opt=01



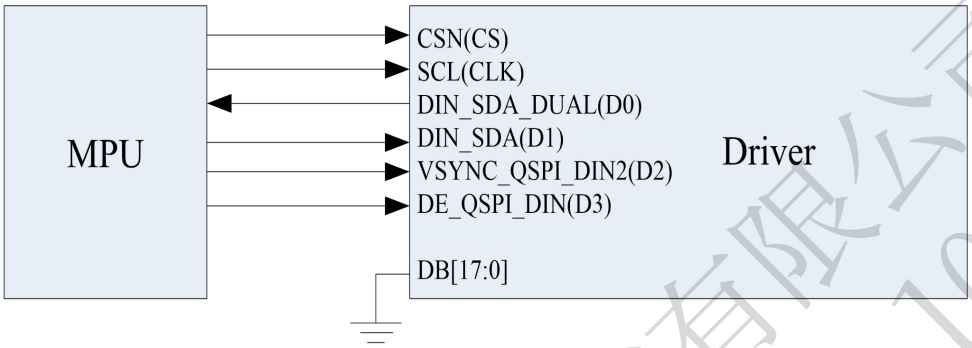
5.4.2.4.1.1.2.3 Mode3:Cr_spi_dual_opt=10



5.5 Quad Serial Peripheral Interface

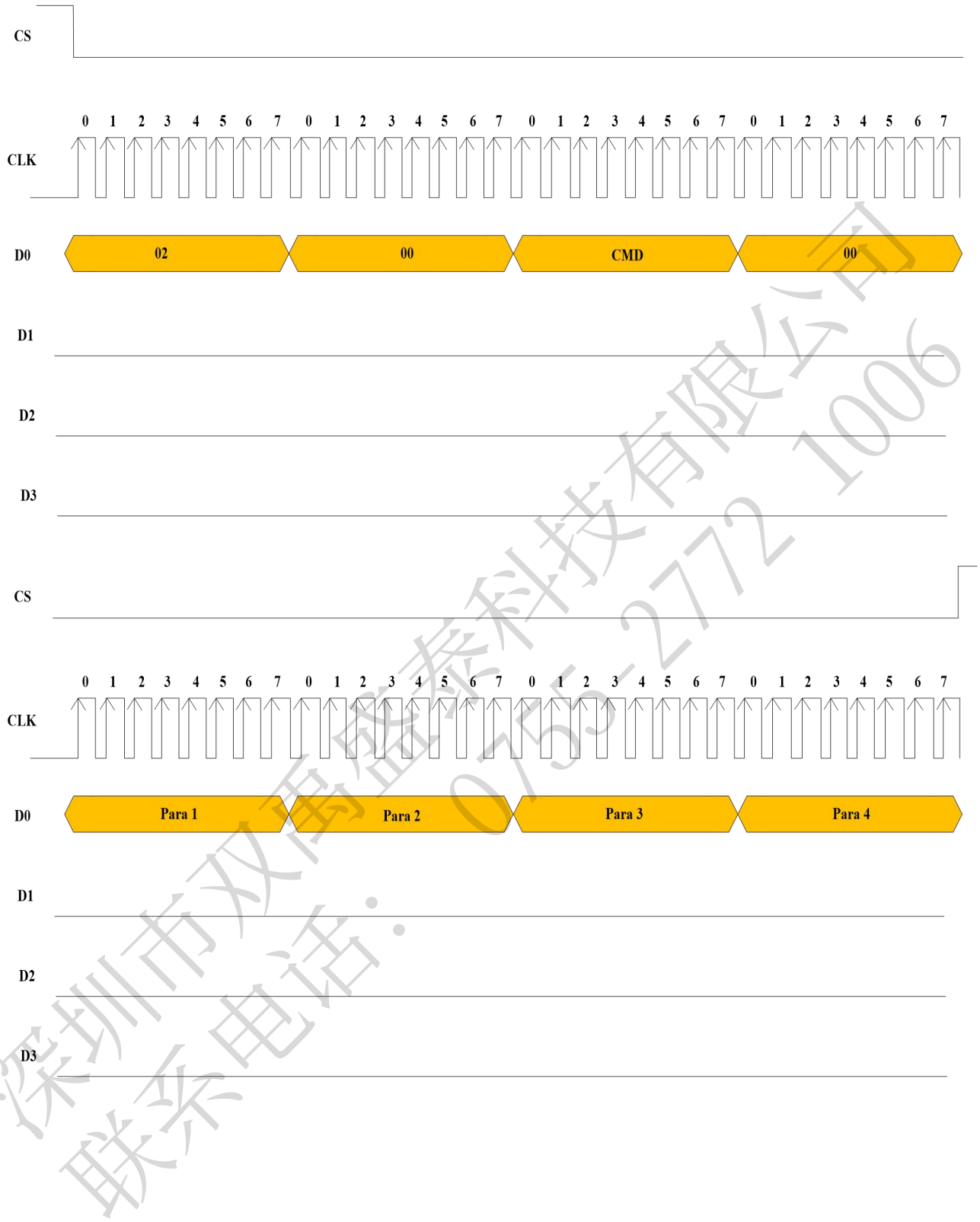
Connect Pin:DE_QSPI_DIN3,VSYNC_QSPI_DIN2,DIN_SDA,DIN_SDA_DUAL,SCL,CSX,RSTN

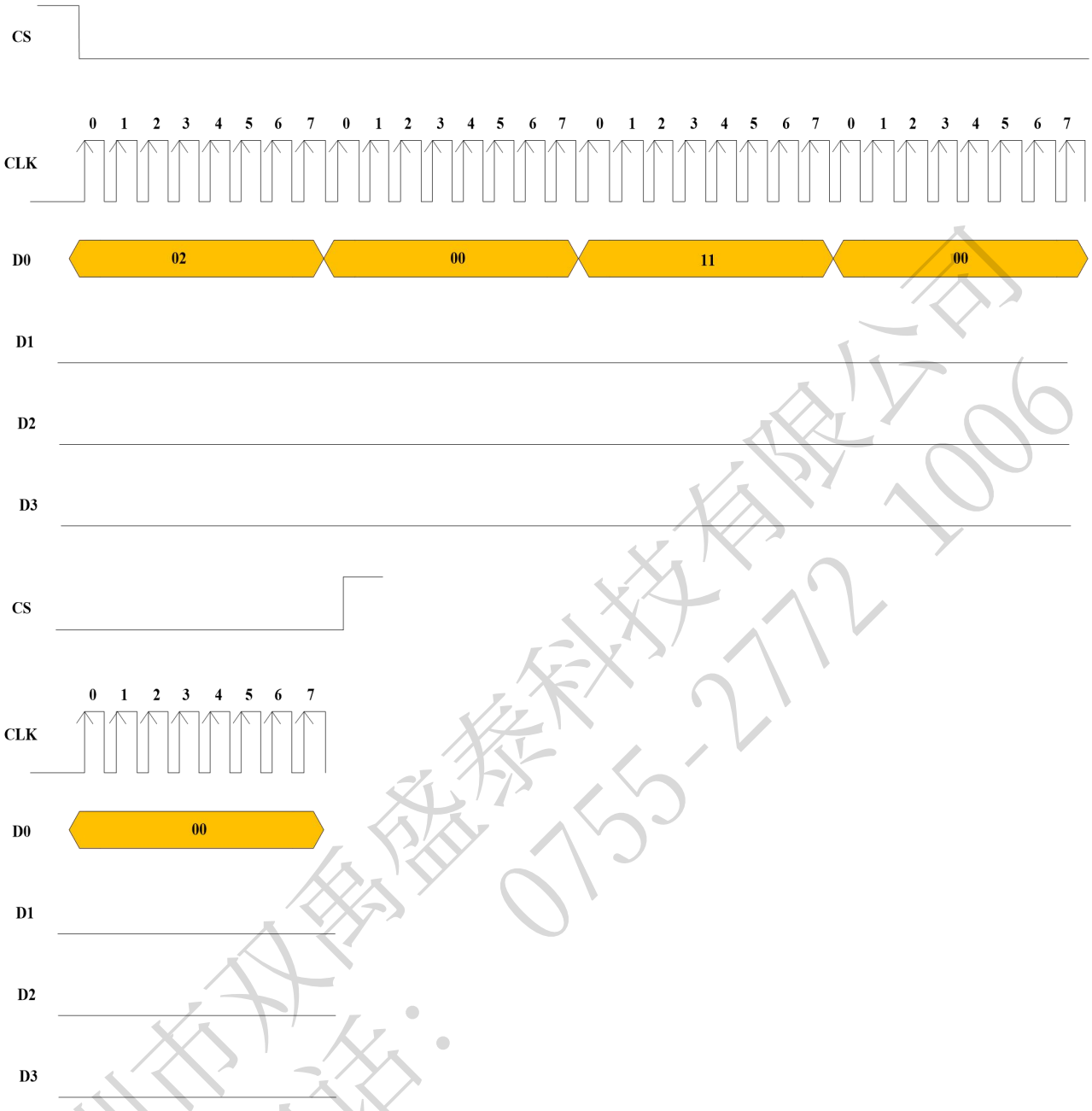
The Quad Serial Peripheral Interface of AXS15260 can be selected by setting hardware pin IM [3:0] to “0101”. The following shown figure is the example of interface with Quad Serial Peripheral Interface.

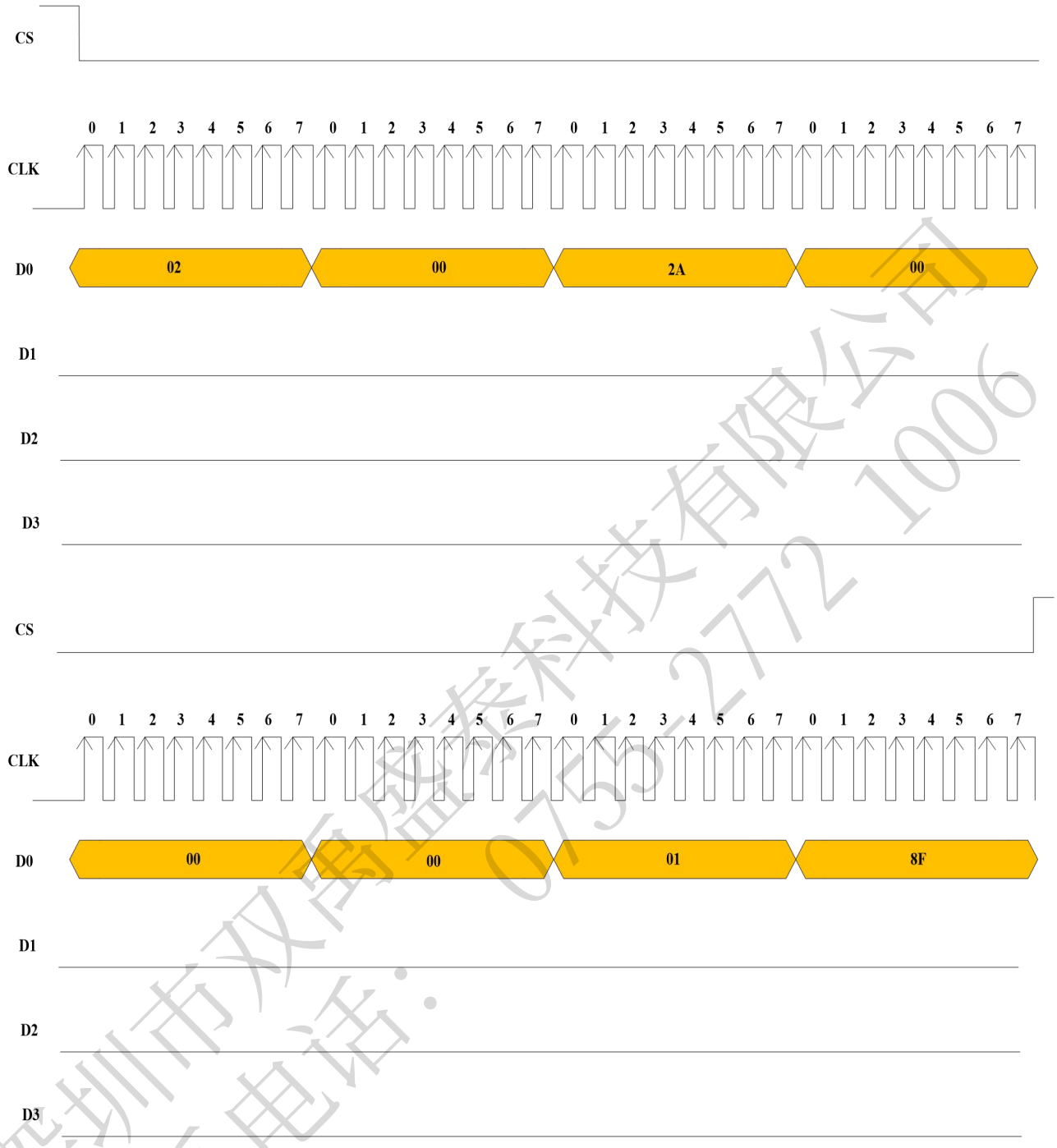


5.5.1 Write Cycle Sequence

The AXS15260 reads the data at the rising edge of SCL signal. The timing of Write Cycle Sequence is shown as below.

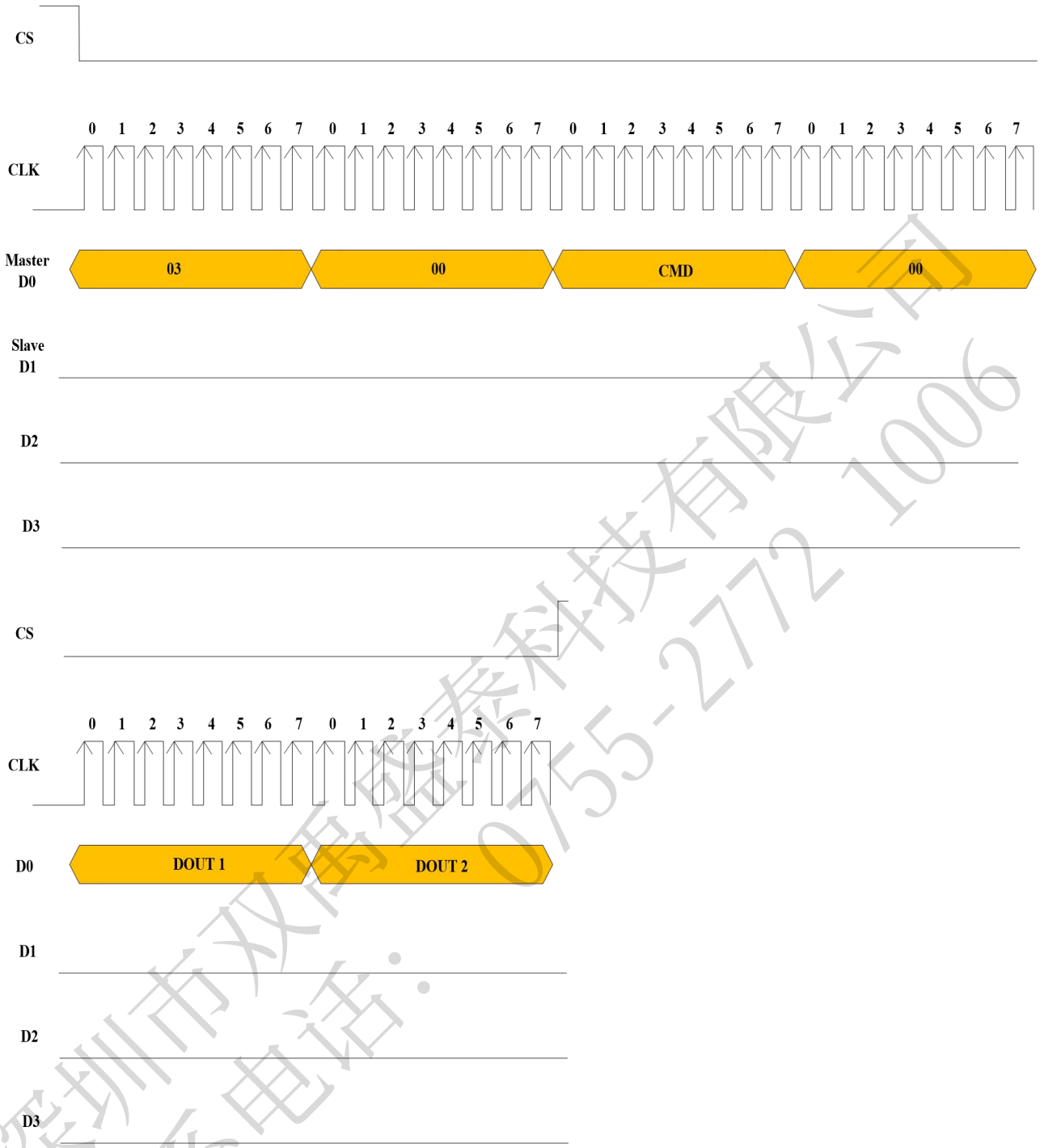






5.5.2 Read Cycle Sequence

The timing of Read Cycle Sequence is shown as below.



5.5.3 QSPI Color Format

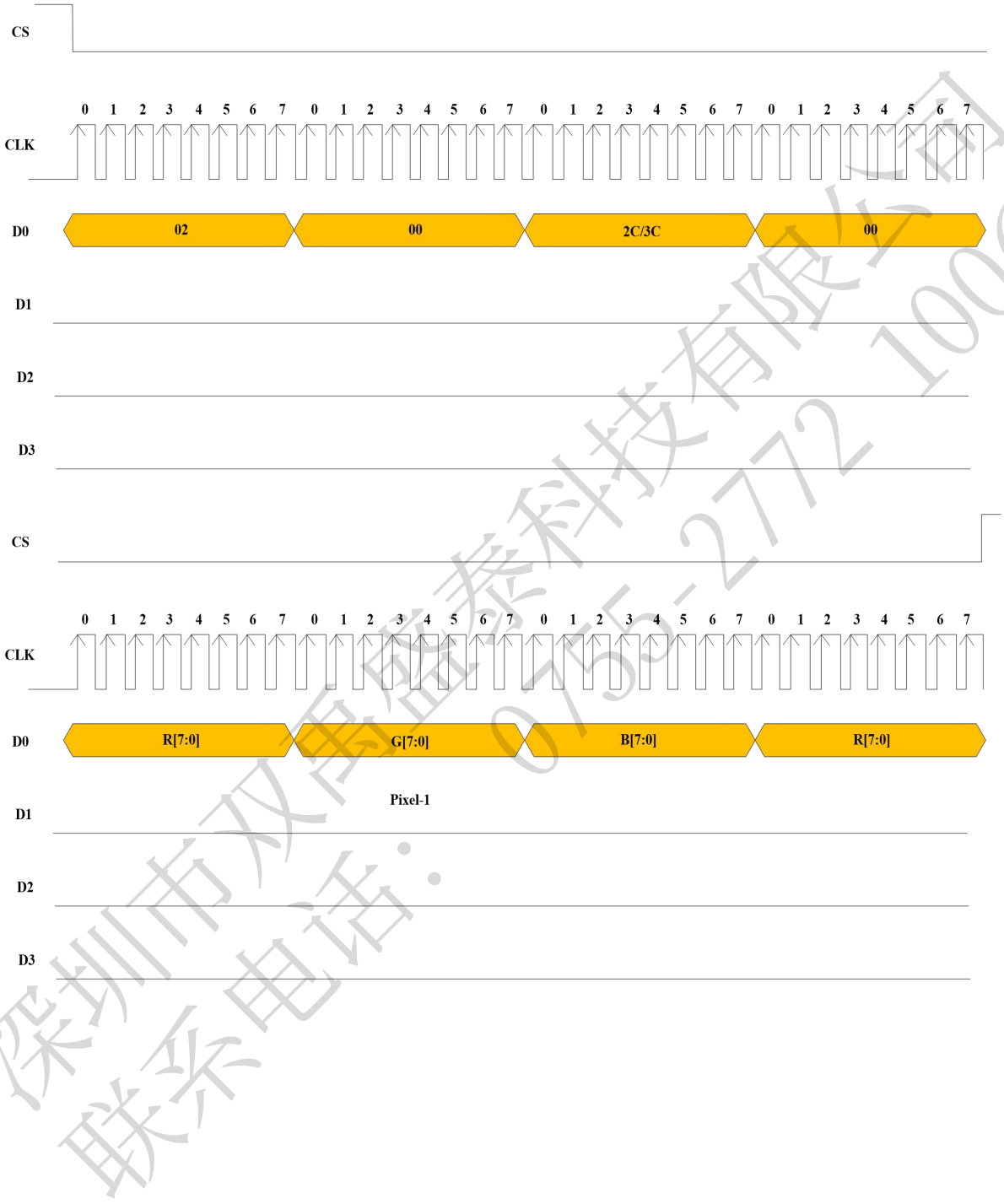
In quad serial Peripheral interface, different display data format is available for five color depths supported by the LCM listed below.

-16.7M colors RGB 8, 8, 8-bits input
-65k colors, RGB 5, 6, 5 -bits input
-256 colors, RGB 3, 3, 2 -bits input
-8 colors，RGB 1, 1, 1-bits input

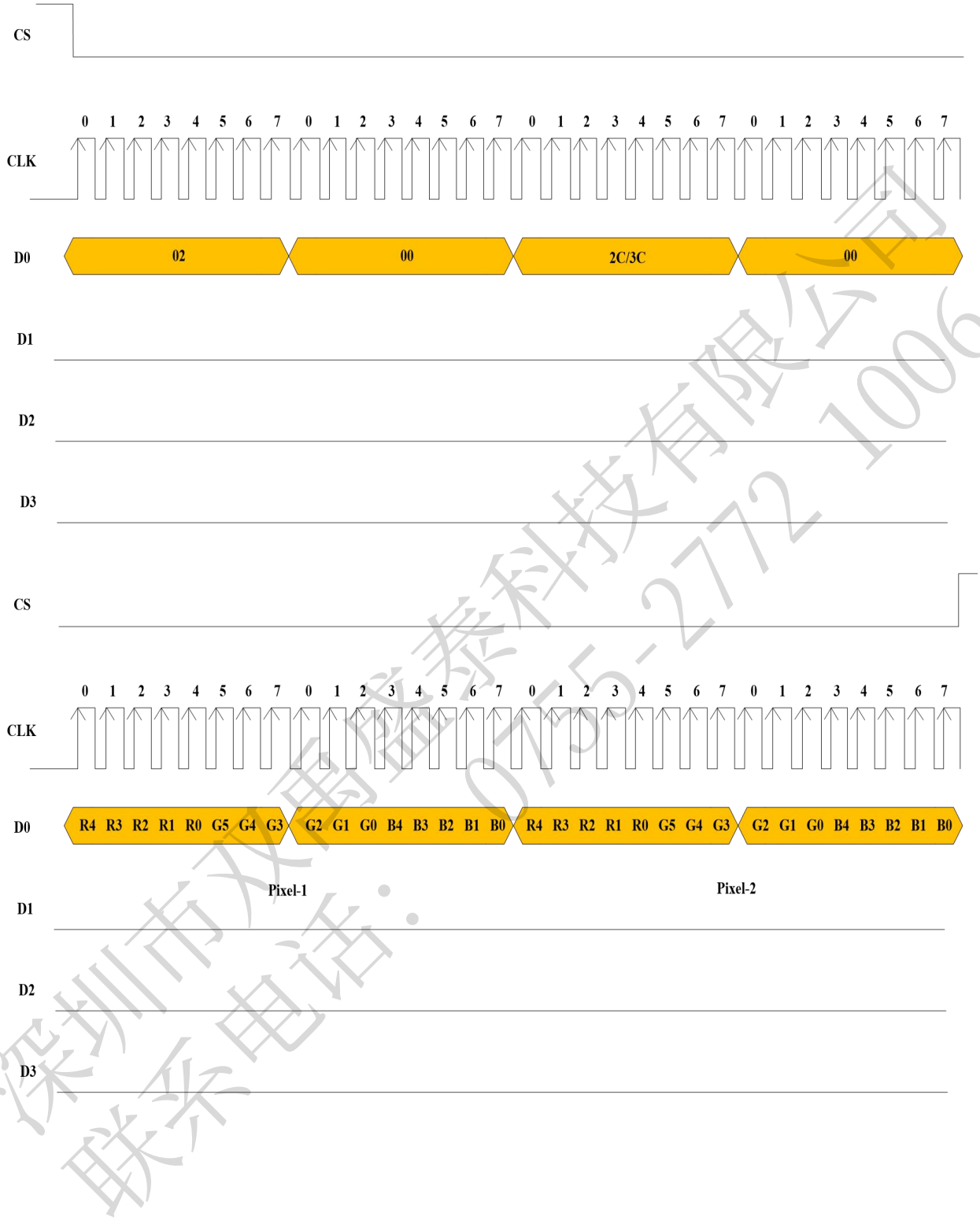
-256 gray，data：00000000~11111111

5.5.3.1 1wire data: only use SDA, first byte=0x02

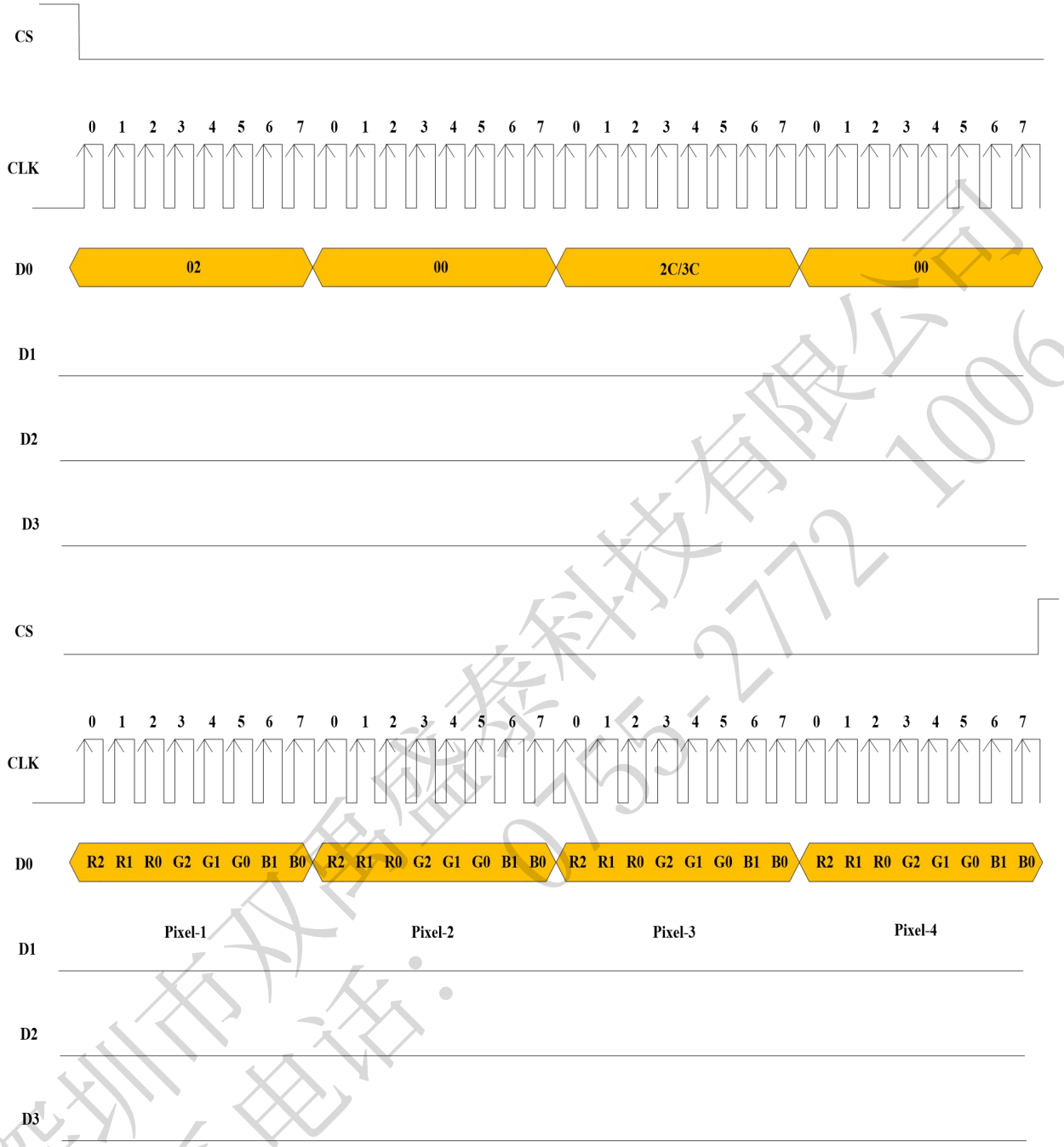
5.5.3.1.1 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input)



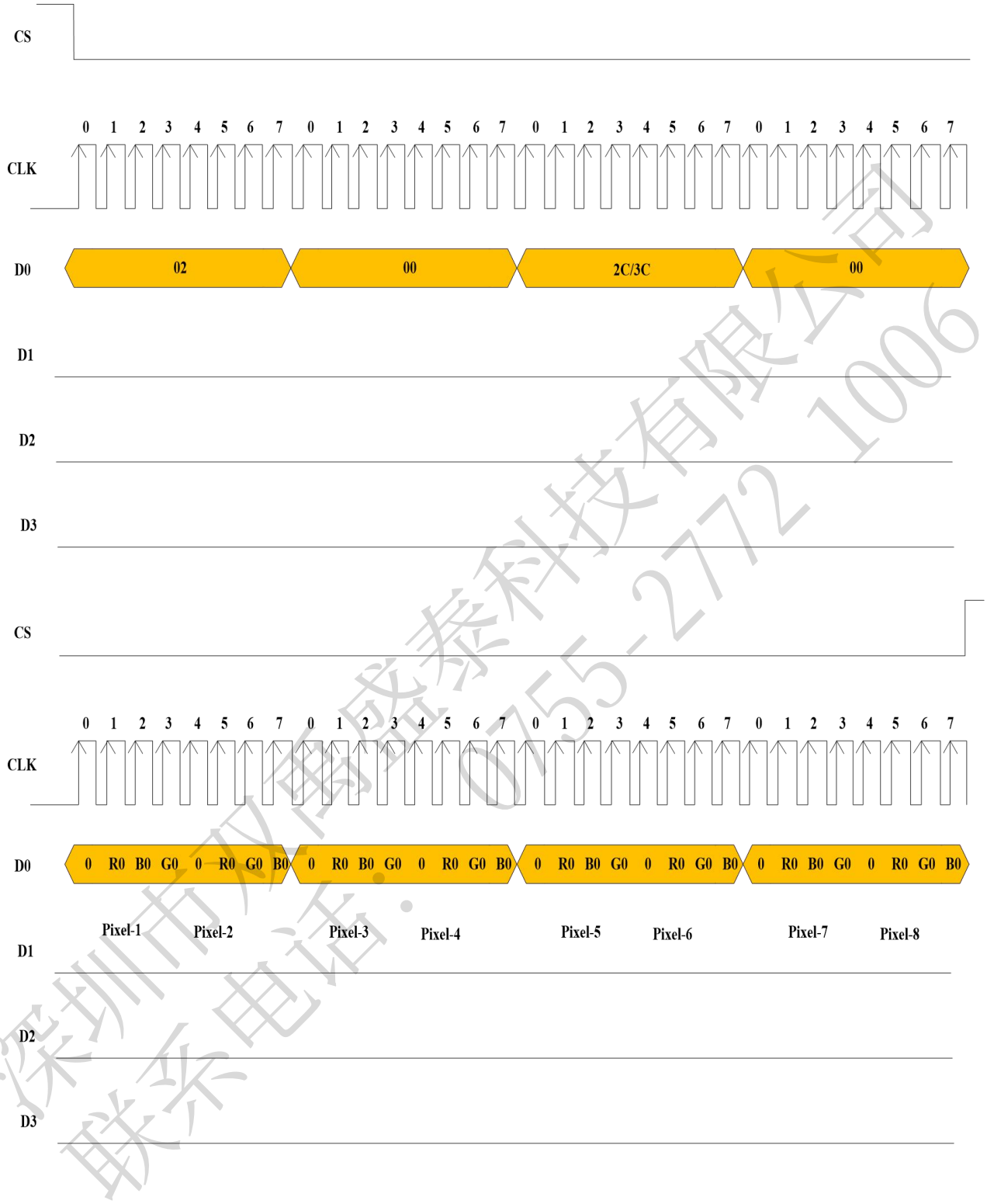
5.5.3.1.2 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input)



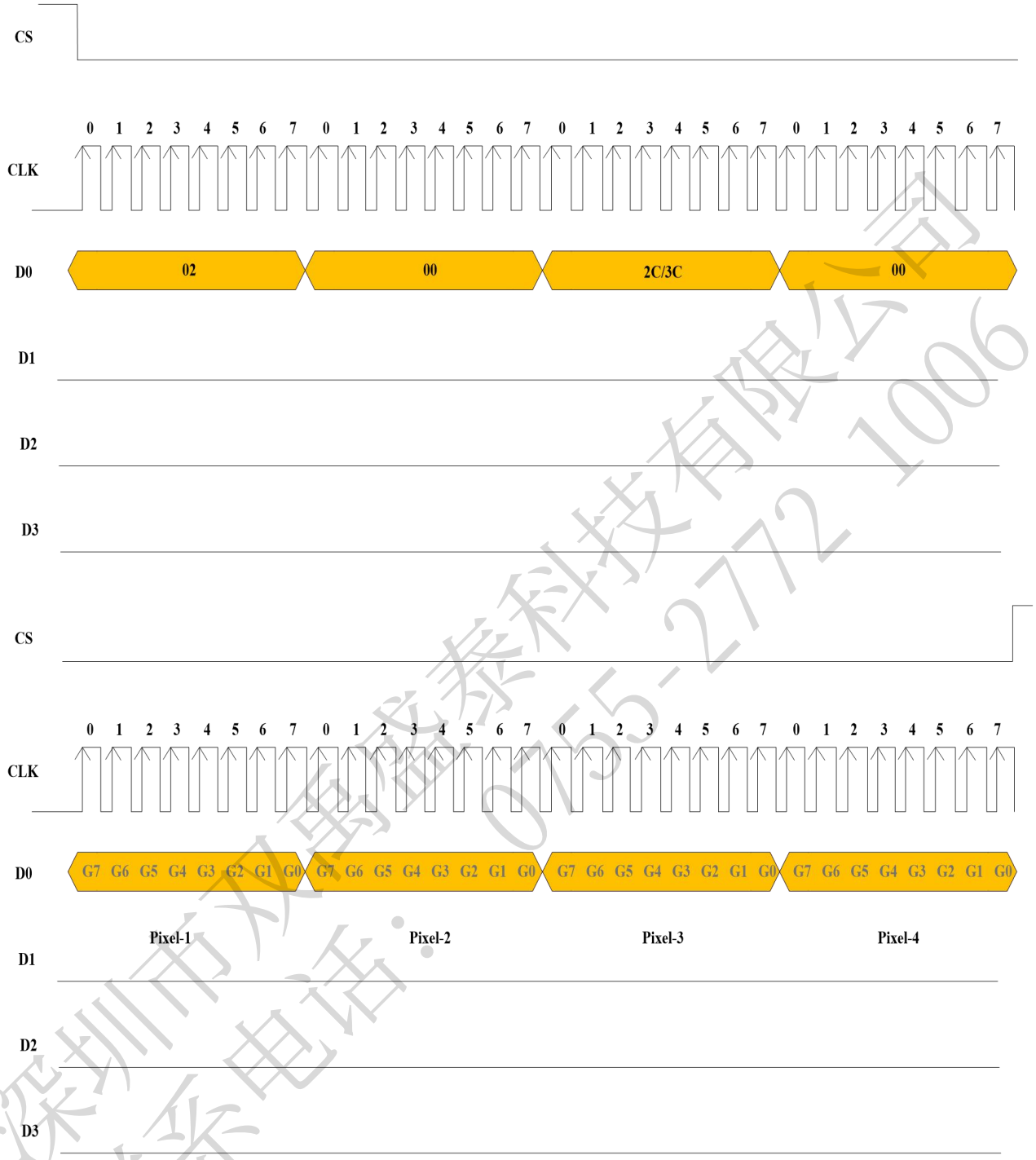
5.5.3.1.3 256-Colors:8-bit/pixel (RGB 3, 3,2 -bits input)



5.5.3.1.4 8-Colors:3-bit/pixel (RGB 1, 1,1 -bits input)

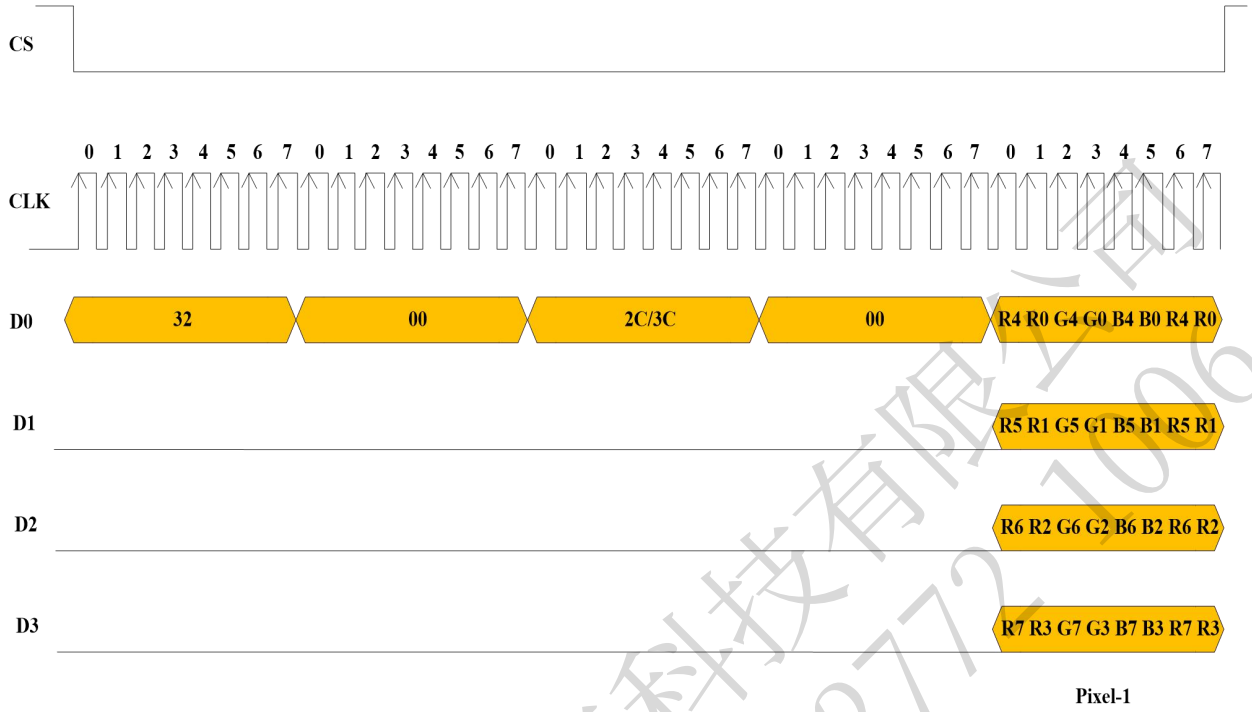


5.5.3.1.5 256GRAY(data:bin0~bin11111111)

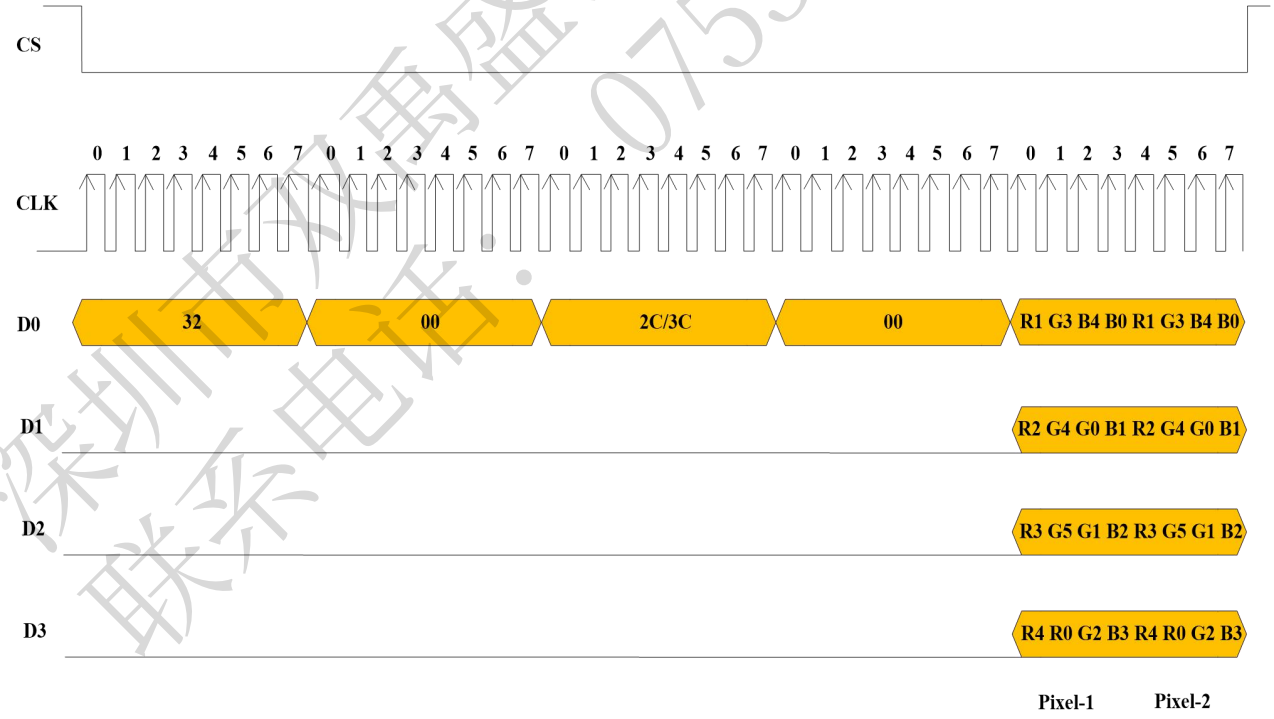


5.5.3.2 4wire data 1wire Addr: first byte=0x32

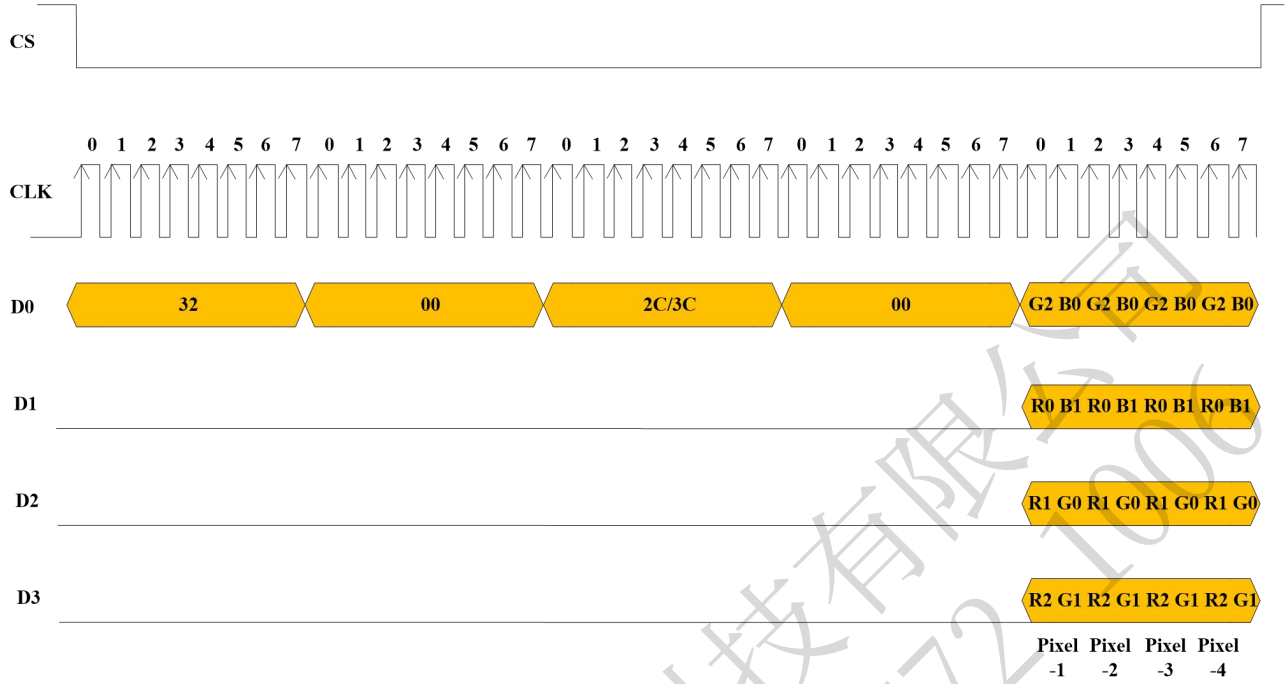
5.5.3.2.1 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input)



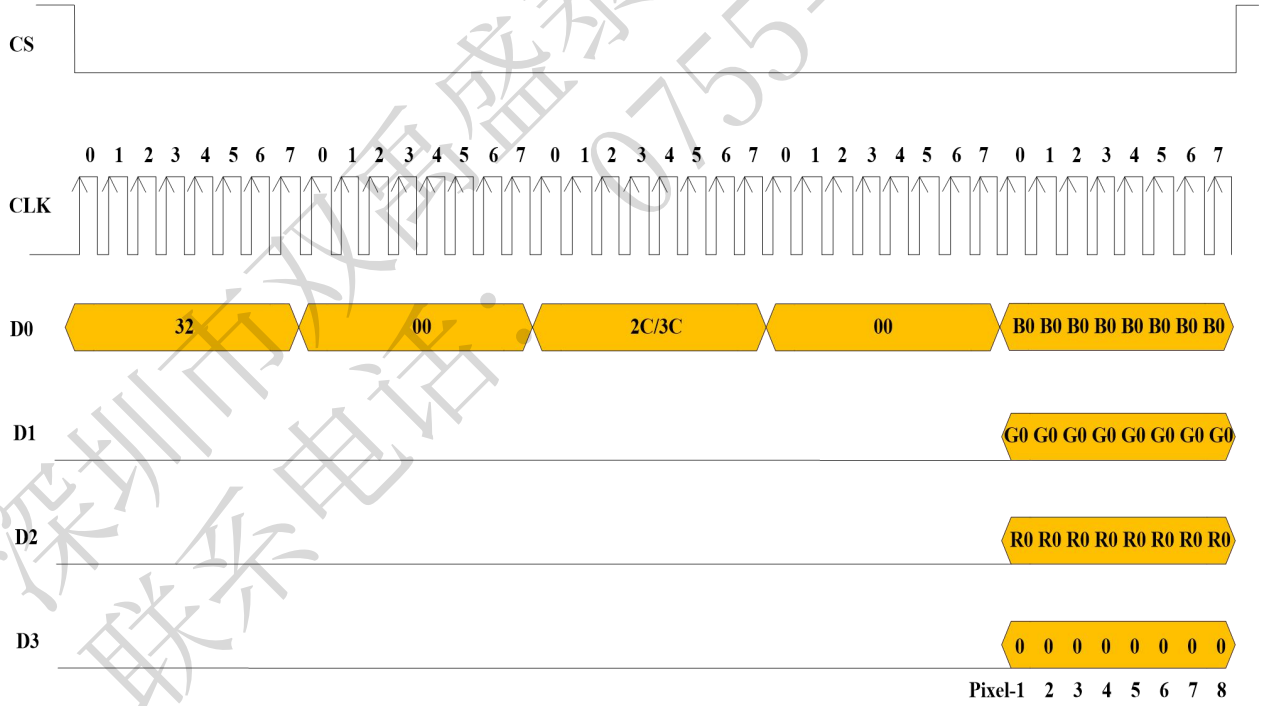
5.5.3.2.2 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input)



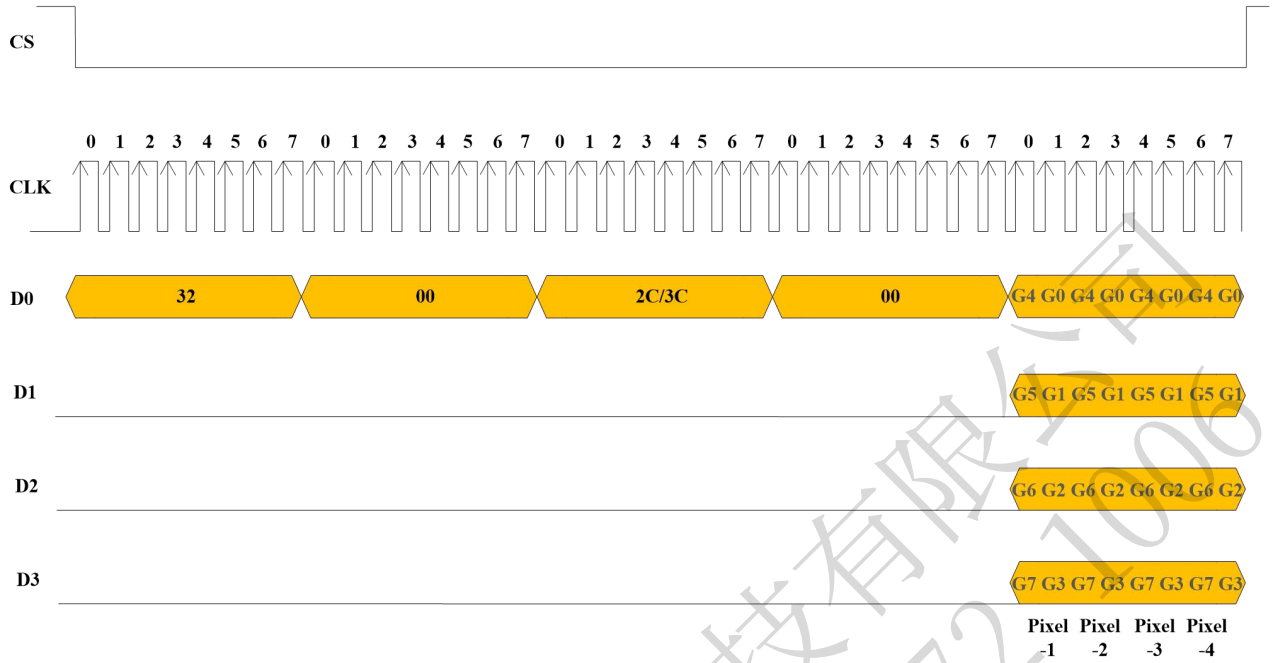
5.5.3.2.3 256-Colors:8-bit/pixel (RGB 3, 3,2 -bits input)



5.5.3.2.4 8-Colors:3-bit/pixel (RGB 1, 1,1 -bits input)

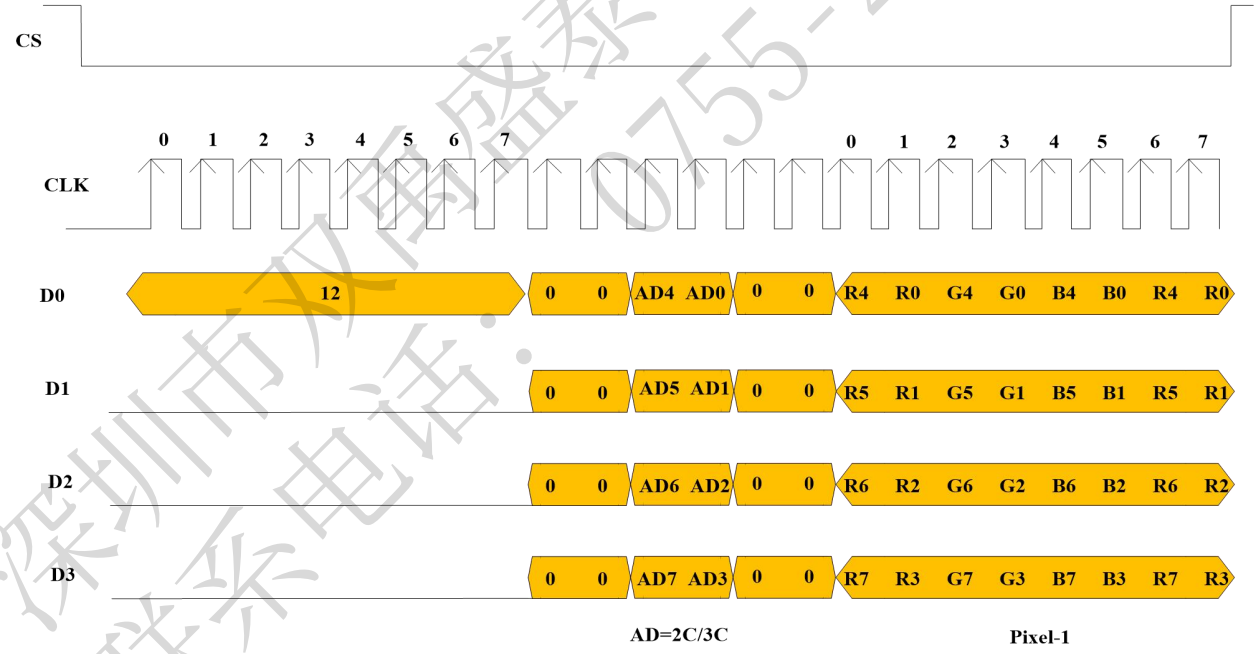


5.5.3.2.5 256GRAY(data:bin0~bin11111111)

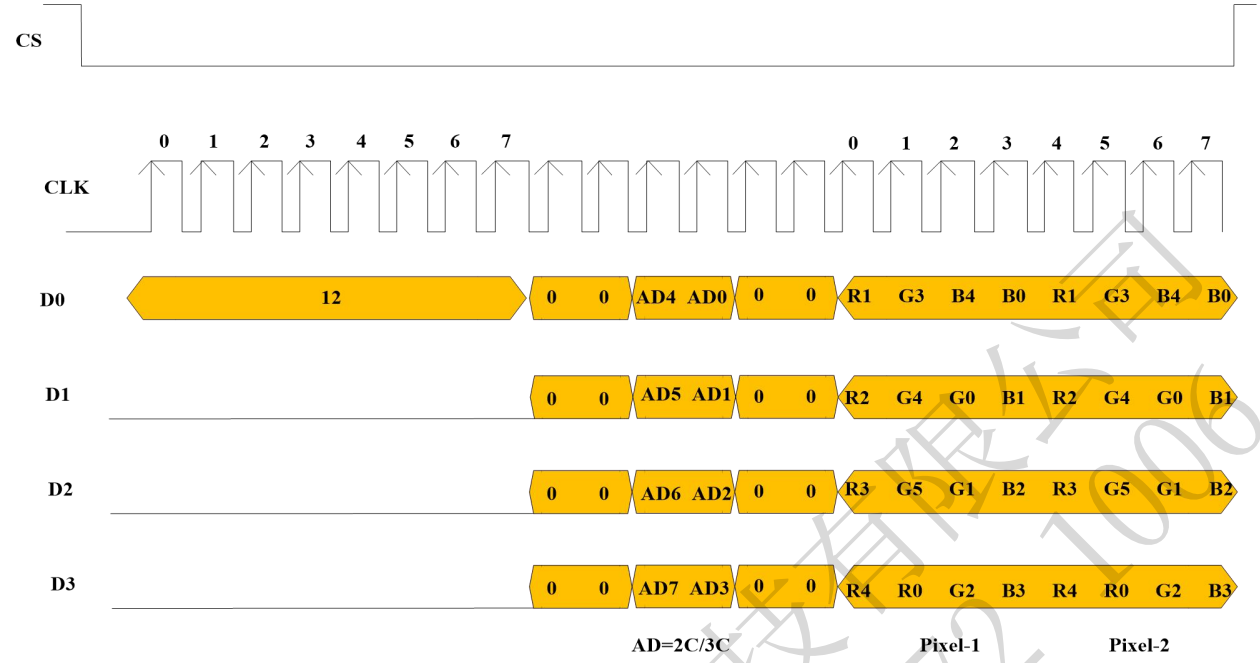


5.5.3.3 4wire data 4wire Addr: first byte=0x12

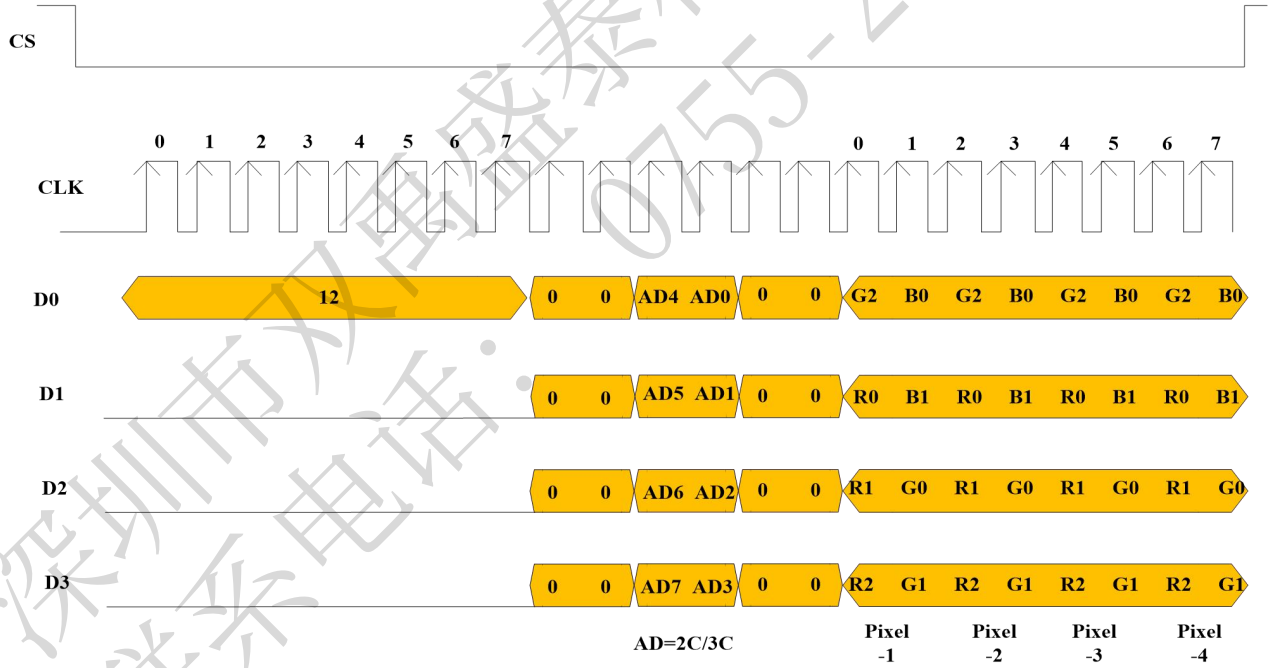
5.5.3.3.1 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input)



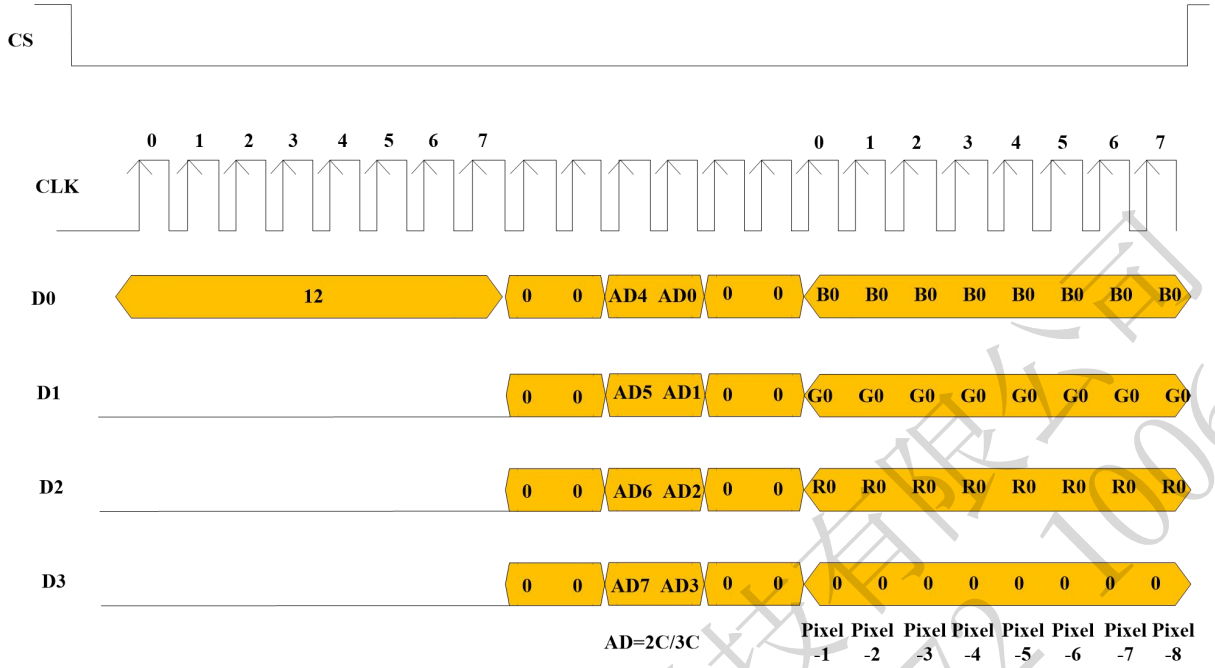
5.5.3.3.2 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input)



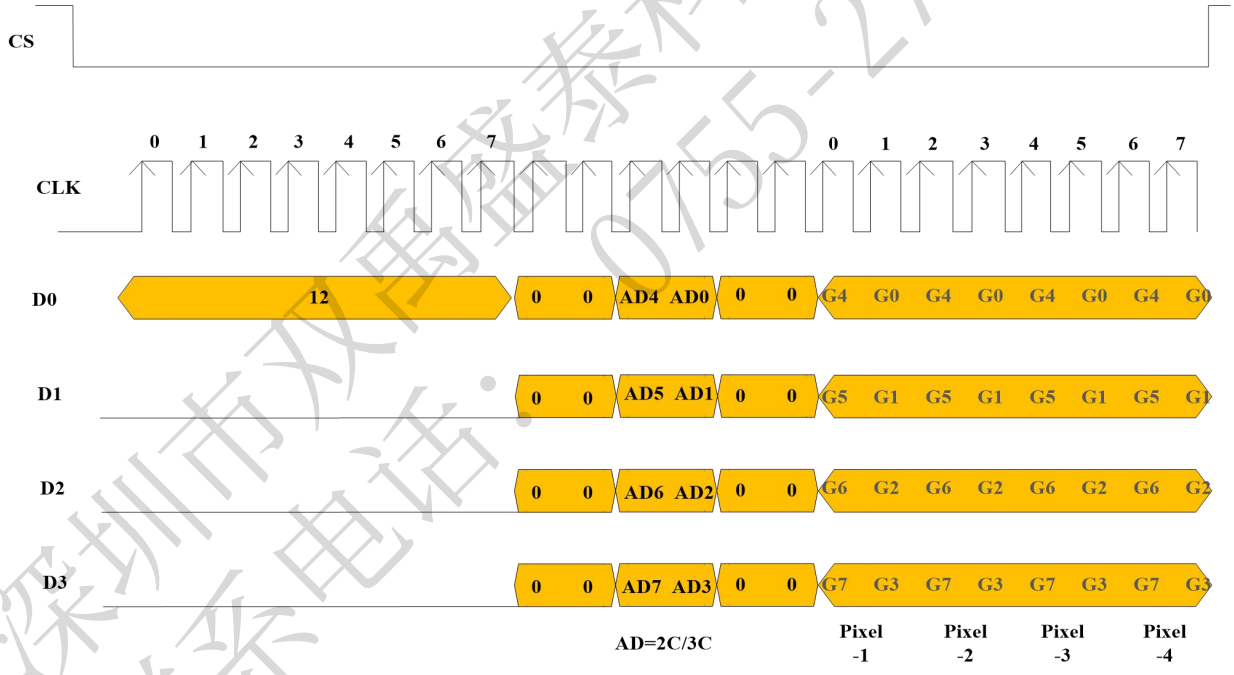
5.5.3.3.3 256-Colors:8-bit/pixel (RGB 3, 3,2 -bits input)



5.5.3.3.4 8-Colors:3-bit/pixel (RGB 1, 1,1 -bits input)



5.5.3.3.5 256GRAY(data:bin0~bin11111111)



5.6 8080-Series MCU Interface

5.6.1 8080-Series MCU Write Cycle Sequence

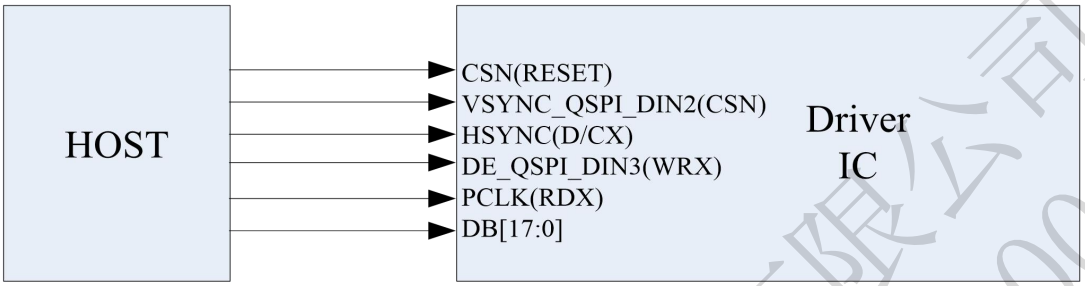
The write cycle means that the host writes information (register index / parameter) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (DB[23:0]). D/CX is a control signal, which tells if the data is an index or a parameter. The data signals represent index number if the signal is low (D/CX=’0’) and

vice versa the data signals represent parameter (D/CX=’1’).

5.6.2 18-bit 8080-Series Interface Write Format

Connect Pin:
DB[17:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN

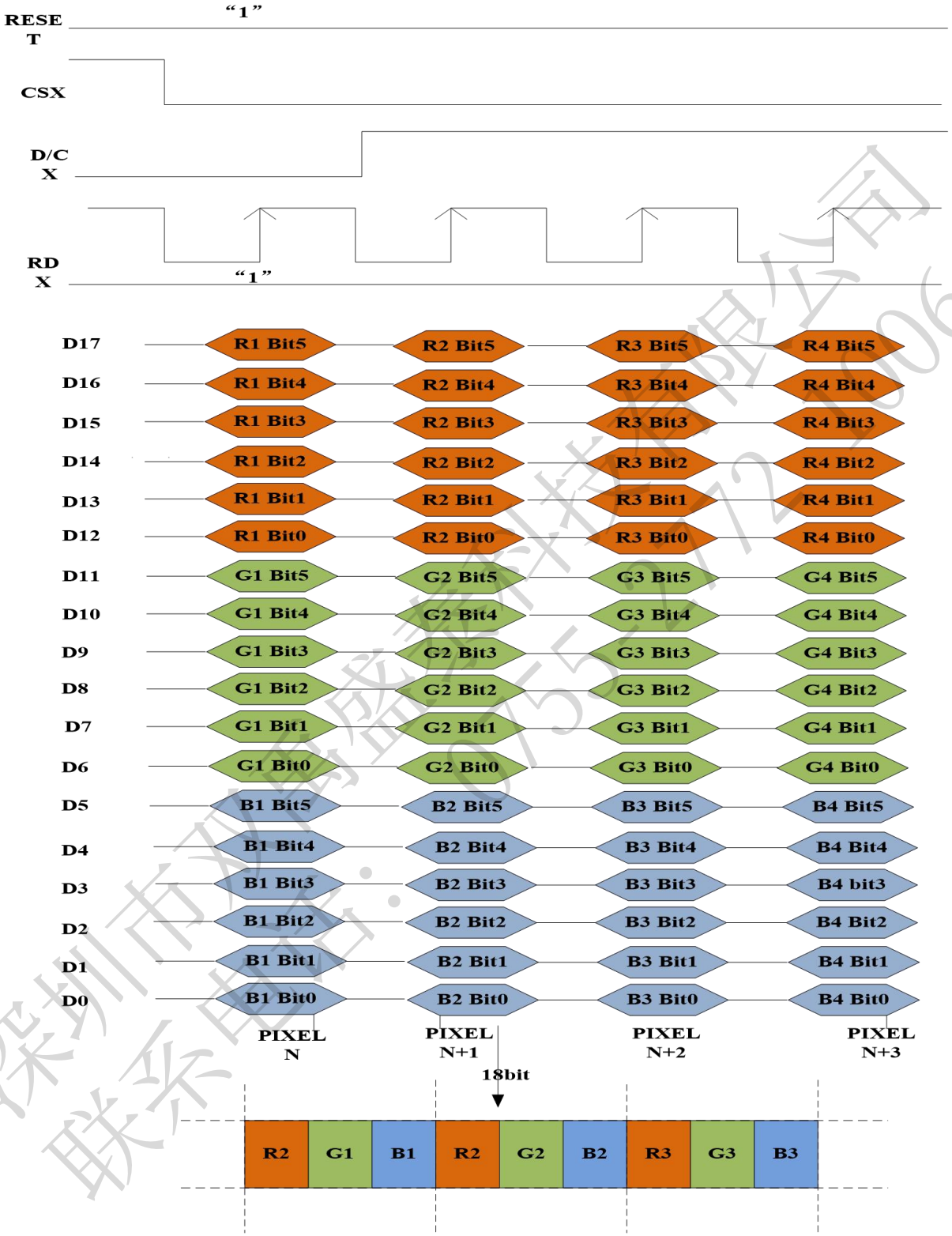
The 18-bit 8080-series interface is selected by setting the IM [3:0] =“0111”.低 18bits/高



18-bit 8080-Series Interface Connection

This mode accepts only 262k colors format in display. In this interface, index, parameter, and pixel-data should be written according to the following figures.

5.6.2.1 18-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input)262K-Colors

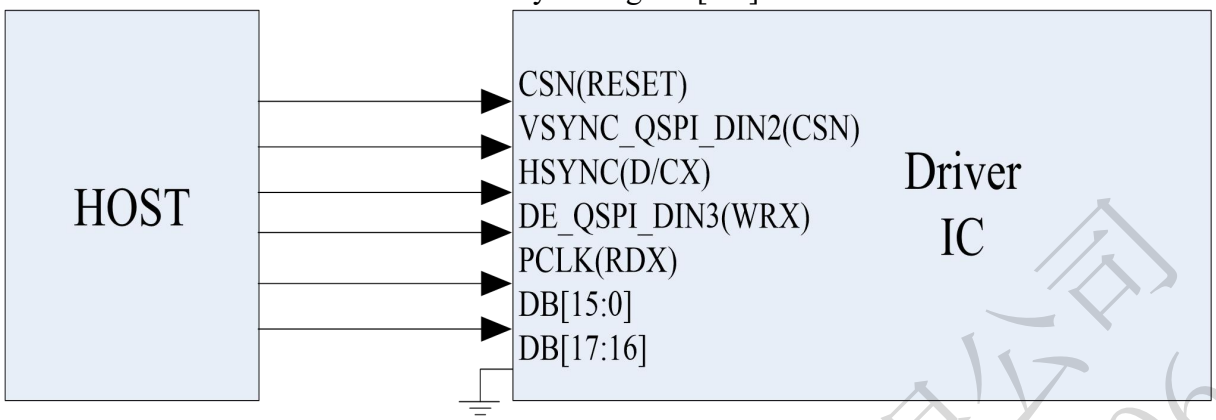


5.6.3 16-bit 8080-Series Interface Write Format

Connect Pin:

DB[15:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN

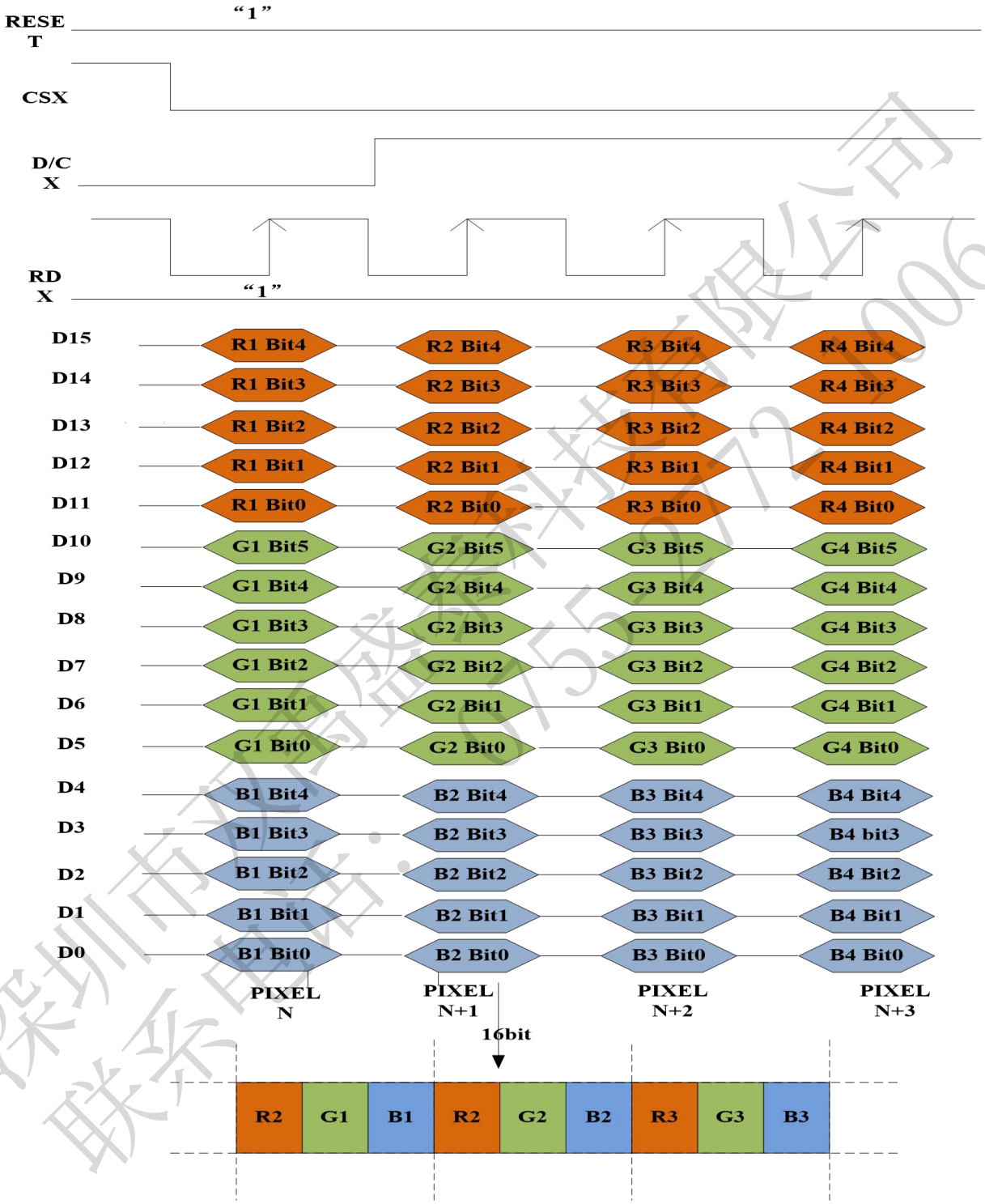
The 16-bit 8080-series interface is selected by setting IM[3:0]=”1000”.



16-bit 8080-Series Interface Connection

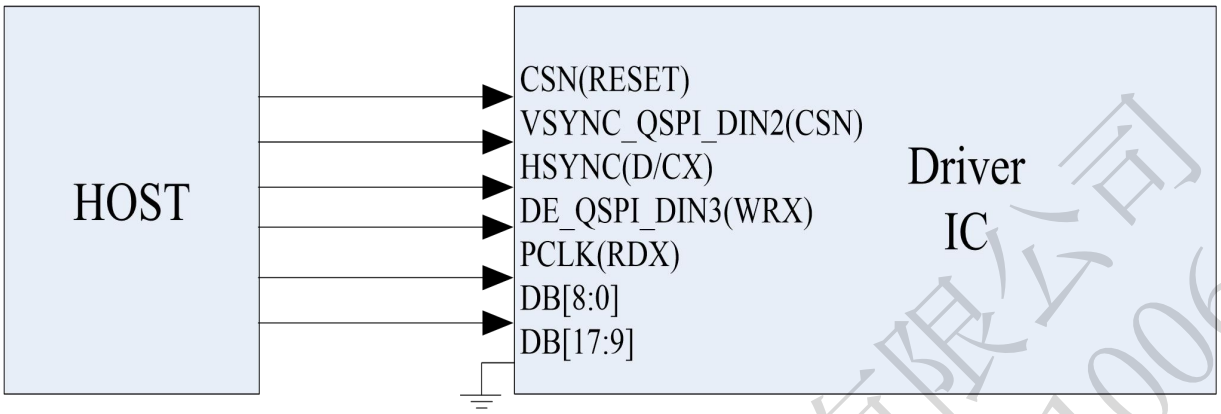
AXS15260 accepts 262k-color or 65k-color format in this mode. When the 262k-color format is used, two transfers for each pixel are required.

5.6.3.1 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input) 65K-Color



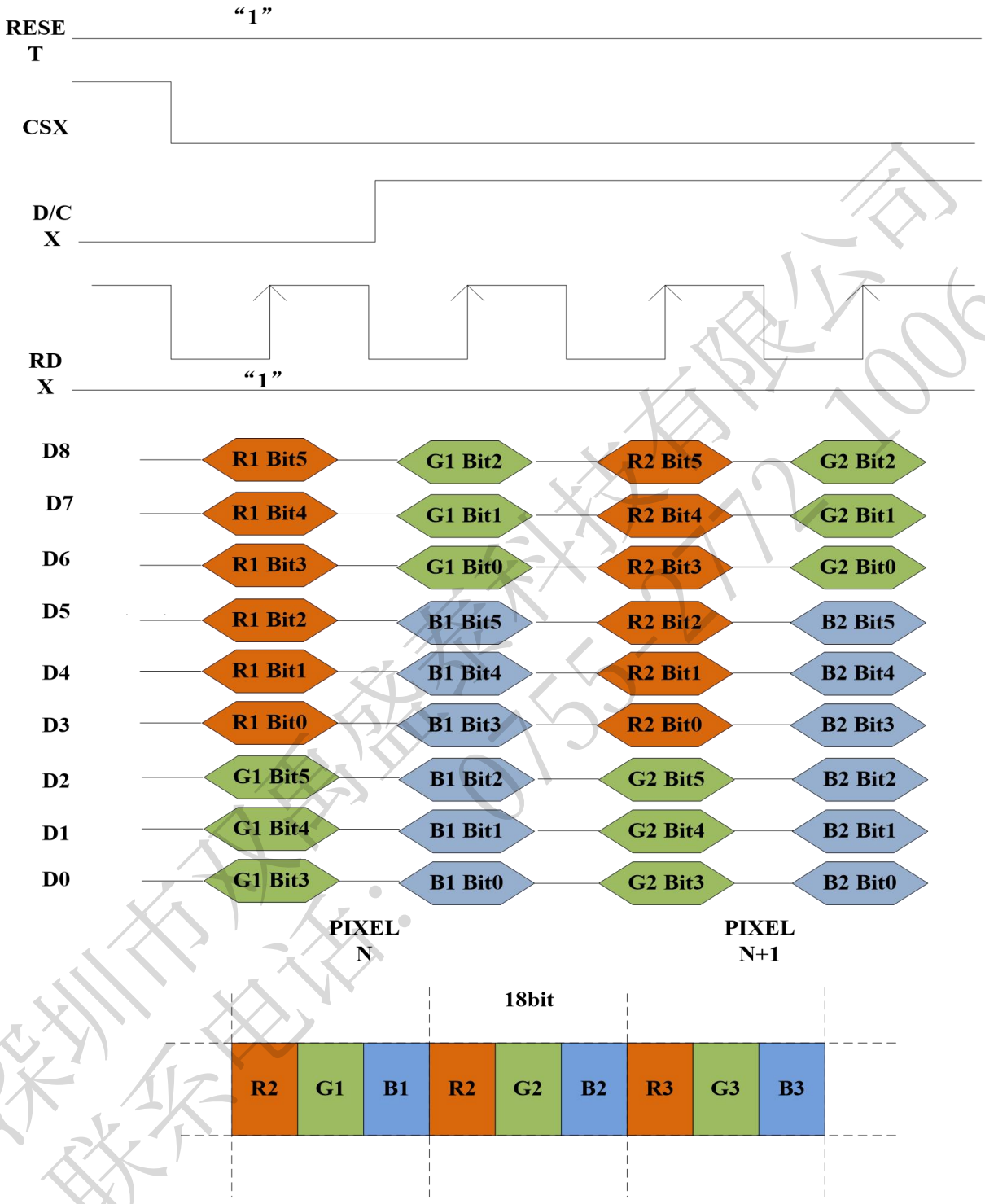
5.6.4 9-bit 8080-Series Interface Write Format

Connect Pin:
DB[8:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN
The 9-bit 8080-series interface is selected by setting the IM [3:0] = “1001”.



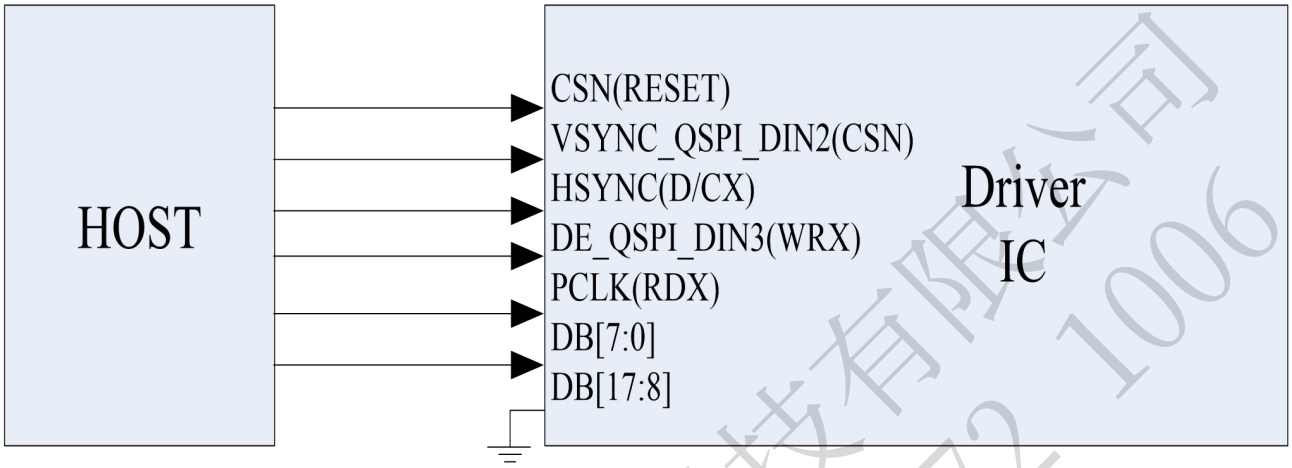
9-bit 8080-Series Interface Connection

5.6.4.1 9-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input)262K-Colors



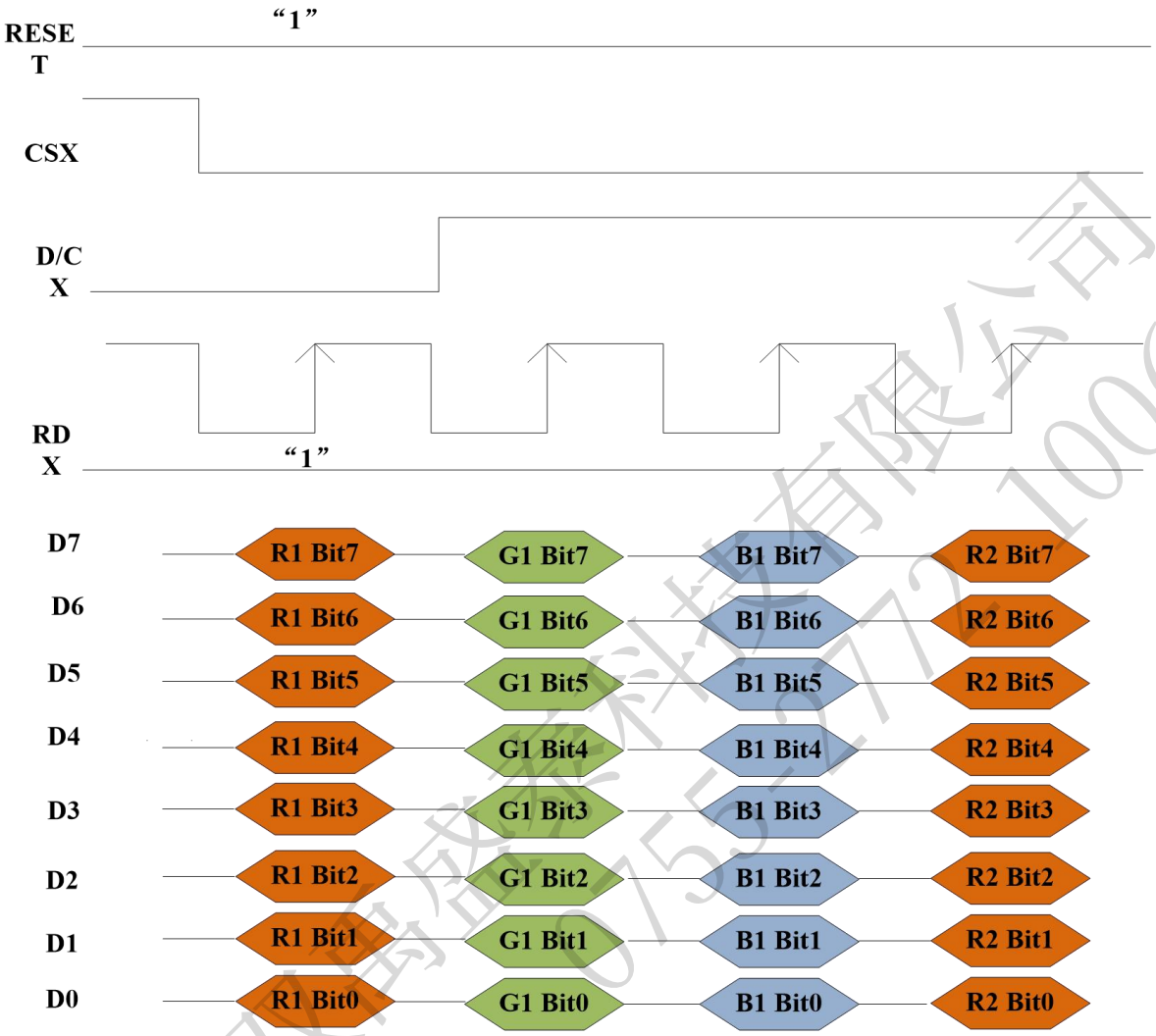
5.6.5 8-bit 8080-Series Interface Write Format

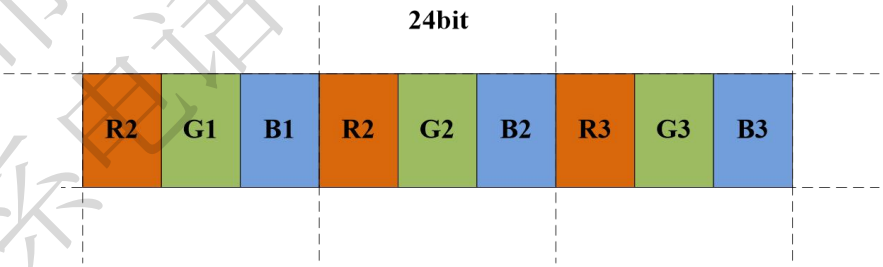
Connect Pin:
DB[7:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX),DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN
The 8080 8-bit interface is selected by setting the IM [3:0] as “1010”.



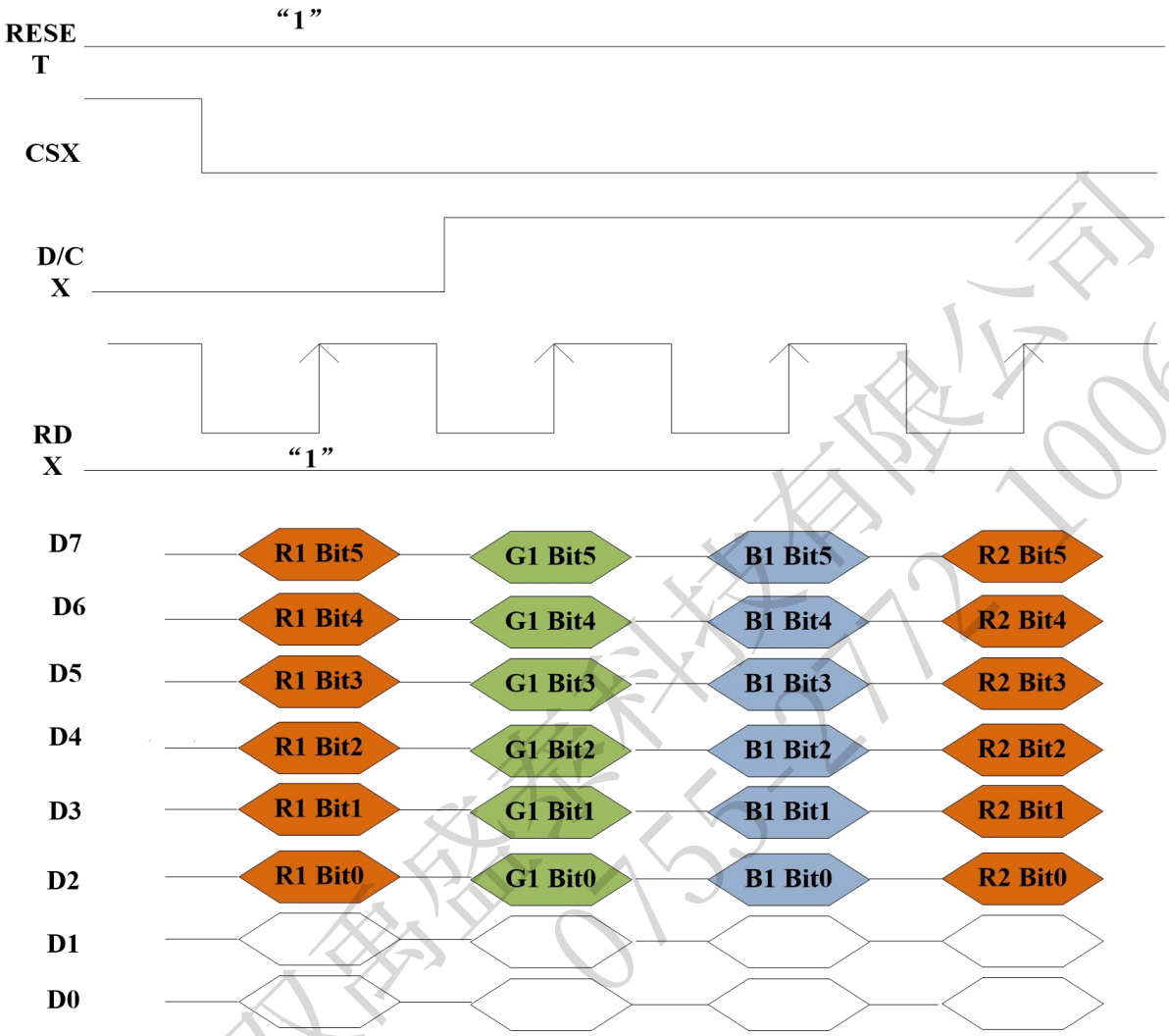
8-bit 8080-Series Interface Connection

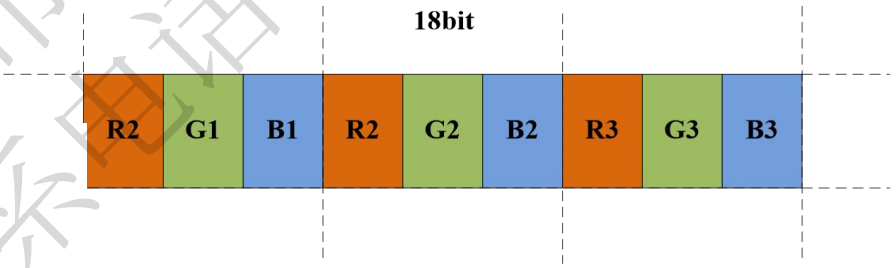
5.6.5.1 8-bit data bus for 24-bit/pixel (RGB 8-8-8-bit input)16.7M-Colors



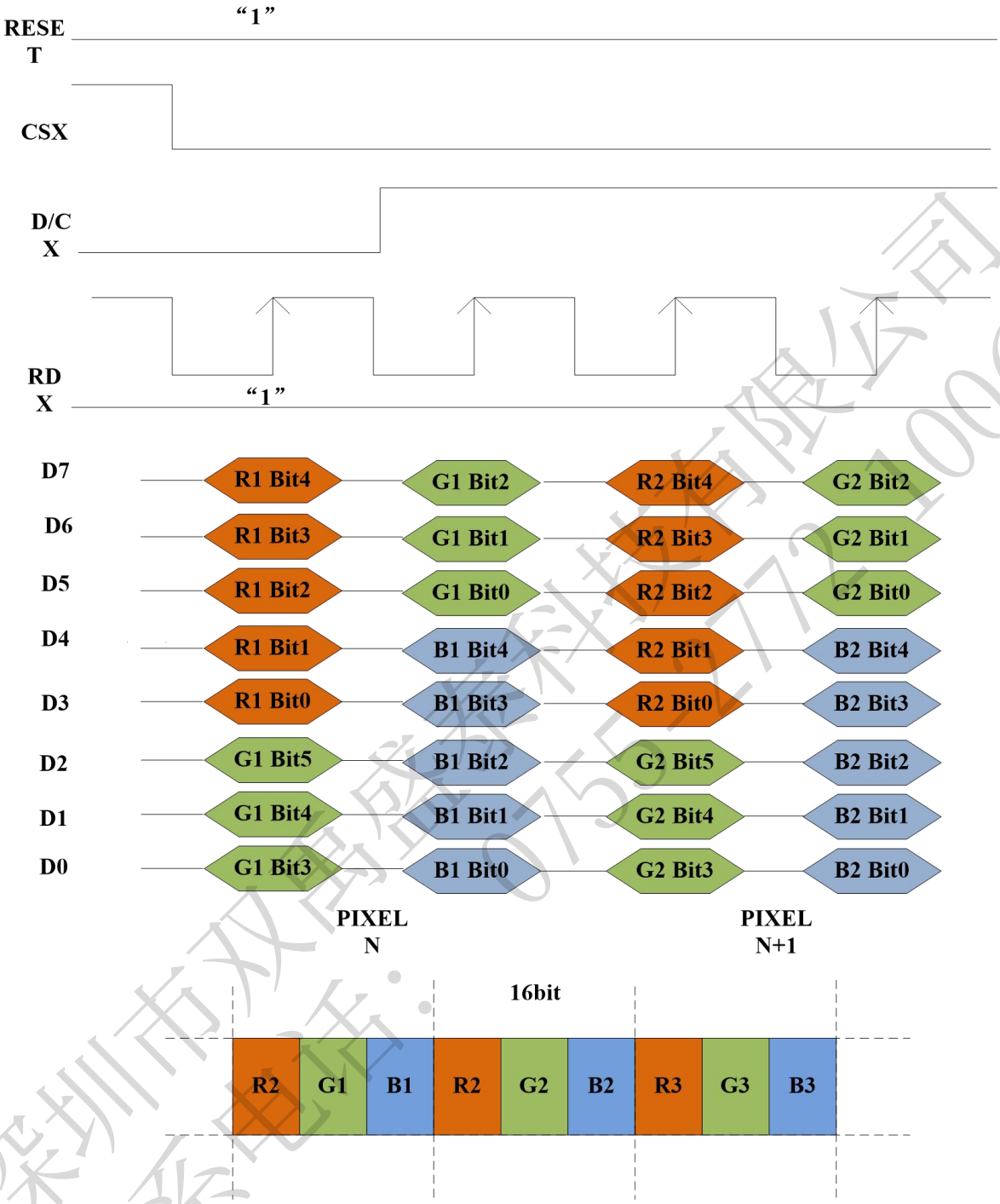


5.6.5.2 8-bit data bus for 18-bit/pixel (RGB 6-6-6L-bit input)262K-Colors





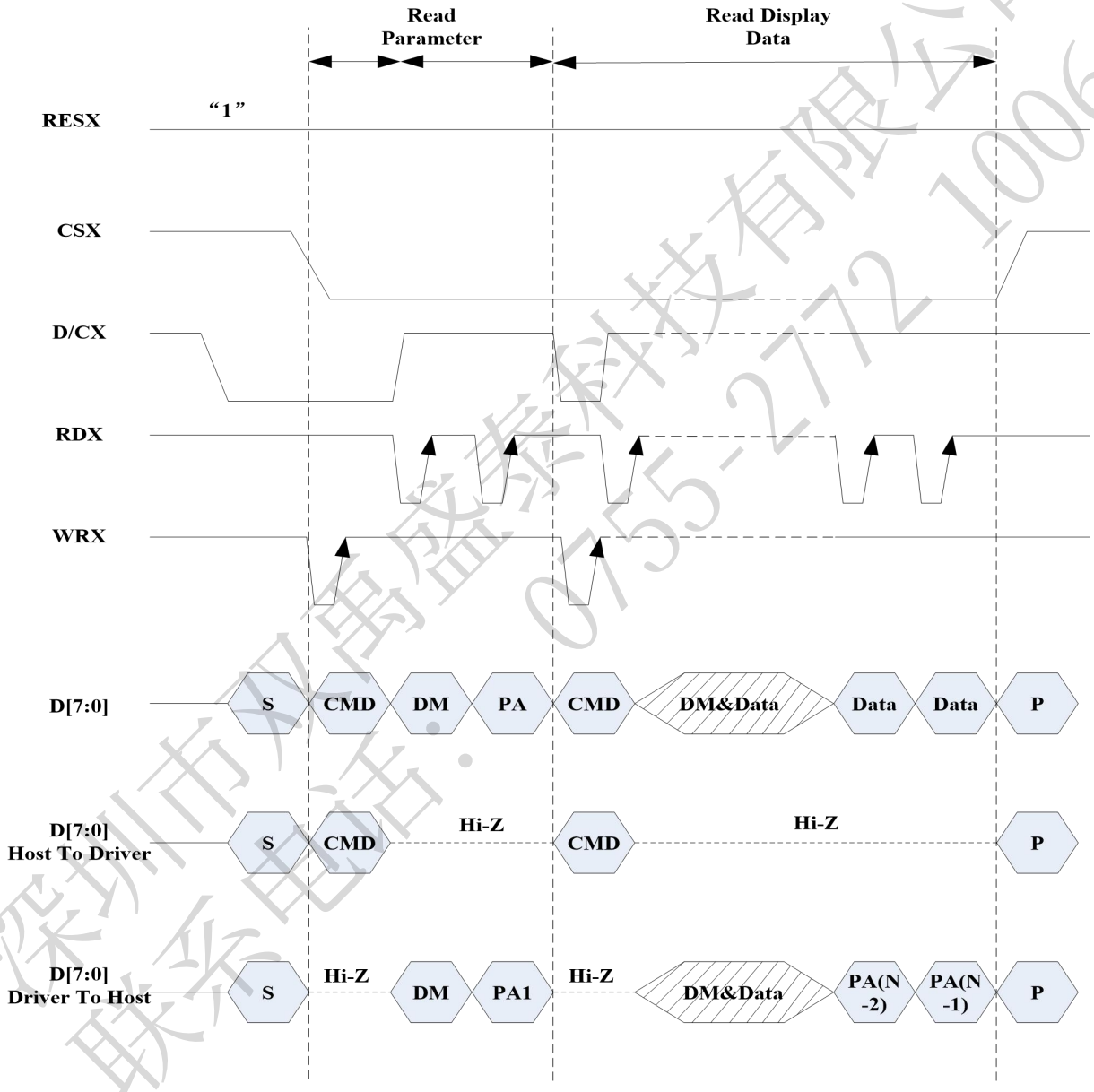
5.6.5.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input)65K-Colors



5.6.6 8080-Series MCU Read Cycle Sequence

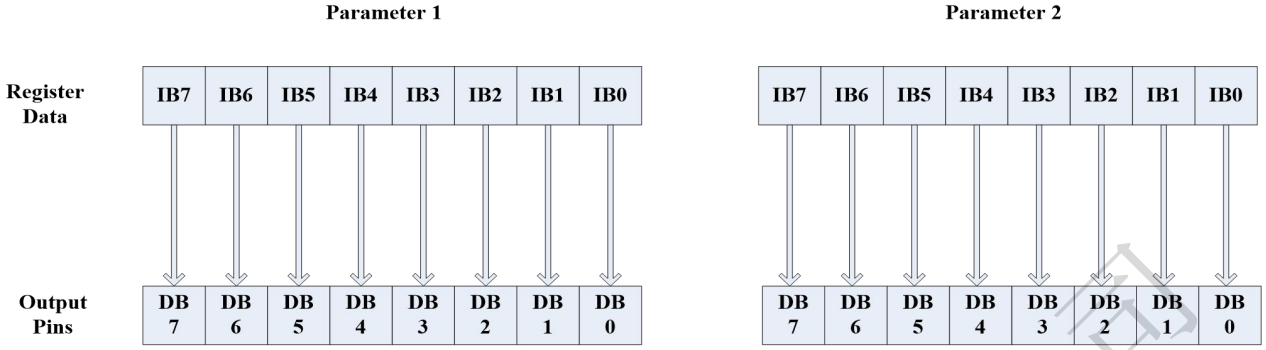
The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The driver sends data (DB [7:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

8080-series interface read Protocol



8080-series interface read Protocol,read data from register

5.6.6.1.1 8-bit data bus



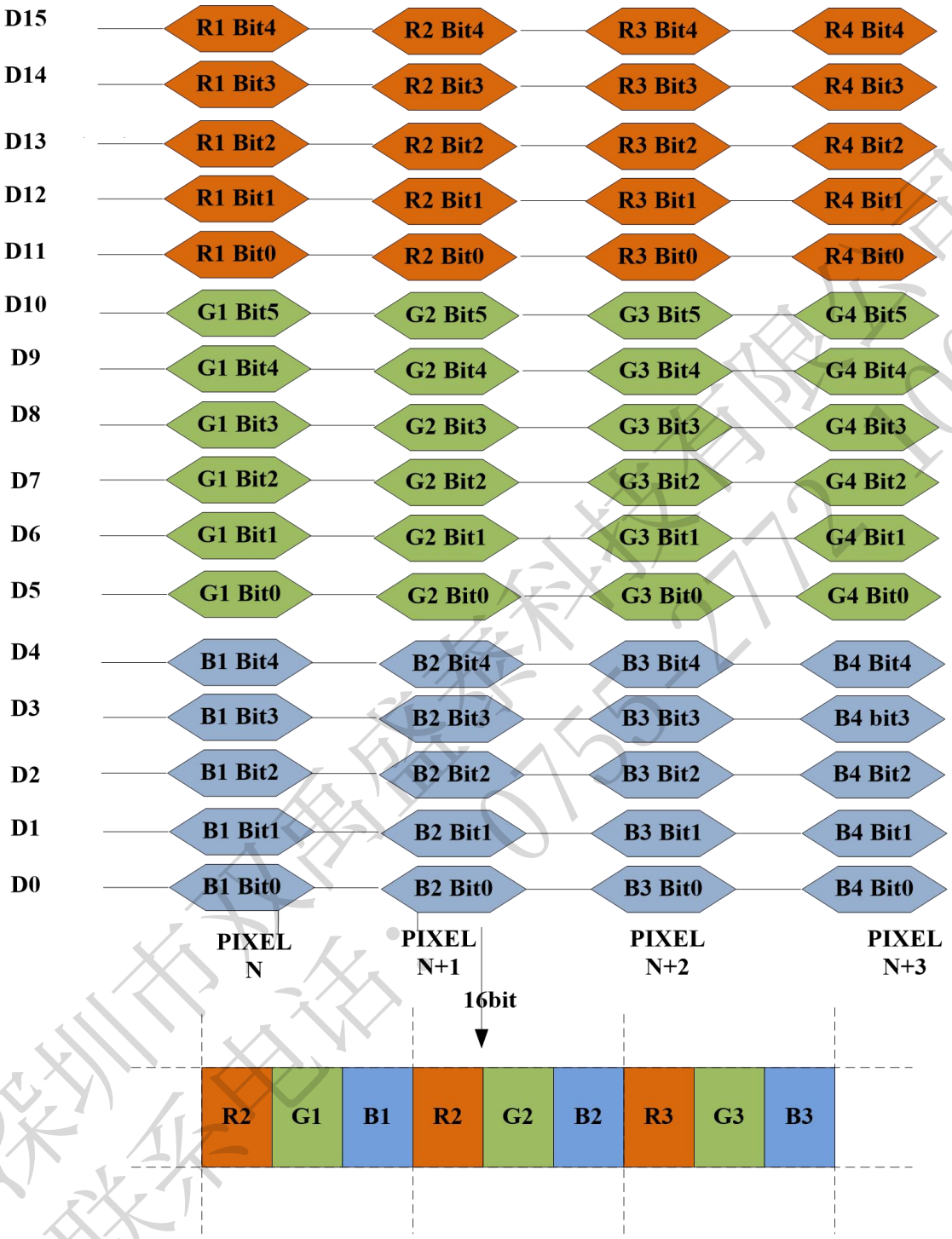
5.7 RGB Interface

5.7.1 RGB Color Format

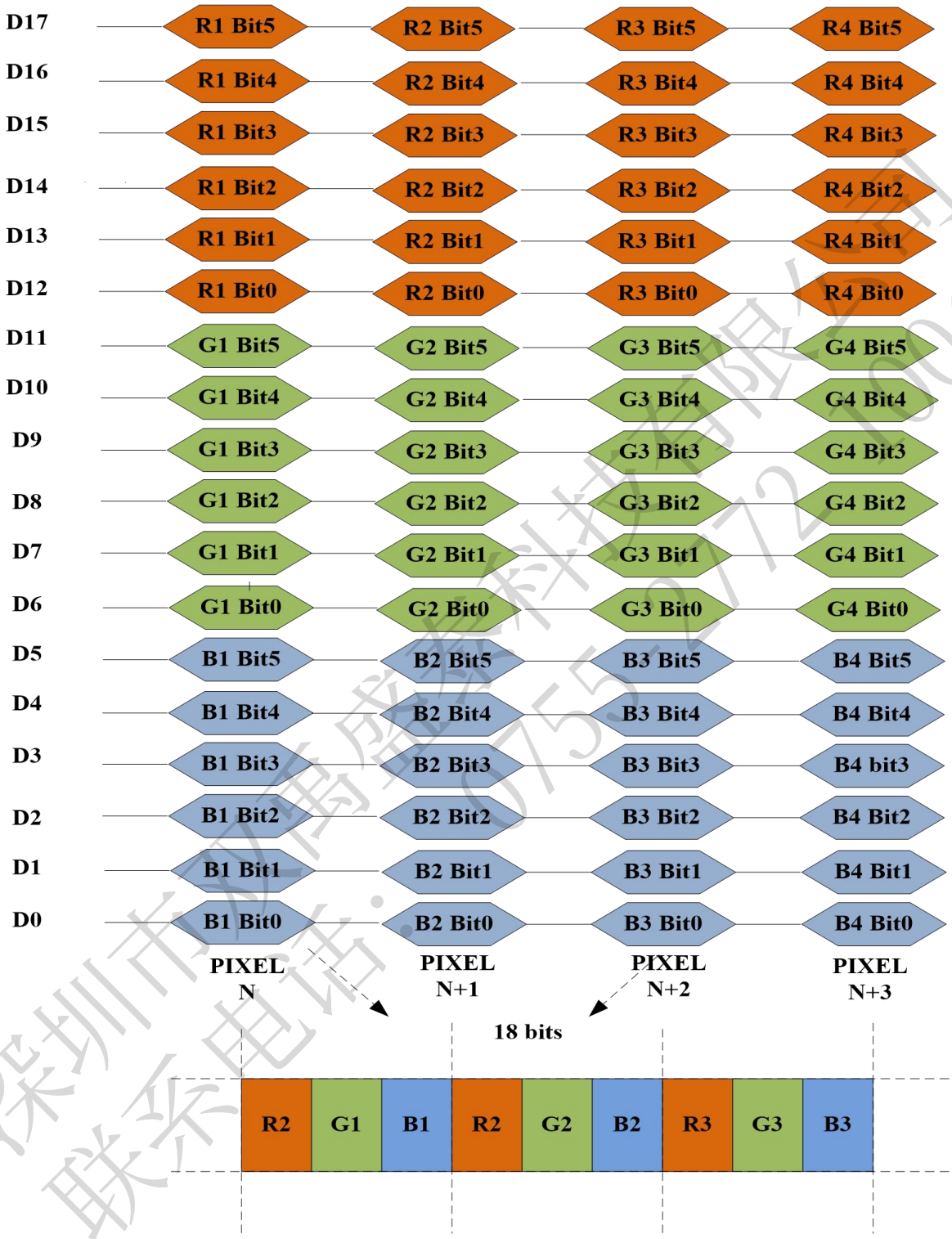
Connect Pin:DB[15/17/23:0],VSYNC_QSPI_DIN2,HSYNC,DE_QSPI_DIN3,PCLK

AXS15260 supports two kinds of RGB interface, DE mode， and 16bit/18bit/24bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, DB[15/17/23:0] pins can be used; When using RGB interface, only serial interface can be selected. IM [3:0] as “1110”。

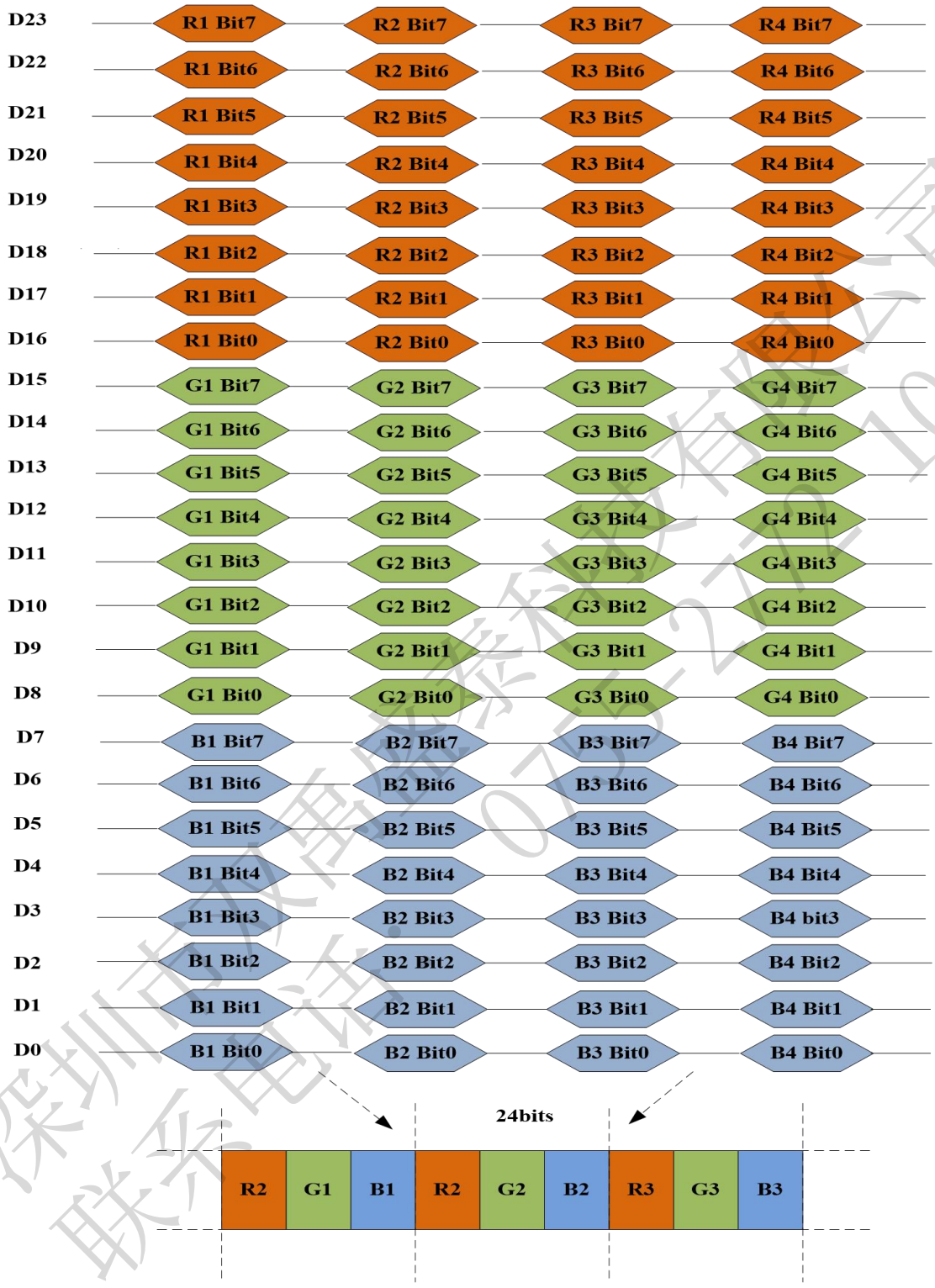
5.7.1.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input)65K-Colors



5.7.1.2 Write data for 18-bit/pixel (RGB 6-6-6-bit input)262K-Colors

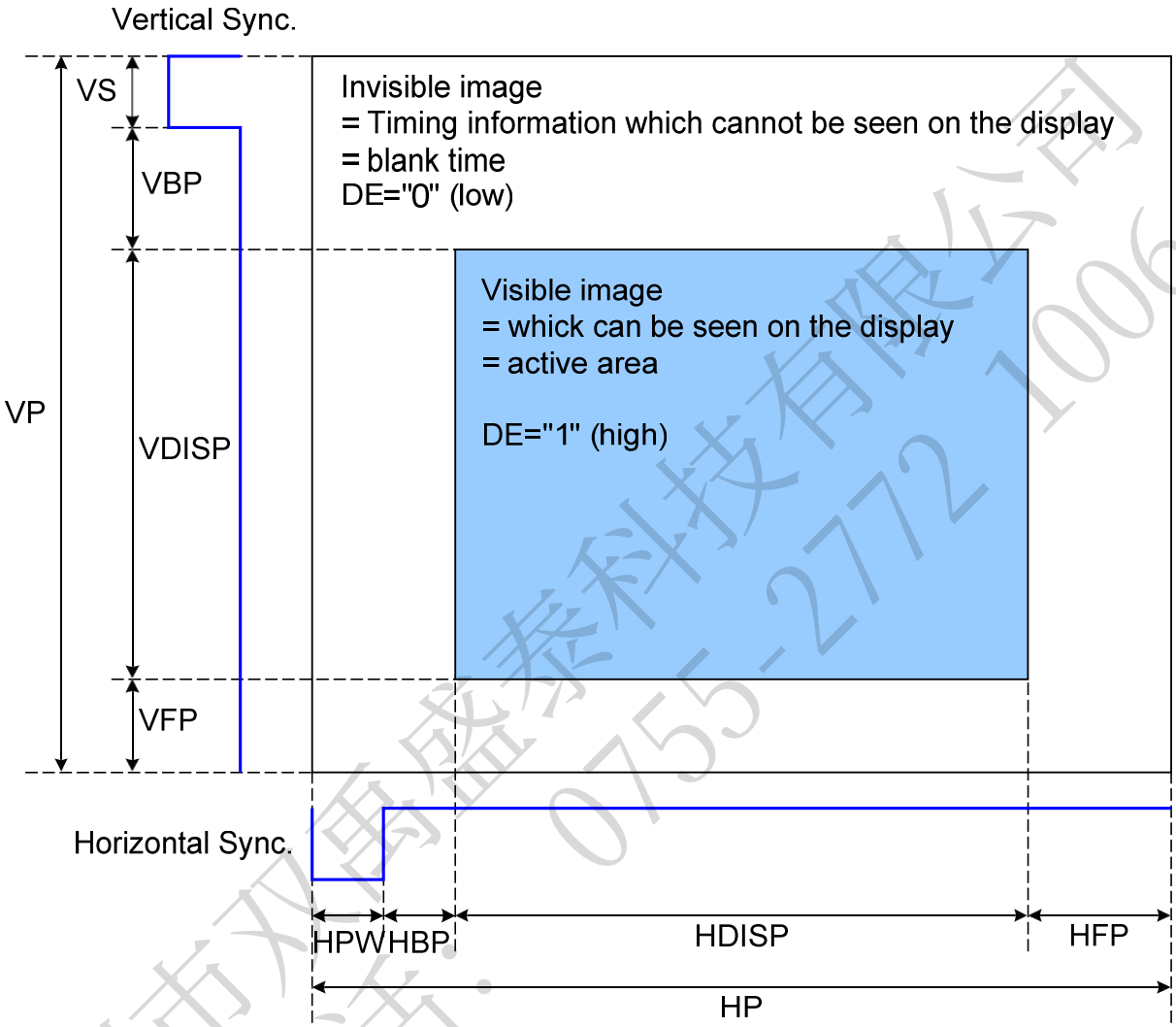


5.7.1.3 Write data for 24-bit/pixel (RGB 8-8-8-bit input)16.7M-Colors



5.7.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within



the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

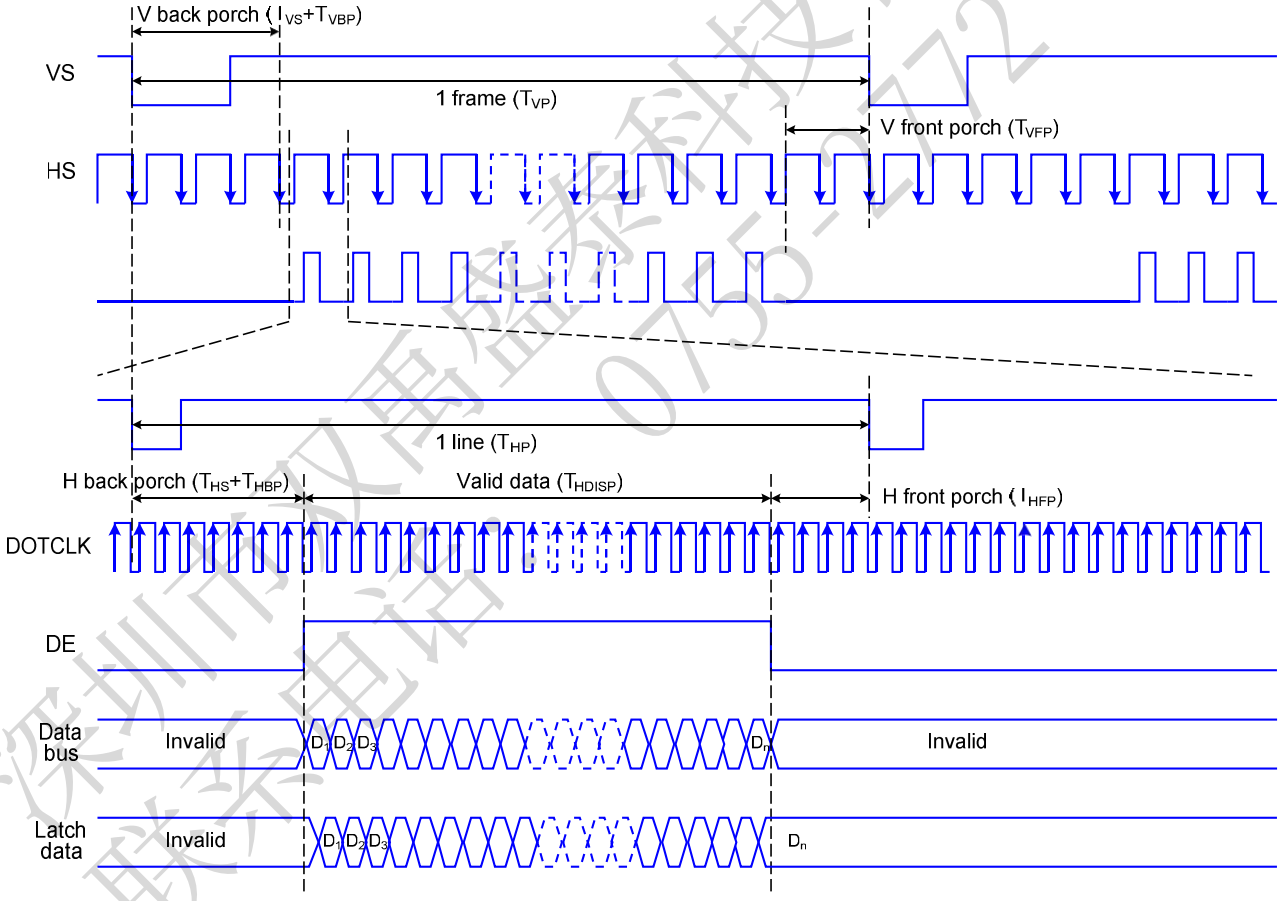
DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	-	2	hpw+hbp=75	Clock
Horizontal Sync. Back Porch	hbp	-	30		Clock
Horizontal Sync. Front Porch	hfp	-	30	-	Clock
Vertical Sync. Width	vs	-	2	-	Line
Vertical Sync. Back Porch	vbp	-	254		Line
Vertical Sync. Front Porch	vfp	-	10	-	Line

5.7.3 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

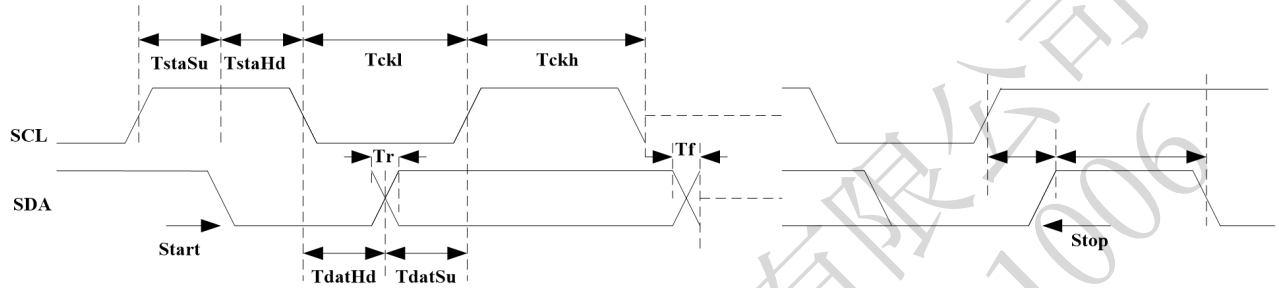
VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period. In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

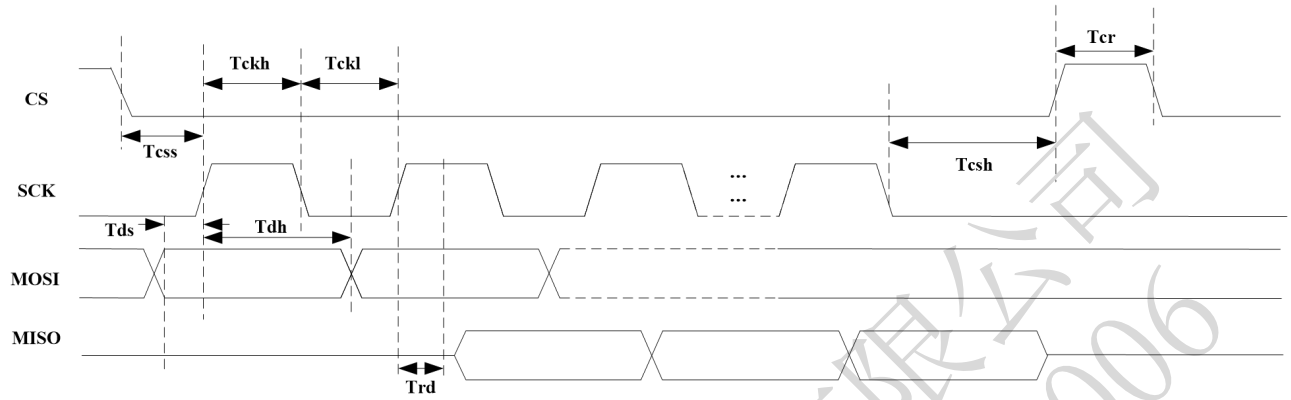
5.8 Touch part interface

5.8.1 I2C Interface



Parameter	Symbol	Min.	Typ	Max.	Unit
Working Frequency	F_{clk}	20	-	400	Khz
I2C Clock Low	T_{CKL}	1300	-	-	ns
I2C Clock High	T_{CKH}	600	-	-	ns
I2C Clock and Data rising time	T_r	-	-	300	ns
I2C Clock and Data falling time	T_f	-	-	300	ns
I2C Data hold time	T_{DatHd}	0	-	-	ns
I2C Data setup time	T_{DatSu}	100	-	-	ns
I2C Start Condition hold time	T_{StaHd}	600	-	-	ns
I2C Start Condition setup time	T_{StaSu}	600	-	-	ns
I2C Stop Condition setup time	T_{StpSu}	600	-	-	ns
I2C Bus free time	$T_{BusFree}$	1300	-	-	ns

5.8.2 SPI Interface



SPI Timing

Parameter	Symbol	Min.	Typ	Max.	Unit
SCK Frequency	f_{SCK}	-	-	18	Mhz
CS Set-up Time	t_{CSS}	200	-	-	ns
CS Hold Time	t_{CSH}	200	-	-	ns
CS Recovery Time	t_{CR}	1	-	-	ns
SCK clock High Time	t_{CKH}	27.8	-	-	ns
SCK clock Low Time	t_{CKL}	27.8	-	-	ns
Data Output Delay Time	t_{RD}	-	-	-	ns
Input Data Set-up Time	t_{DS}	25	-	-	ns
Input Data Hold Time	t_{DH}	25	-	-	ns

5.9 Display Reference Clock Function

The AXS15260 provides a function to decide internal oscillator for display clock reference of driver IC.

Relationship between Liquid Crystal Driver Duty and the Frame Frequency

The formula below is used to calculate the relationship between the liquid crystal driver duty and the frame frequency. The frame frequency is determined by setting the 1H period adjustment (RTN) bit.

RTN setting for 1H period:

Step1: To decide real one line period in Command Mode:

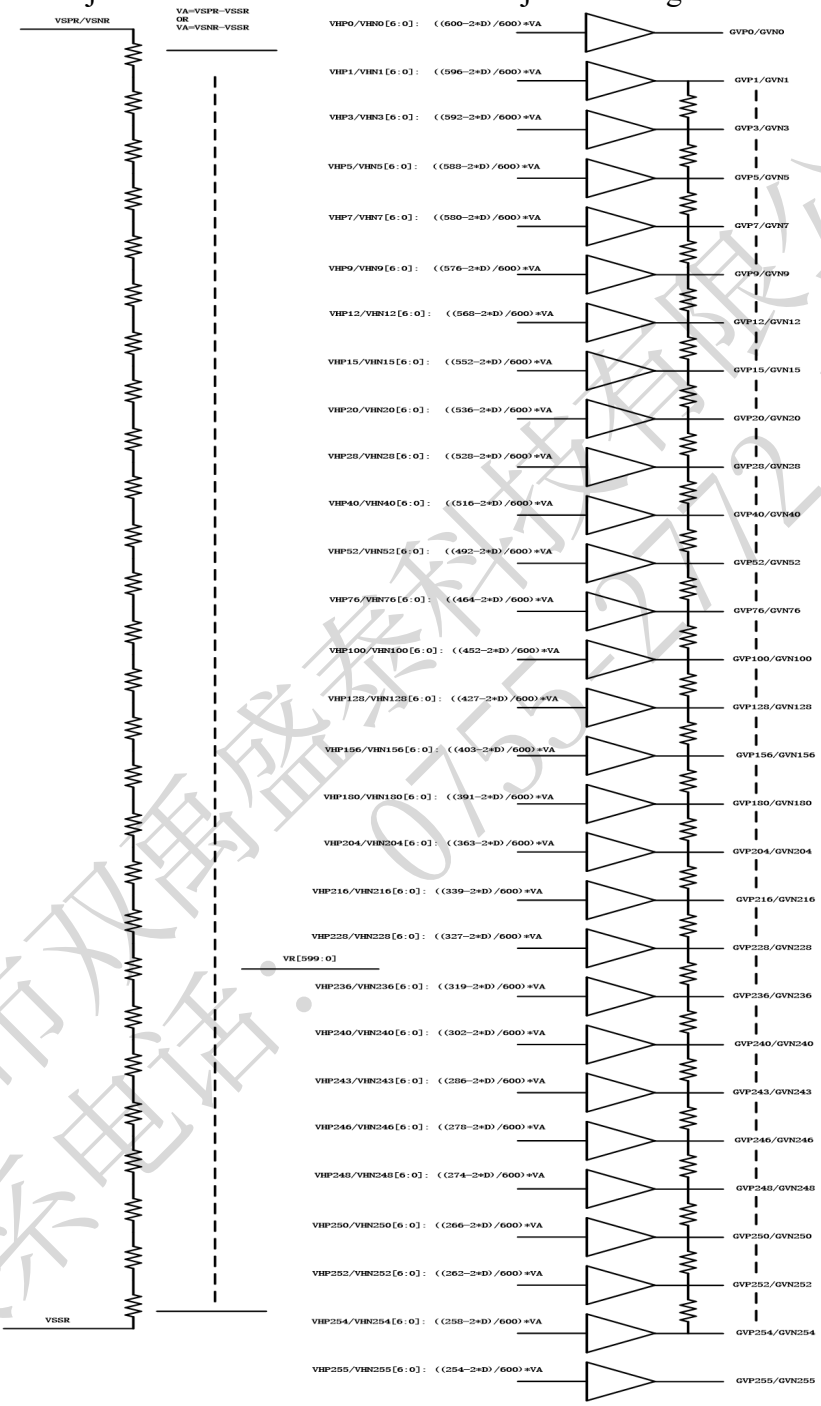
$$RTN = 1H(period) = \frac{Fosc - 5\%}{(Line + BP + FP) * FrameRate(Hz)}$$

$$RTN = 1H(period) = \frac{F_{pll} - 5\%}{(Line + BP + FP) * FrameRate(Hz)}(us)$$ (Note.1, Note.2, Note.3)

RTN: Number of clocks per line.
Line: Display Line Number
FP: Number of lines for the front porch.
BP: Number of lines for the back porch.
Note.1: The RTN formula can cover full temp range variation
Note.2: When Touch function ON (must take account of DP/TP ratio)
Note.3: For detailed RTN calculation method, please contact AXS.

5.10 Gamma Function

The structure of grayscale amplifier is shown as below. The 30 voltage levels between VSPR/VSNR and GND determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



Figure：Gamma Architecture for AXS15260

5.11 Reset Function

The RESET function of AXS15260 is triggered by a RESX input. After reset function triggered, the AXS15260 enter a reset period, and the duration of this period must be at least 5ms. During this period, the AXS15260 and its power circuit will be initialized.

Initial States of Output Pins

The following table represents the output pins and its initial state (2-power mode: VCI, VDDI).

Output Pins	Initial State
S<810:1>	GND
SX<480:1>	GND
VCOM	Disabled (GND level output)
GOUT_L[17:1], GOUT_R[17:1]	Disabled (GND level output)
LED_PWM	Disabled (GND level output)
VGH	Disabled
VGL	Disabled
VGHO	Disabled
VGLO	Disabled
VREF_TP	Disabled (Hi-z)
VCG_TP	Disabled (Hi-z)

5.12 Driver Operation Mode

AXS15260 driver can work in four operation modes of Reset State, Power Off state, Power On state and Display On State.

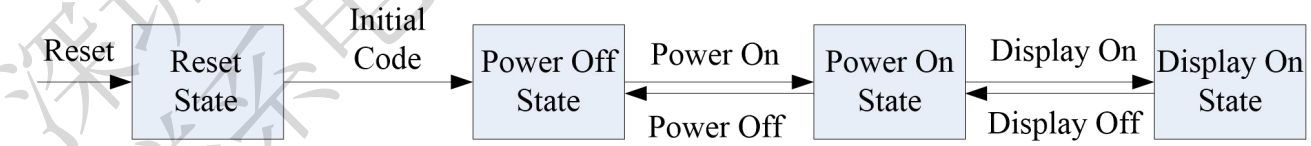
After reset, AXS15260 driver is in Reset state. In this state, all configurations are not initialized. Driver powers are not setup.

Initial code can be loaded from internal OTP or external flash or sent by host via MIPI interface. After the Initial code is loaded, AXS15260 driver enters Power Off state. AXS15260 driver is configured but powers are not up.

Power on command is sent from the Host. AXS15260 driver changes to Power On state on receiving power on command. All powers will be generated internally.

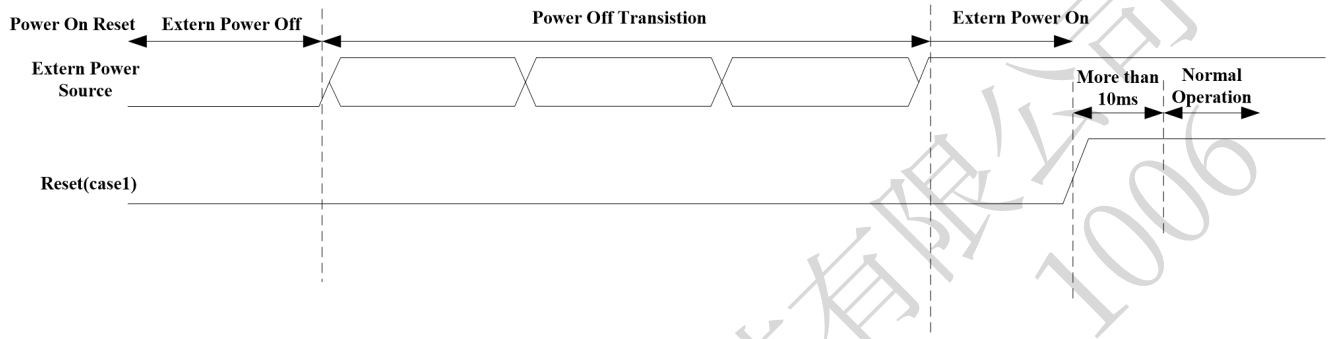
In Power on state, display on command can turn on the data path for display.

In Display on state, display off command can turn AXS15260 driver to Power On state and power off command can turn it to Power Off state.



5.12.1 Timing of Reset Pin

AXS15260 provides H/W pin to do driver IC initialization. For power-on reset, one-finger reset (Case1) methods can be applied to do driver IC initialization. The detailed H/W reset pin timing is shown as below.
Of the two methods, RESET(Case 2) is recommended.



H/W reset pin timing for power-on reset

5.13 Tear Effect Information

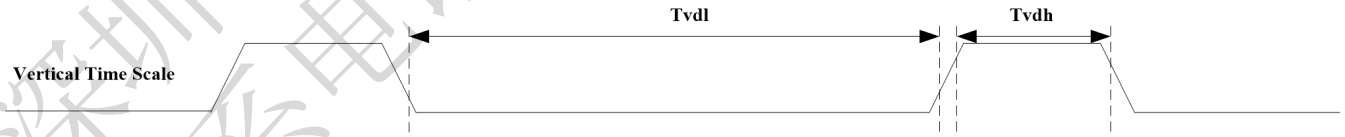
5.13.1 General

Tearing Effect line supplies to the MCU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command

5.13.2 Tearing effect line models

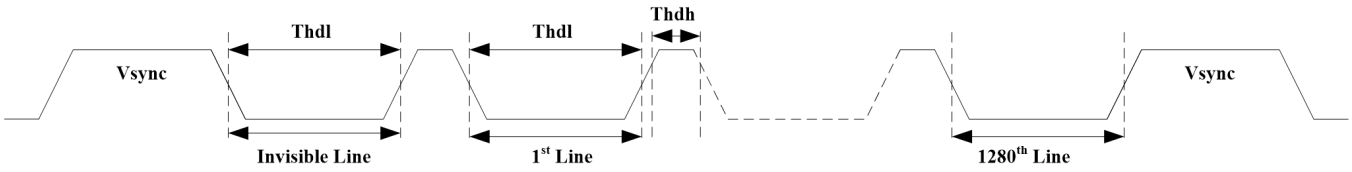
The Tearing Effect line supplies to the MCU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

Mode1：The Tearing Effect Output signal consists of V-Sync information only:



tvdh = The display panel is not updated from the Frame Memory.
tvdl = The display panel is updated from the Frame Memory (except Invisible Line – see below).

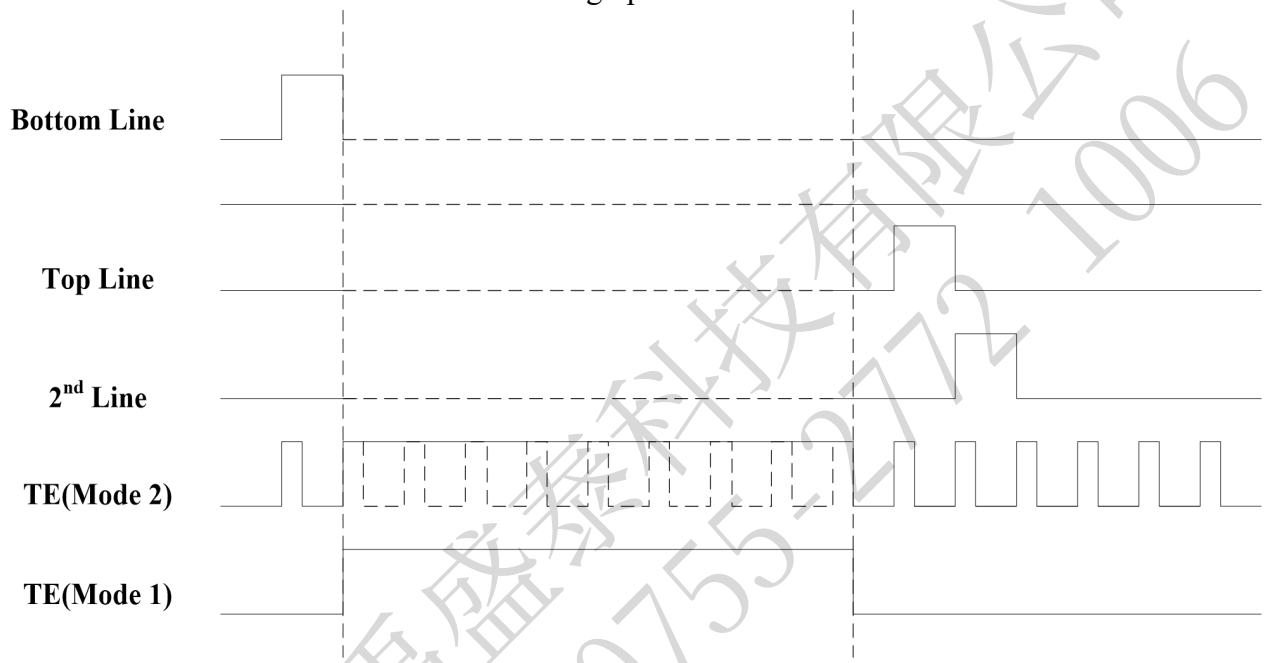
Mode 2： The Tearing Effect Output signal consists of V-Sync and H-Sync information; There is one V-sync and 4 H-sync pulses per field:



t_{vdh} = The display panel is not updated from the Frame Memory.

t_{vdl} = The display panel is updated from the Frame Memory (except Invisible Line – see below).

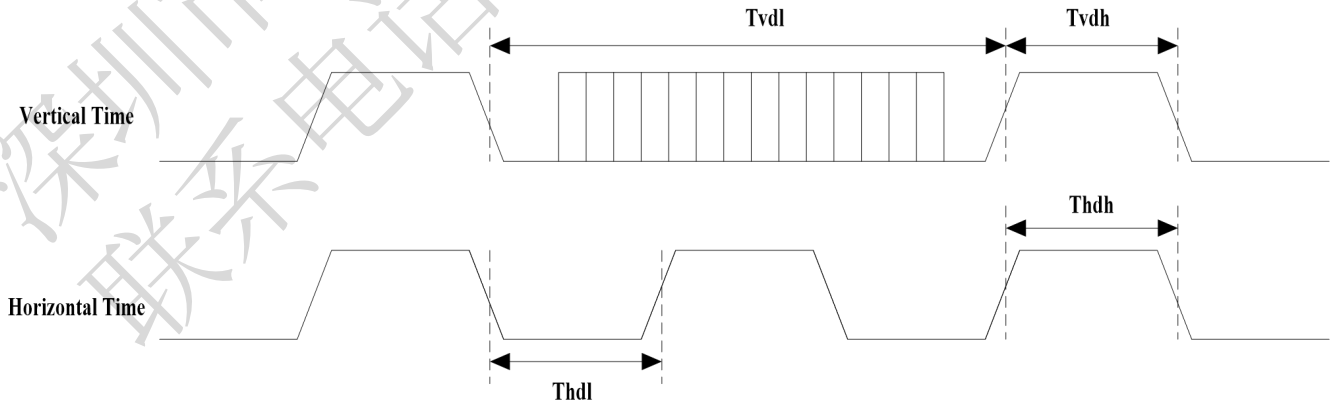
TE Line mode1 and Mode2 is shown as below graph:



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

5.13.2.1 Tearing effect line timing

The Tearing Effect signal is described below:

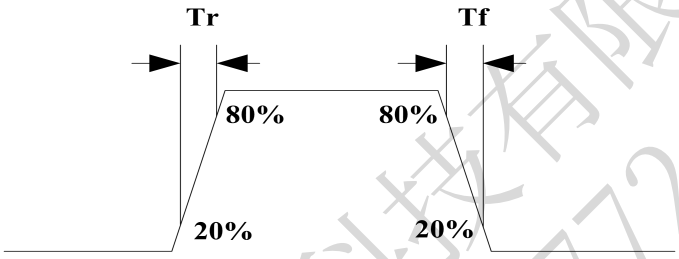


Symbol	Parameter	min	max	unit	description

tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	16	-	µs	
thdh	Horizontal Timing Low Duration	-	500	µs	

Idle Mode Off/On

The TE signal rising and falling timing is described below:



5.14 OTP Programming Procedure

5.14.1 Power function description

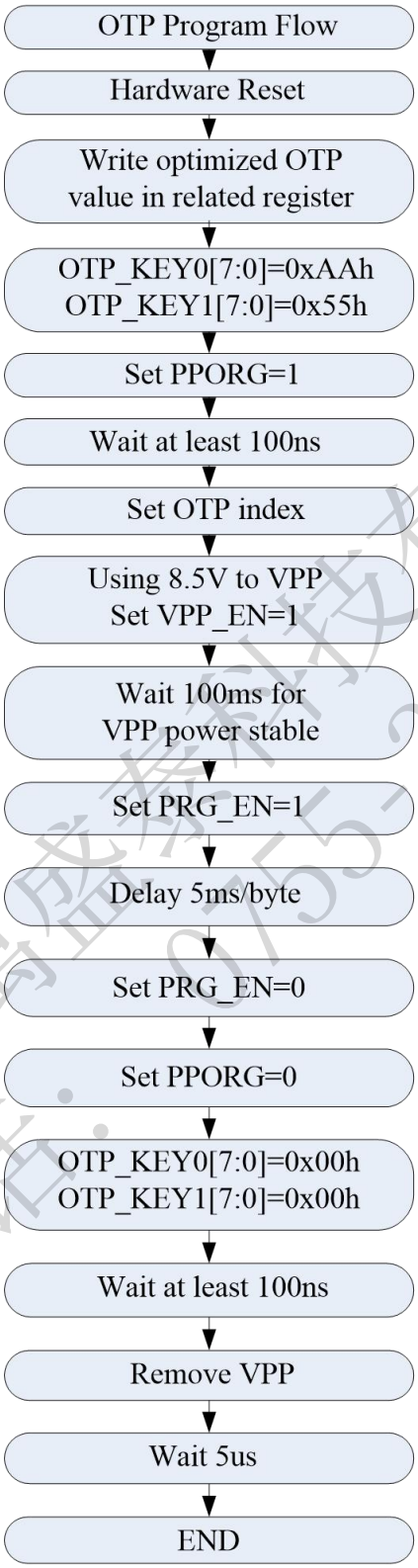
The OTP control signals control data reading and writing, only load once when reset. According to the request of the OTP, reset signal need delay at least 20ns to generate control signal. And signal transition should be less than 1ns.

STEP: Write the register parameters, then use index read all index, if both consistent, to write read content into the OTP. This method requires each register readout parameters contend is the same as written contend before. Each number of parameter is the same. And it may waste OTP resources if did not in byte. In order to prevent the wrong, the rest of resource as a reserve. The content behind can cover the front.

In the program, Write the index and parameters, matching read contend with register number, and loading the content behind in register.

In addition, you can also load OTP after reset release, and programming OTP by external interface generating timing.

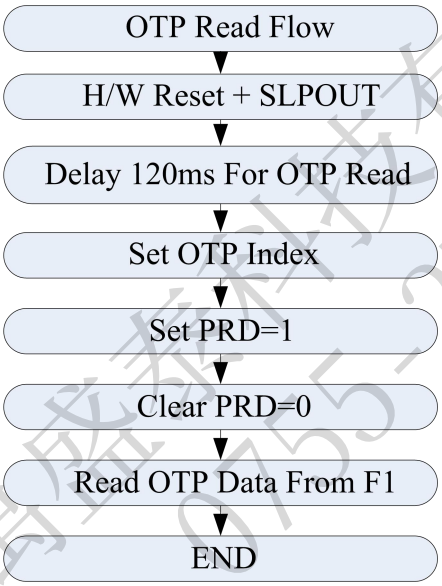
5.14.2 OTP program flow chart



Step	External Power OTP Program Sequence
1	Power on and reset the module
2	Write optimized OTP value in related register

3	OTP_KEY 0xAA 0x55
4	Set PPORG=1, wait 100ns
5	Set OTP index
6	Use 8.5V to VPP, Set VPP_EN=1, wait 100ms
7	Set PRG_EN=1, wait 5ms/byte
8	Set PRG_EN=0
9	Set PPORG=0, wait 100ns
10	OTP_KEY 0x00 0x00
11	Remove VPP, wait 5us

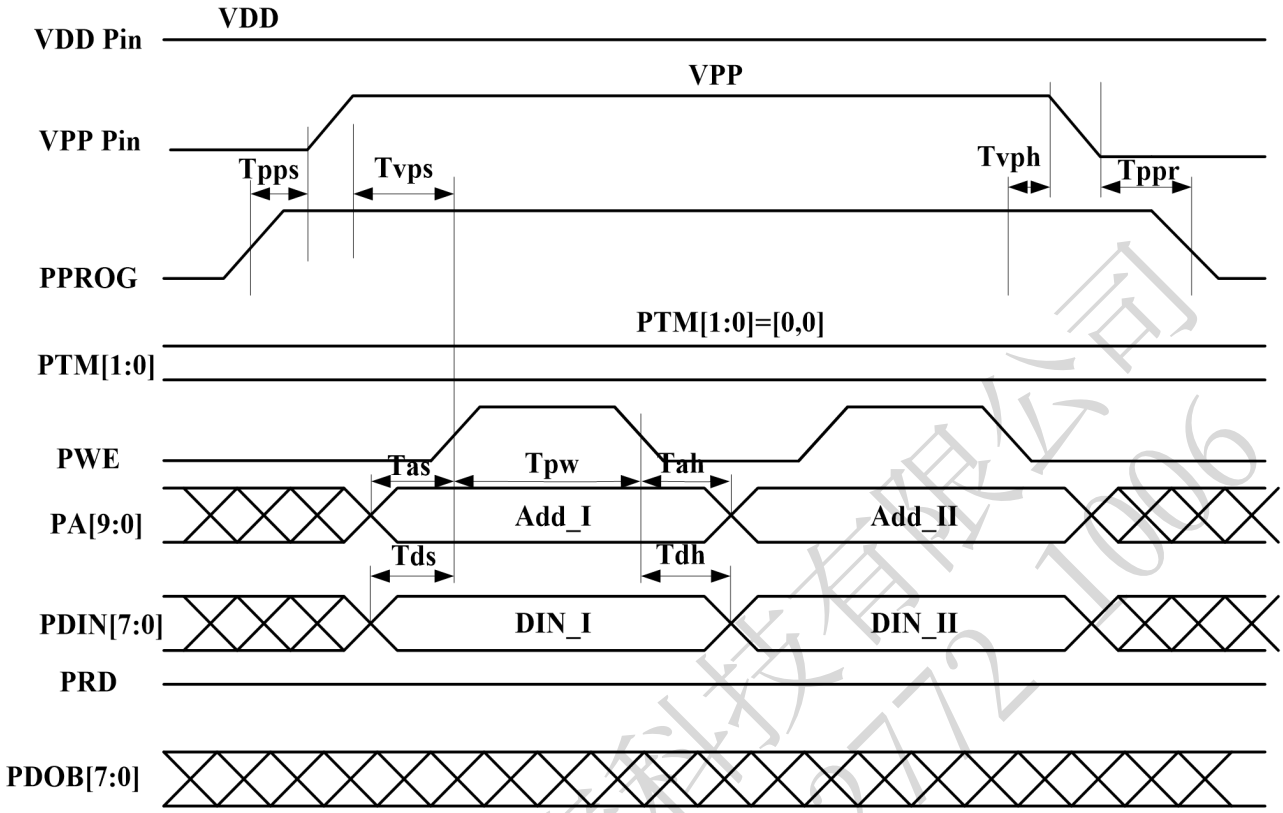
5.14.3 OTP read program flow chart with External Power



When testing, connect signal with the test port, then observe the contend.

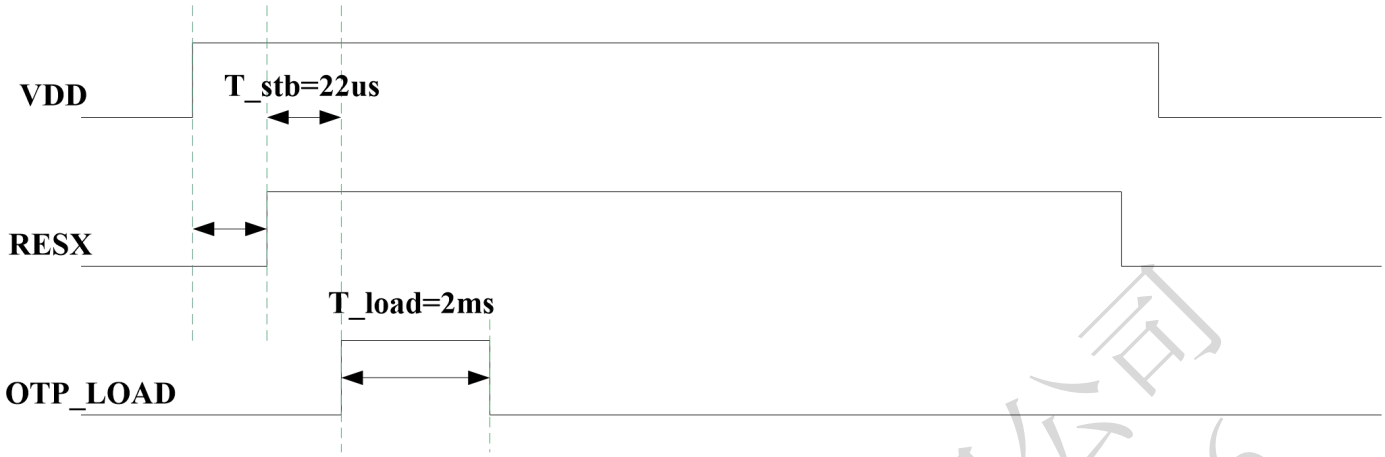
5.14.4 Timing description

Rogram timing：

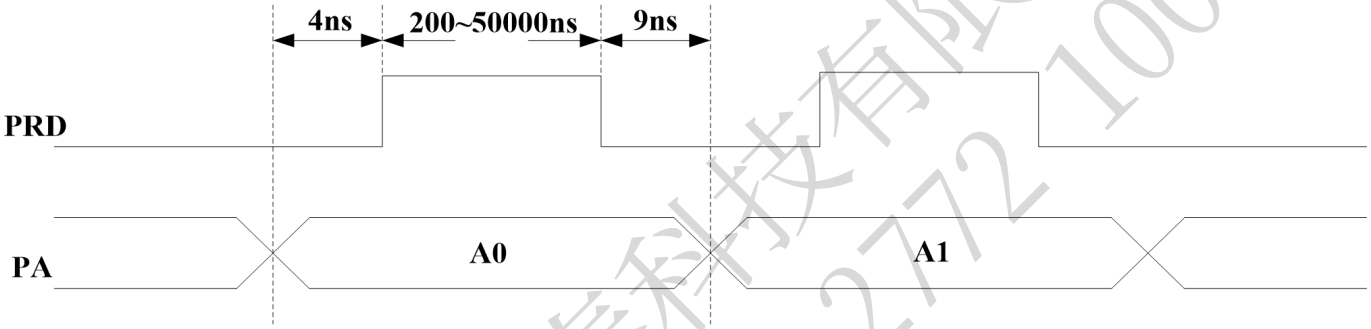


Parameter	Symbol	Min	Max	Unit
Address Setup Time	Tas	4	-	ns
Address Hold Time	Tah	9	-	ns
Data Setup Time	Tds	4	-	ns
Data Hold Time	Tdh	9	-	ns
Program Mode Setup Time	Tpps	10	-	ns
Program Mode Recovery Time	Tppr	10	-	ns
External VPP Setup Time	Tvps	0	-	ns
External VPP Hold Time	Tvph	0	-	ns
Program Pulse Width Time	Tpw	300	350	ns

load otp timing description, time is default value.



when read, tprd should set as short as possible:



5.15 BIST Function

The BIST (Build In Self Test) is used for inspection, fabrication process and reliability test without external interface operation. this function is controlled by A1 command.

The following BIST patterns are built in the AXS15260, every pattern and its definition number is also defined as follows:

Pattern0：Red
Cr_pat_sel[0]=1

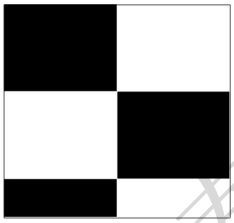
Pattern1：Green
Cr_pat_sel[1]=1

Pattern2：Blue
Cr_pat_sel[2]=1

Pattern3：White
Cr_pat_sel[3]=1

Pattern4：Black
Cr_pat_sel[4]=1

Pattern5：Chese
Cr_pat_sel[5]=1

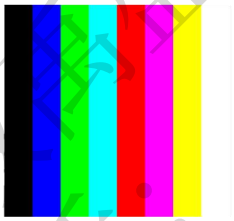


Pattern6：Mid gray
Cr_pat_sel[6]=1

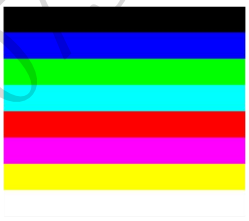
Pattern7：Gray col
Cr_pat_sel[7]=1

Pattern8：Gray row
Cr_pat_sel[1]=1

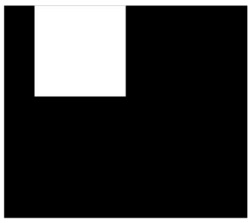
Pattern9：strp col
Cr_pat_sel[1]=1



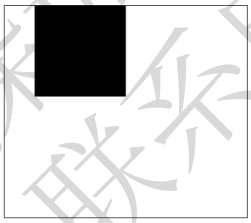
Pattern10：strp row
Cr_pat_sel[1]=1



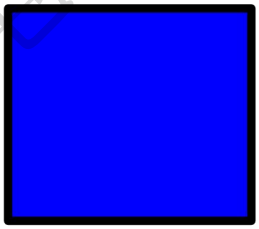
Pattern11：data partial
Cr_pat_sel[11]=1



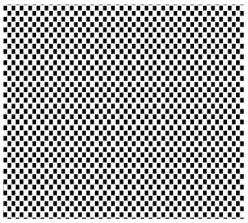
Pattern12：partial inverse
Cr_pat_sel[12]=1



Pattern13：Display rec
Cr_pat_sel[13]=1



Pattern14：data one
Cr_pat_sel[14]=1



Pattern15：crosstalk
Grayscale partial mode
Cr_pat_sel[15]=1

Note:
1.cr_bist_en_mode: Bist mode enable
2.cr_pat_sel: display pattern select
3.Pattern 6(Mid Gray): RGB value(gray_red,gray_g,gray_b)can be defined by the user;
The default color display blue(gray_red=gray_g=0,gray_b=8'h FF);

4.Pattern 13(Display rec):
RGB value (gray_red,gray_g, gray_b)can be defined by the user;
the default color display blue (gray_red=gray_g=0, gray_b=8'h FF);
but the whole picture will add a black border.

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Operation Range

VDDI：VDDI VDDI_TP VDDI_F VDDI_LDO VDDI_DRV VDDI_M

Item	Symbol	Min	Max	Unit
Supply Voltage(Analog)	VCI	-0.3	+7.8	V
Supply Voltage(Analog)	VSP	-0.3	+7.8	V
Supply Voltage(Analog)	VSN	-7.8	+0.3	V
Supply Voltage(I/O)	VDDI	-0.3	+4.0	V
Driver Supply Voltage	VGH-VGL	-0.3	+32	V
Logic Input Voltage Range	VIN	-0.3	VDDI+0.3	V
Logic Output Voltage Range	VO	-0.3	VDDI+0.3	V
Operating Temperature Range	TOPR	-30	+85	℃
Storage Temperature Range	TSTG	-40	+125	℃

6.2 Power Consumption

condition	Image	Current Consumption
MIPI：Dvr+TP(Normal work)	white	TBD
		TBD
MIPI：display without TP	white	TBD
		TBD
SPI 4Wire：display without TP	Yellow	TBD
TP(No Scan/No Display)	-	TBD
		TBD
Monitor	-	TBD
		TBD
		TBD

6.3 DC characteristic

6.3.1 Basic DC characteristic

(VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30ºC ~ 70ºC)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage（2power）	VCI	I/O supply voltage	-	3.3	-	V	
VSP charge pump（2power）	VSP	I/O supply voltage	4.7	5.9	6.3	V	
VSN charge pump（2power）	VSN	I/O supply voltage	-4.5	-5.6	-6.0	V	
Logic Operating voltage（1.8V）	VDDI	I/O supply voltage	-	1.8	-	V	
Logic Operating voltage（3.3V）	VDDI	I/O supply voltage	-	3.3	-	V	
VGH charge pump	VGHOUT1	-	12	15	16	V	
VGH charge pump	VGHOUT2	-	TBD	TBD	TBD	V	
VGL charge pump	VGLOUT1	-	-7.6	-10	-13	V	
VGL charge pump	VGLOUT2	-	TBD	TBD	TBD	V	
VCOM Operation							
VCOM voltage	VCOM	-	-2.5	-	0	V	0
Source Driver							
Source positive output range	Vsout	-	0.5	-	VSP-0.3	V	
Source negative output range	Vsout	-	-0.3	-	VSN+0.3	V	
Reference Voltage							
Internal reference voltage	VREF	-	-	1.8	-	V	
Current Consumption							
Sleep-IN mode(LP-11)	IIOVCC	RESX=High		TBD	TBD	uA	
	IVDD			TBD	TBD	uA	
Sleep-IN mode(ULPS)	IIOVCC	RESX=High		TBD	TBD	uA	
	IVDD			TBD	TBD	uA	

6.3.2 MIPI DC character

DC characteristics for MIPI-DSI

(VCI=3.0V~3.6V, IOVCC = 1.65V~3.6V, Ta = -30ºC ~ 70ºC)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	

Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDI_HS	-		1.8		V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	HS_VSS	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	VDDI_M	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VIHCD,MIN	-	450	-	HS_LDO	mV
Logic 0 contention threshold	VILCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	-	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedence	ZID	-	80	100	125	ohm

6.4 AC characteristic

6.4.1 Reset

The part of touch

POR（Power on Reset）Detect VCI, Vth=2.2V

External Reset: 0~VDDI

Soft reset

Host can issue reset instructions to reset the system

6.4.2 Serial interface characteristics (3-line SPI)

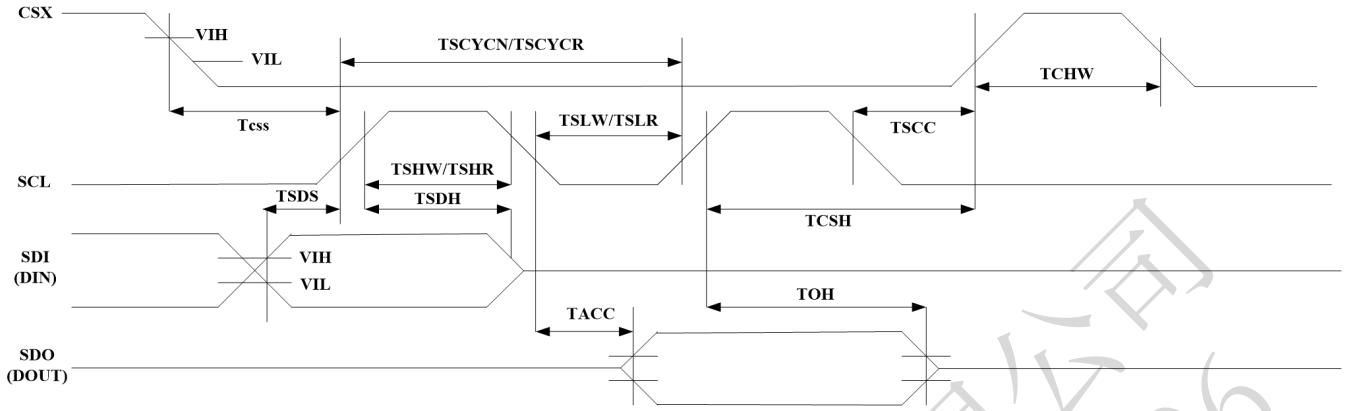


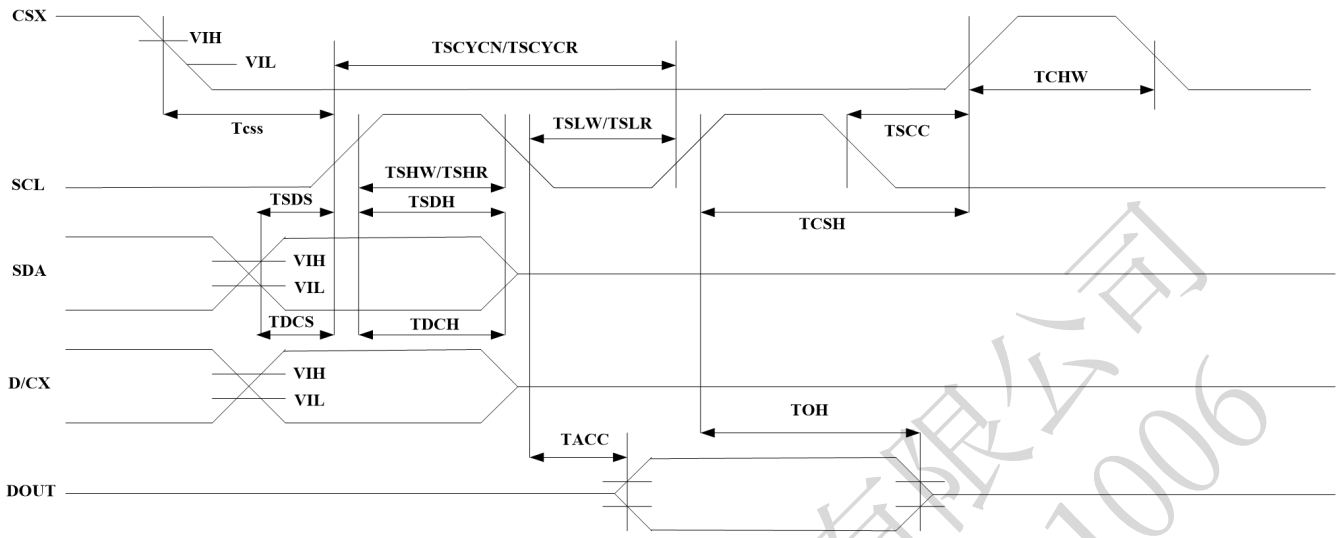
Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	TBD	TBD	ns	-
	TCSH	Chip select hold time	TBD	TBD	ns	-
	TSCC	Chip select setup time	TBD	TBD	ns	-
	TCHW	Chip select setup time	TBD	TBD	ns	-
SCL	TSCYCW	Serial clock cycle (Write)	TBD	TBD	ns	-
	TSHW	SCL “H” pulse width (Write)	TBD	TBD	ns	-
	TSLW	SCL “L” pulse width (Write)	TBD	TBD	ns	-
	TSCYCR	Serial clock cycle (Read)	TBD	TBD	ns	-
	TSHR	SCL “H” pulse width (Read)	TBD	TBD	ns	-
	TSLR	SCL “L” pulse width (Read)	TBD	TBD	ns	-
SDA (DIN) (DOUT)	TSDS	Data setup time	TBD	TBD	ns	-
	TSDH	Data hold time	TBD	TBD	ns	-
	TACC	Access time	TBD	TBD	ns	For maximum CL=30pF For minimum CL=8pF
	TOH	Output disable time	TBD	TBD	ns	

Note 1: VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30ºC ~ 70ºC.
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

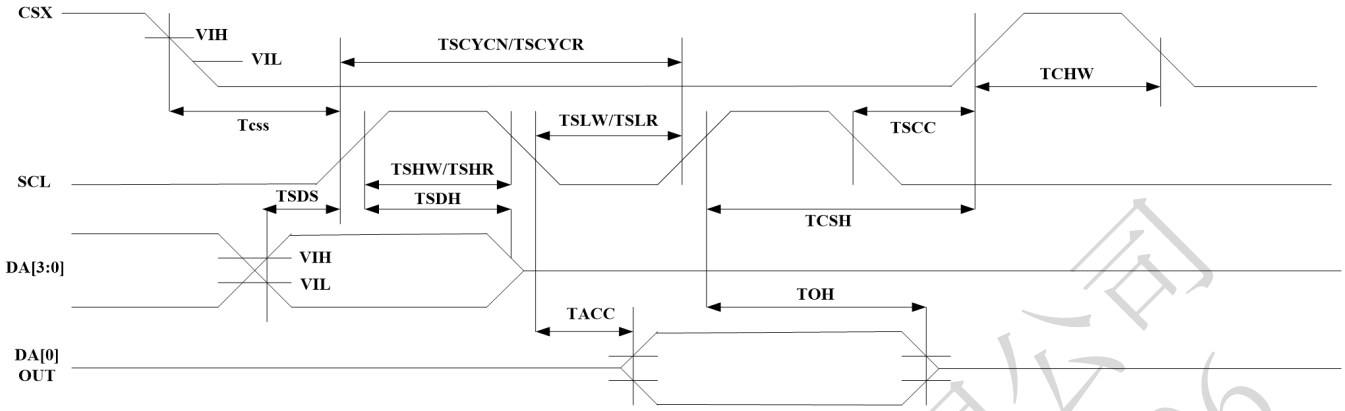
6.4.3 Serial interface characteristics (4-line SPI)



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	TBD	ns	
	T_{CSH}	Chip select hold time (write)	TBD	TBD	ns	
	T_{CSS}	Chip select setup time (read)	TBD	TBD	ns	
	T_{SCC}	Chip select hold time (read)	TBD	TBD	ns	
	T_{CHW}	Chip select “H” pulse width	TBD	TBD	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	TBD	ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	TBD	TBD	ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD	TBD	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	TBD	ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	TBD	TBD	ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD	TBD	ns	
D/CX	T_{DCS}	D/CX setup time	TBD	TBD	ns	
	T_{DCH}	D/CX hold time	TBD	TBD	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	TBD	ns	
	T_{SDH}	Data hold time	TBD	TBD	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Note 1: VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30°C ~ 70°C.
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.4.4 Quad Serial interface characteristics

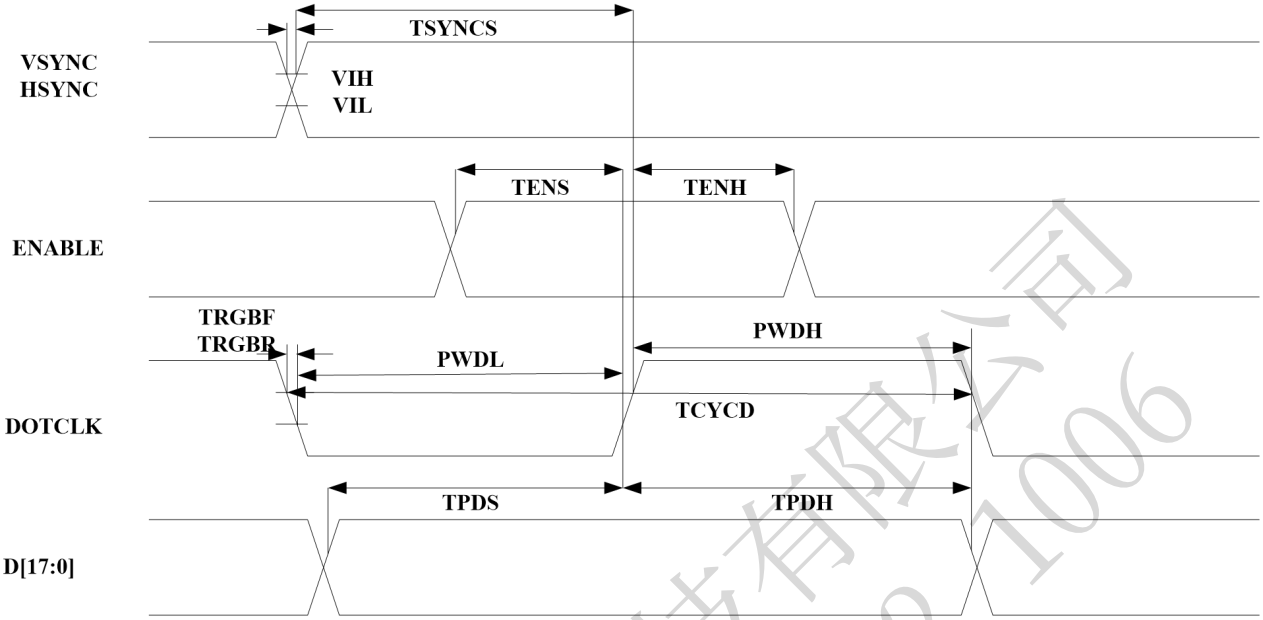


Quad SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD	TBD	ns	
	T_{CSH}	Chip select hold time (write)	TBD	TBD	ns	
	T_{CSS}	Chip select setup time (read)	TBD	TBD	ns	
	T_{SCC}	Chip select hold time (read)	TBD	TBD	ns	
	T_{CHW}	Chip select “H” pulse width	TBD	TBD	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD	TBD	ns	
	T_{SHW}	SCL “H” pulse width (Write)	TBD	TBD	ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD	TBD	ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD	TBD	ns	
	T_{SHR}	SCL “H” pulse width (Read)	TBD	TBD	ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD	TBD	ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD	TBD	ns	
	T_{SDH}	Data hold time	TBD	TBD	ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Note 1: VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30ºC ~ 70ºC.
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

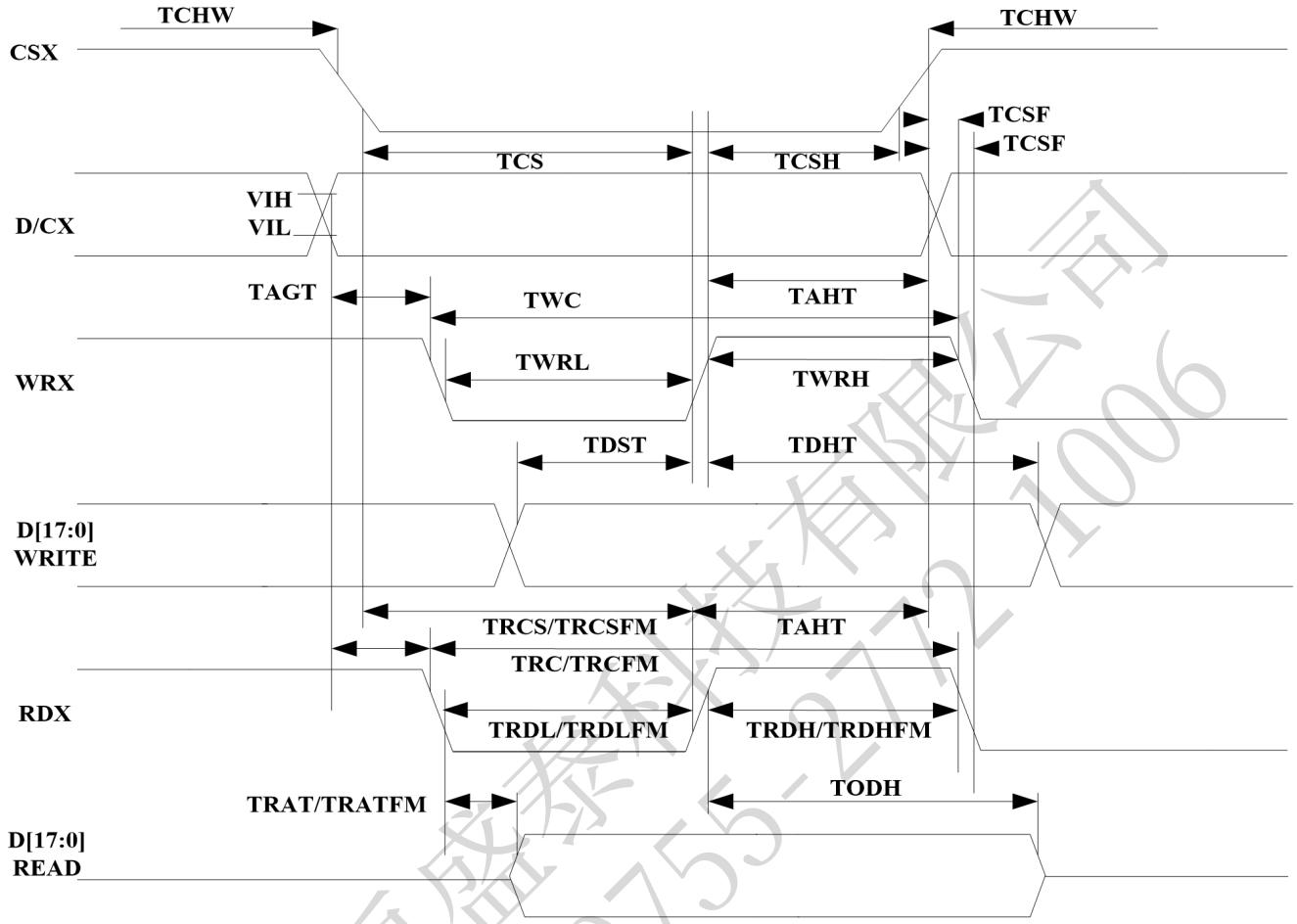
6.4.5 RGB interface characteristics



RGB Interface Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	TBD	TBD	ns	24/18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	TBD	TBD	ns	
DE	tens	DE setup time	TBD	TBD	ns	
	tenh	DE hold time	TBD	TBD	ns	
D[23:0]	tpds	Data setup time	TBD	TBD	ns	
	tpdh	Date hold time	TBD	TBD	ns	
DOTCLK	PWDH	DOTCLK high-level period	TBD	TBD	ns	
	PWDL	DOTCLK low-level period	TBD	TBD	ns	
	tcycd	DOTCLK cycle time	TBD	TBD	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	TBD	TBD	ns	

6.4.6 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



8080 Series Interface Characteristics

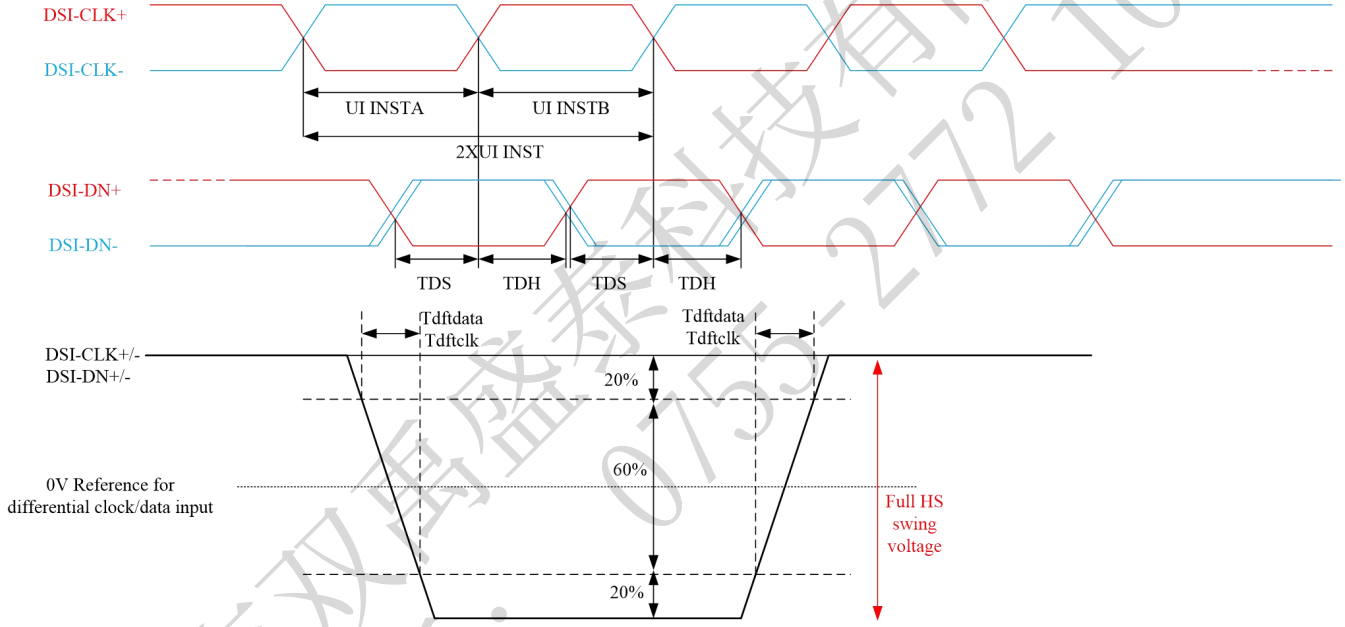
Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	TBD	TBD	ns	
	taht	Address hold time(Write/Read)	TBD	TBD	ns	
CSX	tchw	CSX "H" pulse width	TBD	TBD	ns	
	tcs	Chip Select setup time(Write)	TBD	TBD	ns	
	trcs	Chip Select setup time(Read ID)	TBD	TBD	ns	
	trcsfm	Chip Select setup time(Read FM)	TBD	TBD	ns	
	tcsf	Chip Select Wait time (Write/Read)	TBD	TBD	ns	
WRX	twc	Write Cycle	TBD	TBD	ns	
	twrh	Write Control pulse H duration	TBD	TBD	ns	
	twrl	Write Control pulse L duration	TBD	TBD	ns	
RDX(FM)	trcfm	Read Cycle (FM)	TBD	TBD	ns	
	trdhfm	Read Control H duration(FM)	TBD	TBD	ns	
	trdlfm	Read Control L duration(FM)	TBD	TBD	ns	
RDX(ID)	trc	Read Cycle (ID)	TBD	TBD	ns	
	trdh	Read Control pulse H duration	TBD	TBD	ns	

	trdl	Read Control pulse L duration	TBD	TBD	ns	
D[23:0]	tdst	Write data setup time	TBD	TBD	ns	For CL=30pF
	tdht	Write data hold time	TBD	TBD	ns	
	trat	Read access time	TBD	TBD	ns	
	tratfm	Read access time	TBD	TBD	ns	
	trod	Read output disable time	TBD	TBD	ns	

Note 1: VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30ºC ~ 70ºC.
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.4.7 MIPI-DSI characteristics

6.4.7.1 High speed mode



Parameter	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	1.6		25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	0.8		12.5	ns	$UI=UI_{INSTA}=UI_{INSTB}$
DSI-D0+/-	T_{DS}	Data to clock setup time	0.15	-		UI	
DSI-D0+/-	T_{DH}	Data to clock hold time	0.15	-		UI	

Figure: AC characteristics for MIPI-DSI High speed mode

6.4.7.2 Low power mode

Parameter	Symbol	Parameter	Specification	Unit

			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T LPXD	-	2XT LPXD	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to driver LP-00 by display module	5XT LPXD	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to driver LP-00 after turnaround request - MPU	4XT LPXD	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

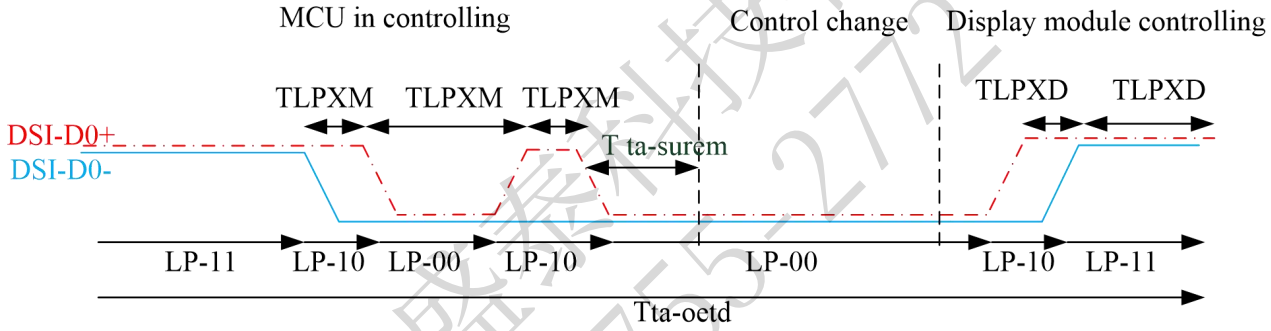


Figure: BTA from the MCU to the Display Module

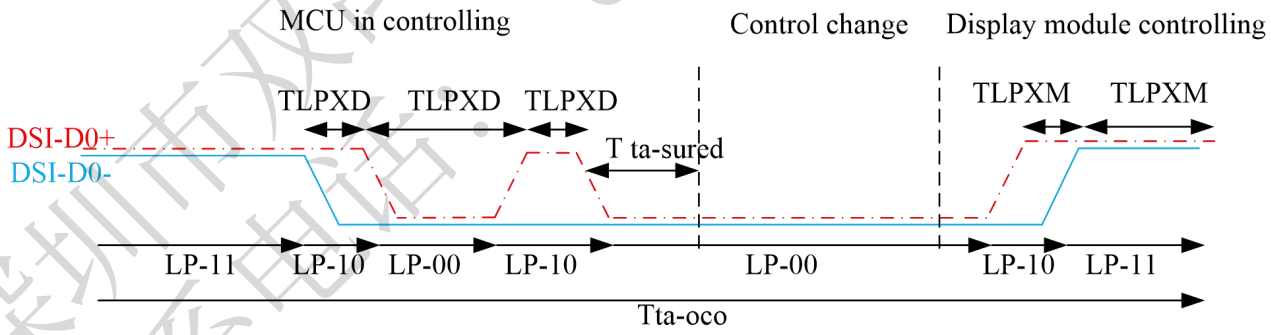


Figure: BTA from the Display Module to the MCU

6.4.7.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns

DSI-Dn+/-	$T_{HS-PREPARE}$	Time to driver LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to driver HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to driver flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ Period to start of LP-11 state	-	-	105ns +12UI	ns

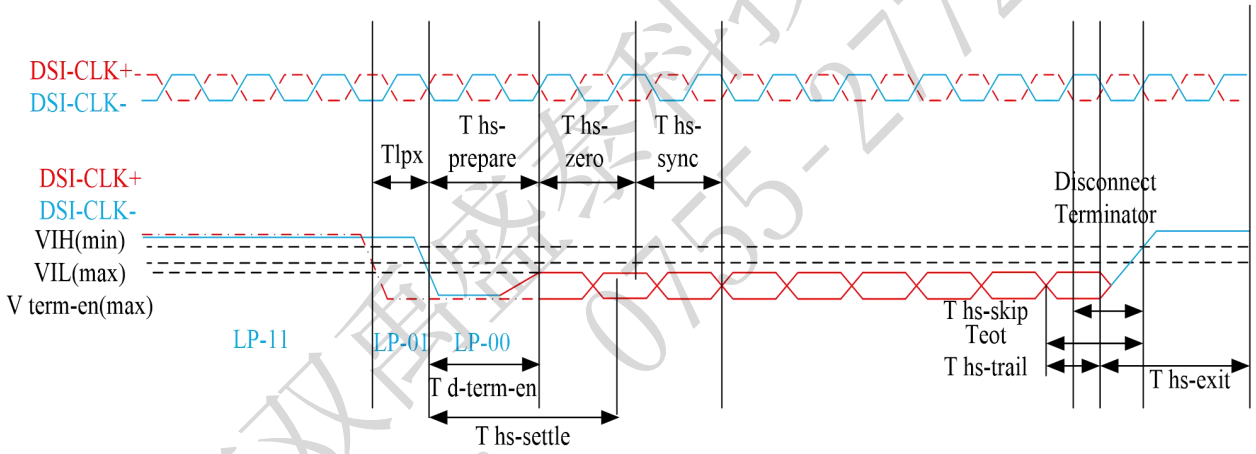


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lanehas transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be drivern prior to any associated Data Lanebeginning the transition from LP to HS mode	8	-	-	UI

DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to driver LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time for lead HS-0 driver period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to driver HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ periodto start of LP-11 state	-	-	105ns + 12UI	ns

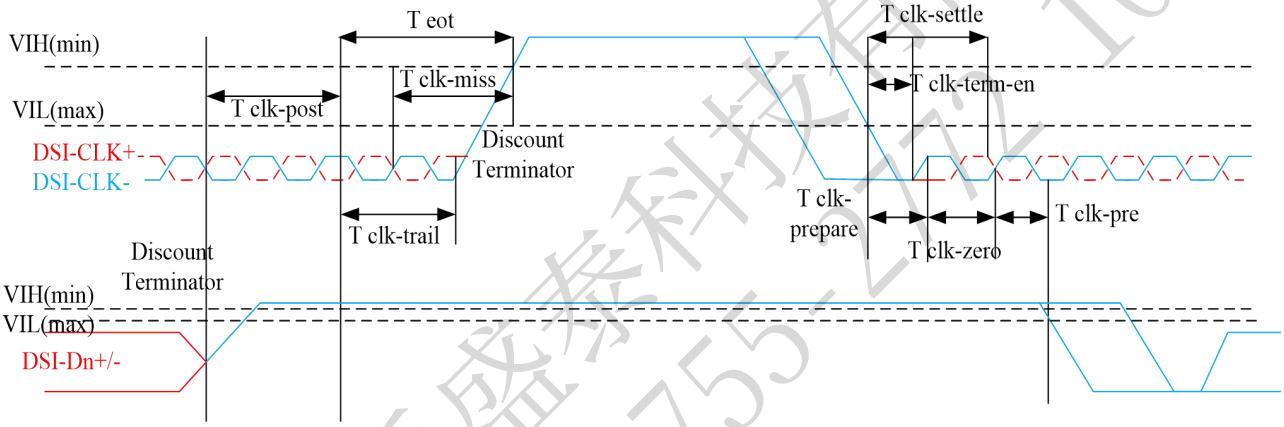


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

6.4.7.4 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when

different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-

BTA	100ns	-	100ns	-	100ns	-

7 Power Definition

7.1 Start-up time

The part of touch

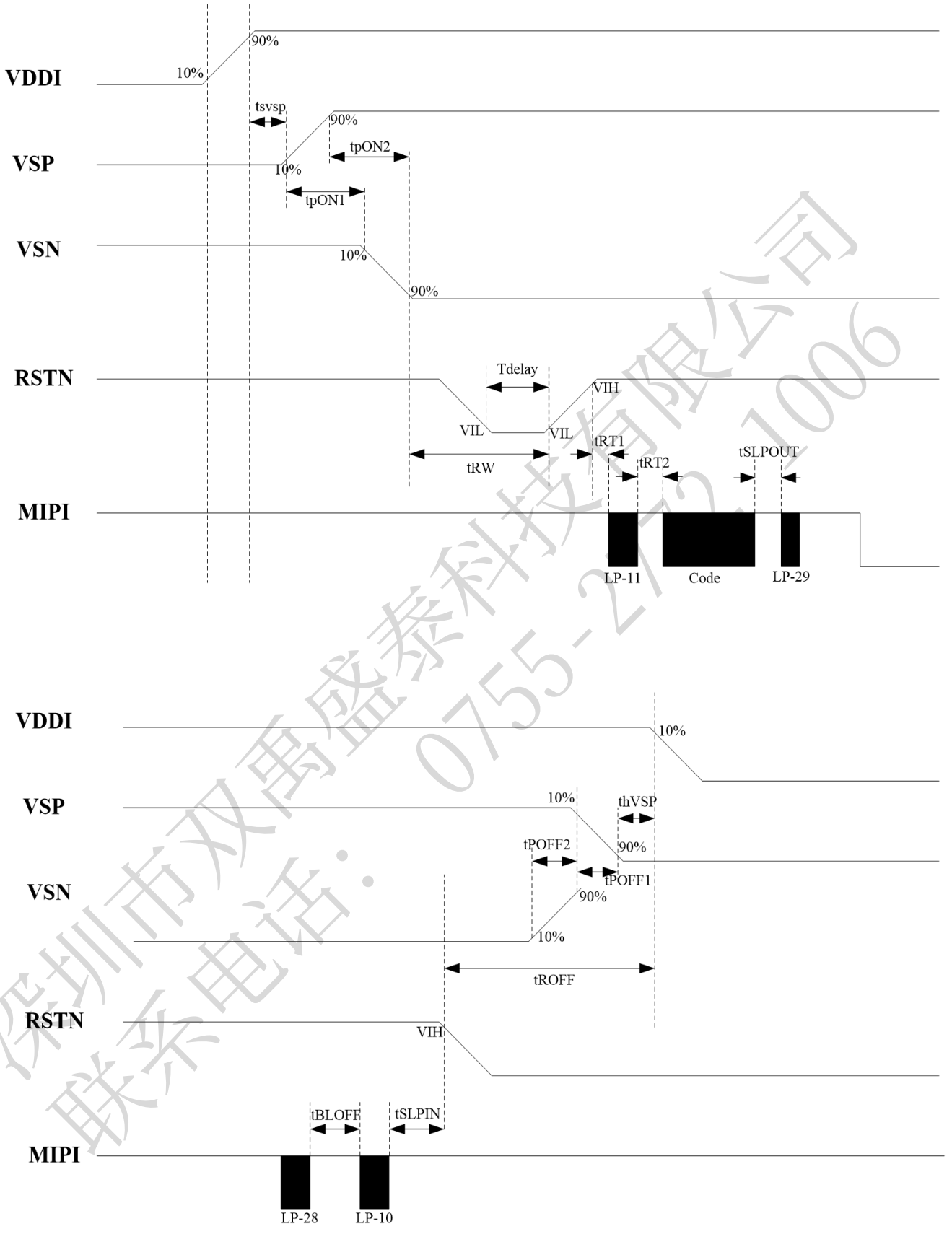
Power on：

Flash boot≤100mS

Wake up≤50ms

7.2 Power On/Off Sequence

The power on/off sequence is illustrated below:



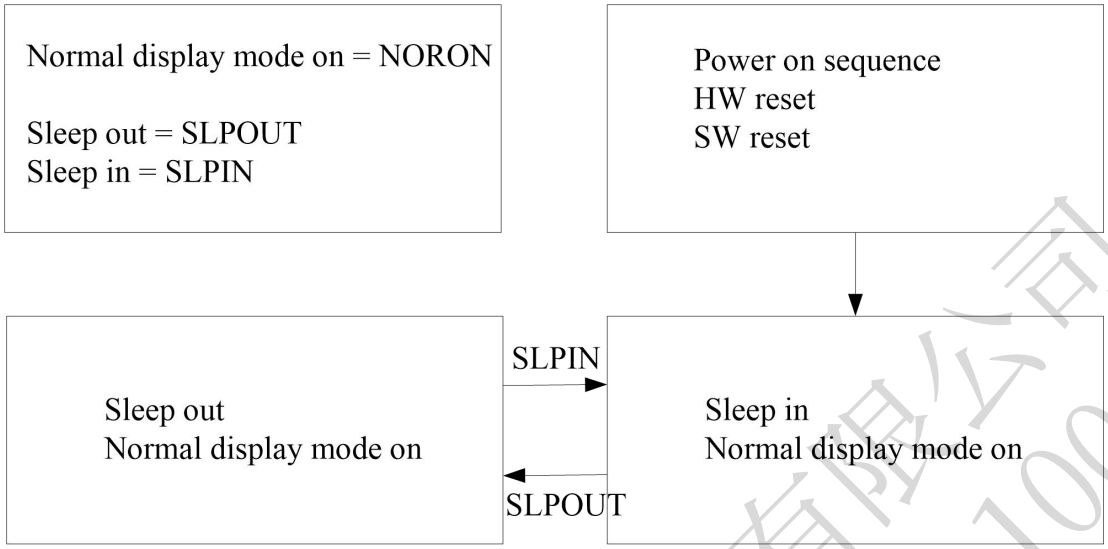
Description	Signal	Condition	Min	Unit

RST Hi-level (VIH) to LP_11 time	tRT1	Power On	160	ms
SLPOUT Sequence Request time	tSLPOUT	Power On	13.5	ms
VDDI On to VSP On time (90% to 10%)	ts_vsp	Power On	14.7	ms
VSP-VSN delay time （10%-10%）	tPON1	Power On	7.9	ms
VSP-VSN delay time （90%-90%）	tPON2	Power On	8	ms
All Power On to RSTN Hi-level time (90%-VIL)	tRW	Power On	28.7	ms
LP_11 to 1st Command time	tRT2	Power On	9.9	ms
RSTN delay time	Tdelay	Power On	10	ms
VSP-VSN delay time （90%-90%）	tPOFF2	Power Off	8.77	ms
VSP-VSN delay time （10%-10%）	tPOFF1	Power Off	3.4	ms
VSP Off to VDDI Off time （10%-90%）	thVSP	Power Off	8.84	ms
RSTN Low to VDDI Off time (VIH to 90%)	tROFF	Power Off	167	ms
SLPIN Sequence Request time	tSLPIN	Power Off	140	ms
LP_28 to LP_10 delay time	tBLOFF	Power Off	9.9	ms

7.2.1 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damage for the display module or the display module will not cause any damage to the host or lines of the interface. At an uncontrolled power off event, the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7.3 Power flow chart

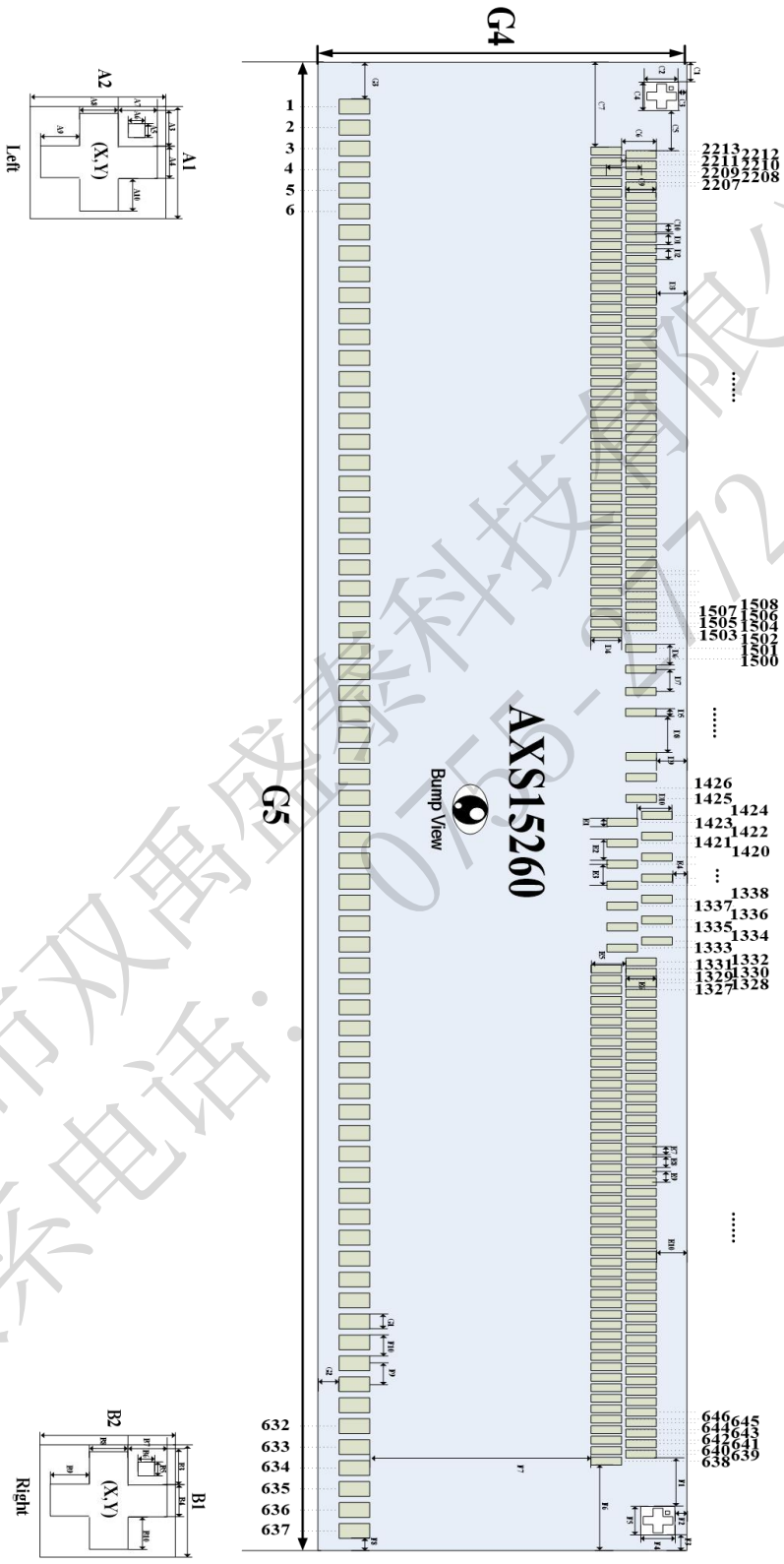


Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

8 CHIP IMFORMATION

8.1 PAD Assignment



Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size
A1	80	A2	80	A3	15	A4	20	A5	10
A6	10	A7	15	A8	20	A9	15	A10	15
B1	80	B2	80	B3	15	B4	20	B5	10
B6	10	B7	15	B8	20	B9	15	B10	15
C1	50	C2	80	C3	50	C4	80	C5	263．69
C6	100	C7	381．69	C8	100	C9	75	C10	14
D1	24/23.99	D2	24/23.99	D3	81.28	D4	75	D5	14
D6	47.98/47.99	D7	47.98/47.99	D8	333.92	D9	81.28	D10	100
E1	14	E2	71.99/71.98	E3	71.99/71.98	E4	35.28	E5	100
E6	75	E7	14	E8	24/23.99	E9	24/23.99	E10	81.28
F1	251.69	F2	50	F3	50	F4	80	F5	80
F6	393.69	F7	441.22	F8	88.76	F9	38.99/39	F10	38.99/39
G1	24	G2	47.5	G3	88.76	G4	820	G5	25000
								Unit=um	

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	25000	820	um
Chip thickness	-	200		
Pad Size	1 - 637	24	75	
	638 - 1332	14	75	
	1333 - 1424	14	75	
	1425 - 1463	14	75	
	1464 - 1502	14	75	
	1503 - 2213	14	75	
Pad Pitch	1 - 637	38.99/39	-	
	638 - 1332	11.99/12	100	
	1333 - 1424	11.99/12	100	
	1425 - 1463	23.99/24	-	
	1464 - 1502	23.99/24	-	
	1503 - 2213	11.99/12	100	

Note1: Have Temperature compensation design.

8.2 PAD CENTER COORDINATE

PAD NO	PAD name	X	Y
1	VGLOUT1	-12399.24	-325
2	VGLOUT1	-12360.25	-325
3	VGL	-12321.26	-325
4	VGL	-12282.27	-325
5	VGLOUT2	-12243.28	-325
6	VGLOUT2	-12204.29	-325
7	VPP	-12165.3	-325
8	VPP	-12126.3	-325
9	VDDA_OTP	-12087.31	-325
10	VDDA_OTP	-12048.32	-325
11	OTP_EXT_EN	-12009.33	-325
12	VCOM_PASS_L	-11970.34	-325
13	VSN	-11931.35	-325
14	VSN	-11892.36	-325
15	VSP	-11853.37	-325
16	VSP	-11814.37	-325
17	VSSA	-11775.38	-325
18	VSSA	-11736.39	-325
19	VSSA	-11697.4	-325
20	VGLO_L	-11658.41	-325
21	VGLO_L	-11619.42	-325
22	VGLO_L	-11580.43	-325
23	VGLO_L	-11541.43	-325
24	VGLO_L	-11502.44	-325
25	VGH_L	-11463.45	-325
26	VGH_L	-11424.46	-325
27	VGH_L	-11385.47	-325
28	VGH_L	-11346.48	-325
29	VGH_L	-11307.49	-325
30	VGHO_L	-11268.5	-325
31	VGHO_L	-11229.5	-325
32	VGHO_L	-11190.51	-325
33	VGHO_L	-11151.52	-325
34	VGHO_L	-11112.53	-325
35	CGOUT_L<1>	-11073.54	-325
36	CGOUT_L<2>	-11034.55	-325
37	CGOUT_L<3>	-10995.56	-325
38	CGOUT_L<4>	-10956.56	-325
39	CGOUT_L<5>	-10917.57	-325
40	CGOUT_L<6>	-10878.58	-325
41	CGOUT_L<7>	-10839.59	-325
42	CGOUT_L<8>	-10800.6	-325
43	CGOUT_L<9>	-10761.61	-325

PAD NO	PAD name	X	Y
1108	VSSA	6472.56	291.22
1109	VSSA	6460.56	191.22
1110	VSSA	6448.57	291.22
1111	VSSA	6436.57	191.22
1112	VSSA	6424.57	291.22
1113	SX<320>	6412.57	191.22
1114	S<540>	6400.58	291.22
1115	S<539>	6388.58	191.22
1116	VSSA	6376.58	291.22
1117	S<538>	6364.59	191.22
1118	SX<319>	6352.59	291.22
1119	S<537>	6340.59	191.22
1120	S<536>	6328.59	291.22
1121	VSSA	6316.6	191.22
1122	S<535>	6304.6	291.22
1123	SX<318>	6292.6	191.22
1124	S<534>	6280.6	291.22
1125	S<533>	6268.61	191.22
1126	VSSA	6256.61	291.22
1127	S<532>	6244.61	191.22
1128	SX<317>	6232.61	291.22
1129	S<531>	6220.62	191.22
1130	S<530>	6208.62	291.22
1131	VSSA	6196.62	191.22
1132	S<529>	6184.63	291.22
1133	SX<316>	6172.63	191.22
1134	S<528>	6160.63	291.22
1135	S<527>	6148.63	191.22
1136	SX<315>	6136.64	291.22
1137	S<526>	6124.64	191.22
1138	SX<314>	6112.64	291.22
1139	S<525>	6100.64	191.22
1140	S<524>	6088.65	291.22
1141	SX<313>	6076.65	191.22
1142	S<523>	6064.65	291.22
1143	SX<312>	6052.65	191.22
1144	S<522>	6040.66	291.22
1145	S<521>	6028.66	191.22
1146	SX<311>	6016.66	291.22
1147	S<520>	6004.67	191.22
1148	SX<310>	5992.67	291.22
1149	S<519>	5980.67	191.22
1150	S<518>	5968.67	291.22

44	CGOUT_L<10>	-10722.62	-325
45	CGOUT_L<11>	-10683.63	-325
46	CGOUT_L<12>	-10644.63	-325
47	CGOUT_L<13>	-10605.64	-325
48	CGOUT_L<14>	-10566.65	-325
49	CGOUT_L<15>	-10527.66	-325
50	CGOUT_L<16>	-10488.67	-325
51	CGOUT_L<17>	-10449.68	-325
52	VSSD	-10410.69	-325
53	VSSD	-10371.69	-325
54	VSSD	-10332.7	-325
55	VDD	-10293.71	-325
56	VDD	-10254.72	-325
57	VDD	-10215.73	-325
58	VDD_HS	-10176.74	-325
59	VDD_HS	-10137.75	-325
60	VDD_HS	-10098.76	-325
61	VDD_HS	-10059.76	-325
62	VDDI_HS	-10020.77	-325
63	VDDI_HS	-9981.78	-325
64	VDDI_HS	-9942.79	-325
65	VDDI_HS	-9903.8	-325
66	HS_LDO	-9864.81	-325
67	HS_LDO	-9825.82	-325
68	HS_LDO	-9786.82	-325
69	HS_LDO	-9747.83	-325
70	VSS_HS	-9708.84	-325
71	VSS_HS	-9669.85	-325
72	VSS_HS	-9630.86	-325
73	VSS_HS	-9591.87	-325
74	HS_D3P	-9552.88	-325
75	HS_D3P	-9513.89	-325
76	HS_D3P	-9474.89	-325
77	HS_D3P	-9435.9	-325
78	HS_D3N	-9396.91	-325
79	HS_D3N	-9357.92	-325
80	HS_D3N	-9318.93	-325
81	HS_D3N	-9279.94	-325
82	VSS_HS	-9240.95	-325
83	VSS_HS	-9201.95	-325
84	HS_D0P	-9162.96	-325
85	HS_D0P	-9123.97	-325
86	HS_D0P	-9084.98	-325
87	HS_D0P	-9045.99	-325
88	HS_D0N	-9007	-325
89	HS_D0N	-8968.01	-325

1151	SX<309>	5956.68	191.22
1152	S<517>	5944.68	291.22
1153	SX<308>	5932.68	191.22
1154	S<516>	5920.68	291.22
1155	S<515>	5908.69	191.22
1156	SX<307>	5896.69	291.22
1157	S<514>	5884.69	191.22
1158	SX<306>	5872.69	291.22
1159	S<513>	5860.7	191.22
1160	S<512>	5848.7	291.22
1161	SX<305>	5836.7	191.22
1162	S<511>	5824.71	291.22
1163	SX<304>	5812.71	191.22
1164	S<510>	5800.71	291.22
1165	S<509>	5788.71	191.22
1166	SX<303>	5776.72	291.22
1167	S<508>	5764.72	191.22
1168	SX<302>	5752.72	291.22
1169	S<507>	5740.72	191.22
1170	S<506>	5728.73	291.22
1171	SX<301>	5716.73	191.22
1172	S<505>	5704.73	291.22
1173	SX<300>	5692.73	191.22
1174	S<504>	5680.74	291.22
1175	S<503>	5668.74	191.22
1176	SX<299>	5656.74	291.22
1177	S<502>	5644.75	191.22
1178	SX<298>	5632.75	291.22
1179	S<501>	5620.75	191.22
1180	S<500>	5608.75	291.22
1181	SX<297>	5596.76	191.22
1182	S<499>	5584.76	291.22
1183	SX<296>	5572.76	191.22
1184	S<498>	5560.76	291.22
1185	S<497>	5548.77	191.22
1186	SX<295>	5536.77	291.22
1187	S<496>	5524.77	191.22
1188	SX<294>	5512.77	291.22
1189	S<495>	5500.78	191.22
1190	S<494>	5488.78	291.22
1191	SX<293>	5476.78	191.22
1192	S<493>	5464.79	291.22
1193	SX<292>	5452.79	191.22
1194	S<492>	5440.79	291.22
1195	S<491>	5428.79	191.22
1196	SX<291>	5416.8	291.22

90	HS_D0N	-8929.02	-325
91	HS_D0N	-8890.02	-325
92	VSS_HS	-8851.03	-325
93	VSS_HS	-8812.04	-325
94	HS_CP	-8773.05	-325
95	HS_CP	-8734.06	-325
96	HS_CP	-8695.07	-325
97	HS_CP	-8656.08	-325
98	HS_CN	-8617.08	-325
99	HS_CN	-8578.09	-325
100	HS_CN	-8539.1	-325
101	HS_CN	-8500.11	-325
102	VSS_HS	-8461.12	-325
103	VSS_HS	-8422.13	-325
104	HS_D1P	-8383.14	-325
105	HS_D1P	-8344.15	-325
106	HS_D1P	-8305.15	-325
107	HS_D1P	-8266.16	-325
108	HS_D1N	-8227.17	-325
109	HS_D1N	-8188.18	-325
110	HS_D1N	-8149.19	-325
111	HS_D1N	-8110.2	-325
112	VSS_HS	-8071.21	-325
113	VSS_HS	-8032.21	-325
114	HS_D2P	-7993.22	-325
115	HS_D2P	-7954.23	-325
116	HS_D2P	-7915.24	-325
117	HS_D2P	-7876.25	-325
118	HS_D2N	-7837.26	-325
119	HS_D2N	-7798.27	-325
120	HS_D2N	-7759.28	-325
121	HS_D2N	-7720.28	-325
122	VSS_HS	-7681.29	-325
123	VSS_HS	-7642.3	-325
124	VSS_HS	-7603.31	-325
125	VSS_HS	-7564.32	-325
126	HS_LDO	-7525.33	-325
127	HS_LDO	-7486.34	-325
128	HS_LDO	-7447.34	-325
129	HS_LDO	-7408.35	-325
130	VCG_TP	-7369.36	-325
131	VCG_TP	-7330.37	-325
132	VREF_TP	-7291.38	-325
133	VREF_TP	-7252.39	-325
134	VCOM	-7213.4	-325
135	VCOM	-7174.41	-325

1197	S<490>	5404.8	191.22
1198	SX<290>	5392.8	291.22
1199	S<489>	5380.8	191.22
1200	S<488>	5368.81	291.22
1201	SX<289>	5356.81	191.22
1202	S<487>	5344.81	291.22
1203	SX<288>	5332.81	191.22
1204	S<486>	5320.82	291.22
1205	S<485>	5308.82	191.22
1206	VSSA	5296.82	291.22
1207	S<484>	5284.83	191.22
1208	SX<287>	5272.83	291.22
1209	S<483>	5260.83	191.22
1210	S<482>	5248.83	291.22
1211	VSSA	5236.84	191.22
1212	S<481>	5224.84	291.22
1213	SX<286>	5212.84	191.22
1214	S<480>	5200.84	291.22
1215	S<479>	5188.85	191.22
1216	VSSA	5176.85	291.22
1217	S<478>	5164.85	191.22
1218	SX<285>	5152.85	291.22
1219	S<477>	5140.86	191.22
1220	S<476>	5128.86	291.22
1221	VSSA	5116.86	191.22
1222	S<475>	5104.87	291.22
1223	SX<284>	5092.87	191.22
1224	S<474>	5080.87	291.22
1225	S<473>	5068.87	191.22
1226	SX<283>	5056.88	291.22
1227	S<472>	5044.88	191.22
1228	SX<282>	5032.88	291.22
1229	S<471>	5020.88	191.22
1230	S<470>	5008.89	291.22
1231	SX<281>	4996.89	191.22
1232	S<469>	4984.89	291.22
1233	SX<280>	4972.89	191.22
1234	S<468>	4960.9	291.22
1235	S<467>	4948.9	191.22
1236	SX<279>	4936.9	291.22
1237	S<466>	4924.91	191.22
1238	SX<278>	4912.91	291.22
1239	S<465>	4900.91	191.22
1240	S<464>	4888.91	291.22
1241	SX<277>	4876.92	191.22
1242	S<463>	4864.92	291.22

136	ATEST0_NV	-7135.41	-325
137	VCL	-7096.42	-325
138	VCL	-7057.43	-325
139	VSN	-7018.44	-325
140	VSN	-6979.45	-325
141	VSN	-6940.46	-325
142	VDN	-6901.47	-325
143	VDN	-6862.47	-325
144	VDN	-6823.48	-325
145	VSSA	-6784.49	-325
146	VSSA	-6745.5	-325
147	VSSA	-6706.51	-325
148	VSP	-6667.52	-325
149	VSP	-6628.53	-325
150	VSP	-6589.54	-325
151	ATEST1_PV	-6550.54	-325
152	ATEST2_LV	-6511.55	-325
153	VDD_TP	-6472.56	-325
154	VDD_TP	-6433.57	-325
155	VDD	-6394.58	-325
156	VDD	-6355.59	-325
157	VDD	-6316.6	-325
158	VDD	-6277.6	-325
159	VSSD	-6238.61	-325
160	VSSD	-6199.62	-325
161	VSSD	-6160.63	-325
162	VSSD	-6121.64	-325
163	VDDI_DRV	-6082.65	-325
164	VDDI_DRV	-6043.66	-325
165	DB<23>	-6004.67	-325
166	DB<23>	-5965.67	-325
167	DB<22>	-5926.68	-325
168	DB<22>	-5887.69	-325
169	DB<21>	-5848.7	-325
170	DB<21>	-5809.71	-325
171	DB<20>	-5770.72	-325
172	DB<20>	-5731.73	-325
173	DB<19>	-5692.73	-325
174	DB<19>	-5653.74	-325
175	DB<18>	-5614.75	-325
176	DB<18>	-5575.76	-325
177	DB<17>	-5536.77	-325
178	DB<17>	-5497.78	-325
179	DB<16>	-5458.79	-325
180	DB<16>	-5419.8	-325
181	DB<15>	-5380.8	-325

1243	SX<276>	4852.92	191.22
1244	S<462>	4840.92	291.22
1245	S<461>	4828.93	191.22
1246	SX<275>	4816.93	291.22
1247	S<460>	4804.93	191.22
1248	SX<274>	4792.93	291.22
1249	S<459>	4780.94	191.22
1250	S<458>	4768.94	291.22
1251	SX<273>	4756.94	191.22
1252	S<457>	4744.95	291.22
1253	SX<272>	4732.95	191.22
1254	S<456>	4720.95	291.22
1255	S<455>	4708.95	191.22
1256	SX<271>	4696.96	291.22
1257	S<454>	4684.96	191.22
1258	SX<270>	4672.96	291.22
1259	S<453>	4660.96	191.22
1260	S<452>	4648.97	291.22
1261	SX<269>	4636.97	191.22
1262	S<451>	4624.97	291.22
1263	SX<268>	4612.97	191.22
1264	S<450>	4600.98	291.22
1265	S<449>	4588.98	191.22
1266	SX<267>	4576.98	291.22
1267	S<448>	4564.99	191.22
1268	SX<266>	4552.99	291.22
1269	S<447>	4540.99	191.22
1270	S<446>	4528.99	291.22
1271	SX<265>	4517	191.22
1272	S<445>	4505	291.22
1273	SX<264>	4493	191.22
1274	S<444>	4481	291.22
1275	S<443>	4469.01	191.22
1276	SX<263>	4457.01	291.22
1277	S<442>	4445.01	191.22
1278	SX<262>	4433.01	291.22
1279	S<441>	4421.02	191.22
1280	S<440>	4409.02	291.22
1281	SX<261>	4397.02	191.22
1282	S<439>	4385.03	291.22
1283	SX<260>	4373.03	191.22
1284	S<438>	4361.03	291.22
1285	S<437>	4349.03	191.22
1286	SX<259>	4337.04	291.22
1287	S<436>	4325.04	191.22
1288	SX<258>	4313.04	291.22

182	DB<15>	-5341.81	-325
183	DB<14>	-5302.82	-325
184	DB<14>	-5263.83	-325
185	DB<13>	-5224.84	-325
186	DB<13>	-5185.85	-325
187	DB<12>	-5146.86	-325
188	DB<12>	-5107.86	-325
189	HSYNC	-5068.87	-325
190	HSYNC	-5029.88	-325
191	VSYNC	-4990.89	-325
192	VSYNC	-4951.9	-325
193	DE	-4912.91	-325
194	DE	-4873.92	-325
195	VDDI_DRV	-4834.93	-325
196	VDDI_DRV	-4795.93	-325
197	VDD	-4756.94	-325
198	VDD	-4717.95	-325
199	VSSD	-4678.96	-325
200	VSSD	-4639.97	-325
201	PCLK	-4600.98	-325
202	PCLK	-4561.99	-325
203	DB<11>	-4522.99	-325
204	DB<11>	-4484	-325
205	DB<10>	-4445.01	-325
206	DB<10>	-4406.02	-325
207	DB<9>	-4367.03	-325
208	DB<9>	-4328.04	-325
209	DB<8>	-4289.05	-325
210	DB<8>	-4250.06	-325
211	DB<7>	-4211.06	-325
212	DB<7>	-4172.07	-325
213	DB<6>	-4133.08	-325
214	DB<6>	-4094.09	-325
215	DB<5>	-4055.1	-325
216	DB<5>	-4016.11	-325
217	DB<4>	-3977.12	-325
218	DB<4>	-3938.12	-325
219	DB<3>	-3899.13	-325
220	DB<3>	-3860.14	-325
221	DB<2>	-3821.15	-325
222	DB<2>	-3782.16	-325
223	DB<1>	-3743.17	-325
224	DB<1>	-3704.18	-325
225	DB<0>	-3665.19	-325
226	DB<0>	-3626.19	-325
227	VSSD	-3587.2	-325

1289	S<435>	4301.04	191.22
1290	S<434>	4289.05	291.22
1291	SX<257>	4277.05	191.22
1292	S<433>	4265.05	291.22
1293	SX<256>	4253.05	191.22
1294	S<432>	4241.06	291.22
1295	S<431>	4229.06	191.22
1296	SX<255>	4217.06	291.22
1297	S<430>	4205.07	191.22
1298	SX<254>	4193.07	291.22
1299	S<429>	4181.07	191.22
1300	S<428>	4169.07	291.22
1301	SX<253>	4157.08	191.22
1302	S<427>	4145.08	291.22
1303	SX<252>	4133.08	191.22
1304	S<426>	4121.08	291.22
1305	S<425>	4109.09	191.22
1306	SX<251>	4097.09	291.22
1307	S<424>	4085.09	191.22
1308	SX<250>	4073.09	291.22
1309	S<423>	4061.1	191.22
1310	S<422>	4049.1	291.22
1311	SX<249>	4037.1	191.22
1312	S<421>	4025.11	291.22
1313	SX<248>	4013.11	191.22
1314	S<420>	4001.11	291.22
1315	S<419>	3989.11	191.22
1316	SX<247>	3977.12	291.22
1317	S<418>	3965.12	191.22
1318	SX<246>	3953.12	291.22
1319	S<417>	3941.12	191.22
1320	S<416>	3929.13	291.22
1321	SX<245>	3917.13	191.22
1322	S<415>	3905.13	291.22
1323	SX<244>	3893.13	191.22
1324	S<414>	3881.14	291.22
1325	S<413>	3869.14	191.22
1326	SX<243>	3857.14	291.22
1327	S<412>	3845.15	191.22
1328	SX<242>	3833.15	291.22
1329	S<411>	3821.15	191.22
1330	S<410>	3809.15	291.22
1331	SX<241>	3797.16	191.22
1332	S<409>	3785.16	291.22
1333	DUMMY	3725.17	237.22
1334	DUMMY	3713.17	337.22

228	VSSD	-3548.21	-325
229	VDDI_DRV	-3509.22	-325
230	VDDI_DRV	-3470.23	-325
231	CSX	-3431.24	-325
232	CSX	-3392.25	-325
233	SCL	-3353.25	-325
234	SCL	-3314.26	-325
235	RS	-3275.27	-325
236	RS	-3236.28	-325
237	DIN_SDA_DUAL	-3197.29	-325
238	DIN_SDA_DUAL	-3158.3	-325
239	DIN_SDA	-3119.31	-325
240	DIN_SDA	-3080.32	-325
241	TE	-3041.32	-325
242	TE	-3002.33	-325
243	LED_PWM	-2963.34	-325
244	LED_PWM	-2924.35	-325
245	VSSD	-2885.36	-325
246	VSSD	-2846.37	-325
247	VDDI_DRV	-2807.38	-325
248	VDDI_DRV	-2768.38	-325
249	SWIRE	-2729.39	-325
250	SWIRE	-2690.4	-325
251	RSTN_DRV	-2651.41	-325
252	RSTN_DRV	-2612.42	-325
253	VDD	-2573.43	-325
254	VDD	-2534.44	-325
255	VDD	-2495.45	-325
256	VDD	-2456.45	-325
257	VSSD	-2417.46	-325
258	VSSD	-2378.47	-325
259	VSSD	-2339.48	-325
260	VSSD	-2300.49	-325
261	VSSD	-2261.5	-325
262	VDDI	-2222.51	-325
263	VDDI	-2183.51	-325
264	VDDI	-2144.52	-325
265	VDDI	-2105.53	-325
266	ATEST3_LV	-2066.54	-325
267	VDDI_PS	-2027.55	-325
268	VDDI_PS	-1988.56	-325
269	VDDI_PS	-1949.57	-325
270	VDDI_PS	-1910.58	-325
271	PS_ADQ<7>	-1871.58	-325
272	PS_ADQ<7>	-1832.59	-325
273	PS_ADQ<6>	-1793.6	-325

1335	DUMMY	3653.19	237.22
1336	DUMMY	3641.19	337.22
1337	DUMMY	3581.2	237.22
1338	DUMMY	3569.21	337.22
1339	DUMMY	3509.22	237.22
1340	DUMMY	3497.22	337.22
1341	DUMMY	3437.24	237.22
1342	DUMMY	3425.24	337.22
1343	DUMMY	3365.25	237.22
1344	DUMMY	3353.25	337.22
1345	DUMMY	3293.27	237.22
1346	DUMMY	3281.27	337.22
1347	DUMMY	3221.28	237.22
1348	DUMMY	3209.29	337.22
1349	DUMMY	3149.3	237.22
1350	DUMMY	3137.3	337.22
1351	DUMMY	3077.32	237.22
1352	DUMMY	3065.32	337.22
1353	DUMMY	3005.33	237.22
1354	DUMMY	2993.33	337.22
1355	DUMMY	2933.35	237.22
1356	DUMMY	2921.35	337.22
1357	DUMMY	2861.36	237.22
1358	DUMMY	2849.37	337.22
1359	DUMMY	2789.38	237.22
1360	DUMMY	2777.38	337.22
1361	DUMMY	2717.4	237.22
1362	DUMMY	2705.4	337.22
1363	DUMMY	2645.41	237.22
1364	DUMMY	2633.41	337.22
1365	DUMMY	2573.43	237.22
1366	DUMMY	2561.43	337.22
1367	DUMMY	2501.44	237.22
1368	DUMMY	2489.45	337.22
1369	DUMMY	2429.46	237.22
1370	DUMMY	2417.46	337.22
1371	DUMMY	2357.48	237.22
1372	DUMMY	2345.48	337.22
1373	DUMMY	2285.49	237.22
1374	DUMMY	2273.49	337.22
1375	DUMMY	2213.51	237.22
1376	DUMMY	2201.51	337.22
1377	DUMMY	2141.52	237.22
1378	DUMMY	2129.53	337.22
1379	DUMMY	2069.54	237.22
1380	DUMMY	2057.54	337.22

274	PS_ADQ<6>	-1754.61	-325
275	PS_ADQ<5>	-1715.62	-325
276	PS_ADQ<5>	-1676.63	-325
277	PS_ADQ<4>	-1637.64	-325
278	PS_ADQ<4>	-1598.64	-325
279	PS_DQS	-1559.65	-325
280	PS_DQS	-1520.66	-325
281	PS_CLKP	-1481.67	-325
282	PS_CLKP	-1442.68	-325
283	PS_CLKN	-1403.69	-325
284	PS_CLKN	-1364.7	-325
285	VDDI_PS	-1325.71	-325
286	VDDI_PS	-1286.71	-325
287	VDDI_PS	-1247.72	-325
288	VDDI_PS	-1208.73	-325
289	VSSD	-1169.74	-325
290	VSSD	-1130.75	-325
291	VSSD	-1091.76	-325
292	VSSD	-1052.77	-325
293	VREF_PS	-1013.77	-325
294	VREF_PS	-974.78	-325
295	VREF_PS	-935.79	-325
296	VREF_PS	-896.8	-325
297	PS_CEN	-857.81	-325
298	PS_CEN	-818.82	-325
299	PS_DM	-779.83	-325
300	PS_DM	-740.84	-325
301	PS_ADQ<3>	-701.84	-325
302	PS_ADQ<3>	-662.85	-325
303	PS_ADQ<2>	-623.86	-325
304	PS_ADQ<2>	-584.87	-325
305	PS_ADQ<1>	-545.88	-325
306	PS_ADQ<1>	-506.89	-325
307	PS_ADQ<0>	-467.9	-325
308	PS_ADQ<0>	-428.9	-325
309	VSSD	-389.91	-325
310	VSSD	-350.92	-325
311	VSSD	-311.93	-325
312	VSSD	-272.94	-325
313	VDDI_PS	-233.95	-325
314	VDDI_PS	-194.96	-325
315	VDDI_PS	-155.97	-325
316	VDDI_PS	-116.97	-325
317	VDD	-77.98	-325
318	VDD	-38.99	-325
319	VSSD	0	-325

1381	DUMMY	1997.56	237.22
1382	DUMMY	1985.56	337.22
1383	DUMMY	1925.57	237.22
1384	DUMMY	1913.57	337.22
1385	DUMMY	1853.59	237.22
1386	DUMMY	1841.59	337.22
1387	DUMMY	1781.6	237.22
1388	DUMMY	1769.61	337.22
1389	DUMMY	1709.62	237.22
1390	DUMMY	1697.62	337.22
1391	DUMMY	1637.64	237.22
1392	DUMMY	1625.64	337.22
1393	DUMMY	1565.65	237.22
1394	DUMMY	1553.65	337.22
1395	DUMMY	1493.67	237.22
1396	DUMMY	1481.67	337.22
1397	DUMMY	1421.68	237.22
1398	DUMMY	1409.69	337.22
1399	DUMMY	1349.7	237.22
1400	DUMMY	1337.7	337.22
1401	DUMMY	1277.72	237.22
1402	DUMMY	1265.72	337.22
1403	DUMMY	1205.73	237.22
1404	DUMMY	1193.73	337.22
1405	DUMMY	1133.75	237.22
1406	DUMMY	1121.75	337.22
1407	DUMMY	1061.76	237.22
1408	DUMMY	1049.77	337.22
1409	DUMMY	989.78	237.22
1410	DUMMY	977.78	337.22
1411	DUMMY	917.8	237.22
1412	DUMMY	905.8	337.22
1413	DUMMY	845.81	237.22
1414	DUMMY	833.81	337.22
1415	DUMMY	773.83	237.22
1416	DUMMY	761.83	337.22
1417	DUMMY	701.84	237.22
1418	DUMMY	689.85	337.22
1419	DUMMY	629.86	237.22
1420	DUMMY	617.86	337.22
1421	DUMMY	557.88	237.22
1422	DUMMY	545.88	337.22
1423	DUMMY	485.89	237.22
1424	DUMMY	473.89	337.22
1425	DUMMY	437.9	291.22
1426	DUMMY	389.91	291.22

320	VSSD	38.99	-325
321	VSSD	77.98	-325
322	VDDI	116.97	-325
323	VDDI	155.97	-325
324	VDDI	194.96	-325
325	VDDI	233.95	-325
326	VDD_PLL	272.94	-325
327	VDD_PLL	311.93	-325
328	VDD_OSC	350.92	-325
329	VDD_OSC	389.91	-325
330	VSS_OSC	428.9	-325
331	VSS_OSC	467.9	-325
332	OSC_IN	506.89	-325
333	OSC_TE	545.88	-325
334	VDDI_AO	584.87	-325
335	VDDI_AO	623.86	-325
336	VSSA_REF	662.85	-325
337	VSSA_REF	701.84	-325
338	VREF	740.84	-325
339	VREF	779.83	-325
340	VREF	818.82	-325
341	ATEST5_PV	857.81	-325
342	VSP	896.8	-325
343	VSP	935.79	-325
344	VSP	974.78	-325
345	VSP	1013.77	-325
346	VSP	1052.77	-325
347	VSSA	1091.76	-325
348	VSSA	1130.75	-325
349	VSSA	1169.74	-325
350	VSSA	1208.73	-325
351	VDN	1247.72	-325
352	VDN	1286.71	-325
353	VDN	1325.71	-325
354	VDN	1364.7	-325
355	VSN	1403.69	-325
356	VSN	1442.68	-325
357	VSN	1481.67	-325
358	VSN	1520.66	-325
359	VCL	1559.65	-325
360	VCL	1598.64	-325
361	ATEST4_NV	1637.64	-325
362	VDD	1676.63	-325
363	VDD	1715.62	-325
364	VSSD	1754.61	-325
365	VSSD	1793.6	-325

1427	DUMMY	341.92	291.22
1428	DUMMY	293.93	291.22
1429	DUMMY	245.95	291.22
1430	DUMMY	197.96	291.22
1431	DUMMY	149.97	291.22
1432	DUMMY	101.98	291.22
1433	DUMMY	53.99	291.22
1434	DUMMY	6	291.22
1435	DUMMY	-41.99	291.22
1436	DUMMY	-89.98	291.22
1437	DUMMY	-137.97	291.22
1438	DUMMY	-185.96	291.22
1439	DUMMY	-233.95	291.22
1440	DUMMY	-281.94	291.22
1441	DUMMY	-329.93	291.22
1442	DUMMY	-377.92	291.22
1443	DUMMY	-425.91	291.22
1444	DUMMY	-473.89	291.22
1445	DUMMY	-521.88	291.22
1446	DUMMY	-569.87	291.22
1447	DUMMY	-617.86	291.22
1448	DUMMY	-665.85	291.22
1449	DUMMY	-713.84	291.22
1450	DUMMY	-761.83	291.22
1451	DUMMY	-809.82	291.22
1452	DUMMY	-857.81	291.22
1453	DUMMY	-905.8	291.22
1454	DUMMY	-953.79	291.22
1455	DUMMY	-1001.78	291.22
1456	DUMMY	-1049.77	291.22
1457	DUMMY	-1097.76	291.22
1458	DUMMY	-1145.75	291.22
1459	DUMMY	-1193.73	291.22
1460	DUMMY	-1241.72	291.22
1461	DUMMY	-1289.71	291.22
1462	DUMMY	-1337.7	291.22
1463	DUMMY	-1385.69	291.22
1464	DUMMY	-1733.61	291.22
1465	DUMMY	-1781.6	291.22
1466	DUMMY	-1829.59	291.22
1467	DUMMY	-1877.58	291.22
1468	DUMMY	-1925.57	291.22
1469	DUMMY	-1973.56	291.22
1470	DUMMY	-2021.55	291.22
1471	DUMMY	-2069.54	291.22
1472	DUMMY	-2117.53	291.22

366	PSW_ENN	1832.59	-325
367	PSW_PRIO_SEL	1871.58	-325
368	VSSD	1910.58	-325
369	VSSD	1949.57	-325
370	VSSD	1988.56	-325
371	VSSD	2027.55	-325
372	PMOD_SEL	2066.54	-325
373	IGZO_MOD	2105.53	-325
374	VSSD	2144.52	-325
375	VSSD	2183.51	-325
376	BS<3>	2222.51	-325
377	BS<2>	2261.5	-325
378	BS<1>	2300.49	-325
379	BS<0>	2339.48	-325
380	IM<3>	2378.47	-325
381	IM<2>	2417.46	-325
382	IM<1>	2456.45	-325
383	IM<0>	2495.45	-325
384	VSSD	2534.44	-325
385	VSSD	2573.43	-325
386	VSSD	2612.42	-325
387	VSSD	2651.41	-325
388	CSN_FLH	2690.4	-325
389	CSN_FLH	2729.39	-325
390	SCK_FLH	2768.38	-325
391	SCK_FLH	2807.38	-325
392	MISO_FLH	2846.37	-325
393	MISO_FLH	2885.36	-325
394	MOSI_FLH	2924.35	-325
395	MOSI_FLH	2963.34	-325
396	VDDI_FLH	3002.33	-325
397	VDDI_FLH	3041.32	-325
398	VDD_TP	3080.32	-325
399	VDD_TP	3119.31	-325
400	VSSD	3158.3	-325
401	VSSD	3197.29	-325
402	VSSD	3236.28	-325
403	VSSD	3275.27	-325
404	VSSD	3314.26	-325
405	SCAN_MODE	3353.25	-325
406	SCAN_MODE	3392.25	-325
407	SCAN_EN	3431.24	-325
408	SCAN_EN	3470.23	-325
409	SCAN_IN<2>	3509.22	-325
410	SCAN_IN<2>	3548.21	-325
411	SCAN_IN<1>	3587.2	-325

1473	DUMMY	-2165.52	291.22
1474	DUMMY	-2213.51	291.22
1475	DUMMY	-2261.5	291.22
1476	DUMMY	-2309.49	291.22
1477	DUMMY	-2357.48	291.22
1478	DUMMY	-2405.47	291.22
1479	DUMMY	-2453.45	291.22
1480	DUMMY	-2501.44	291.22
1481	DUMMY	-2549.43	291.22
1482	DUMMY	-2597.42	291.22
1483	DUMMY	-2645.41	291.22
1484	DUMMY	-2693.4	291.22
1485	DUMMY	-2741.39	291.22
1486	DUMMY	-2789.38	291.22
1487	DUMMY	-2837.37	291.22
1488	DUMMY	-2885.36	291.22
1489	DUMMY	-2933.35	291.22
1490	DUMMY	-2981.34	291.22
1491	DUMMY	-3029.33	291.22
1492	DUMMY	-3077.32	291.22
1493	DUMMY	-3125.31	291.22
1494	DUMMY	-3173.29	291.22
1495	DUMMY	-3221.28	291.22
1496	DUMMY	-3269.27	291.22
1497	DUMMY	-3317.26	291.22
1498	DUMMY	-3365.25	291.22
1499	DUMMY	-3413.24	291.22
1500	DUMMY	-3461.23	291.22
1501	DUMMY	-3509.22	291.22
1502	DUMMY	-3557.21	291.22
1503	DUMMY	-3593.2	191.22
1504	DUMMY	-3605.2	291.22
1505	DUMMY	-3617.2	191.22
1506	DUMMY	-3629.19	291.22
1507	DUMMY	-3641.19	191.22
1508	DUMMY	-3653.19	291.22
1509	SX<240>	-3665.19	191.22
1510	S<408>	-3677.18	291.22
1511	S<407>	-3689.18	191.22
1512	VSSA	-3701.18	291.22
1513	S<406>	-3713.17	191.22
1514	SX<239>	-3725.17	291.22
1515	S<405>	-3737.17	191.22
1516	S<404>	-3749.17	291.22
1517	VSSA	-3761.16	191.22
1518	S<403>	-3773.16	291.22

412	SCAN_IN<1>	3626.19	-325
413	SCAN_IN<0>	3665.19	-325
414	SCAN_IN<0>	3704.18	-325
415	SCAN_OUT<2>	3743.17	-325
416	SCAN_OUT<2>	3782.16	-325
417	SCAN_OUT<1>	3821.15	-325
418	SCAN_OUT<1>	3860.14	-325
419	SCAN_OUT<0>	3899.13	-325
420	SCAN_OUT<0>	3938.12	-325
421	WORK_MODE	3977.12	-325
422	WORK_MODE	4016.11	-325
423	TS_SEL	4055.1	-325
424	TS_SEL	4094.09	-325
425	RSTN_TP	4133.08	-325
426	RSTN_TP	4172.07	-325
427	VDDI_TP	4211.06	-325
428	VDDI_TP	4250.06	-325
429	VDDI_TP	4289.05	-325
430	VDDI_TP	4328.04	-325
431	VDDI_TP	4367.03	-325
432	VSSD	4406.02	-325
433	VSSD	4445.01	-325
434	CSN_TP	4484	-325
435	CSN_TP	4522.99	-325
436	SCK_TP	4561.99	-325
437	SCK_TP	4600.98	-325
438	MISO_TP	4639.97	-325
439	MISO_TP	4678.96	-325
440	MOSI_TP	4717.95	-325
441	MOSI_TP	4756.94	-325
442	GPIO<7>	4795.93	-325
443	GPIO<7>	4834.93	-325
444	VDD_TP	4873.92	-325
445	VDD_TP	4912.91	-325
446	VSSD	4951.9	-325
447	VSSD	4990.89	-325
448	VSSD	5029.88	-325
449	GPIO<6>	5068.87	-325
450	GPIO<6>	5107.86	-325
451	GPIO<5>	5146.86	-325
452	GPIO<5>	5185.85	-325
453	GPIO<4>	5224.84	-325
454	GPIO<4>	5263.83	-325
455	GPIO<3>	5302.82	-325
456	GPIO<3>	5341.81	-325
457	GPIO<2>	5380.8	-325

1519	SX<238>	-3785.16	191.22
1520	S<402>	-3797.16	291.22
1521	S<401>	-3809.15	191.22
1522	VSSA	-3821.15	291.22
1523	S<400>	-3833.15	191.22
1524	SX<237>	-3845.15	291.22
1525	S<399>	-3857.14	191.22
1526	S<398>	-3869.14	291.22
1527	VSSA	-3881.14	191.22
1528	S<397>	-3893.13	291.22
1529	SX<236>	-3905.13	191.22
1530	S<396>	-3917.13	291.22
1531	S<395>	-3929.13	191.22
1532	SX<235>	-3941.12	291.22
1533	S<394>	-3953.12	191.22
1534	SX<234>	-3965.12	291.22
1535	S<393>	-3977.12	191.22
1536	S<392>	-3989.11	291.22
1537	SX<233>	-4001.11	191.22
1538	S<391>	-4013.11	291.22
1539	SX<232>	-4025.11	191.22
1540	S<390>	-4037.1	291.22
1541	S<389>	-4049.1	191.22
1542	SX<231>	-4061.1	291.22
1543	S<388>	-4073.09	191.22
1544	SX<230>	-4085.09	291.22
1545	S<387>	-4097.09	191.22
1546	S<386>	-4109.09	291.22
1547	SX<229>	-4121.08	191.22
1548	S<385>	-4133.08	291.22
1549	SX<228>	-4145.08	191.22
1550	S<384>	-4157.08	291.22
1551	S<383>	-4169.07	191.22
1552	SX<227>	-4181.07	291.22
1553	S<382>	-4193.07	191.22
1554	SX<226>	-4205.07	291.22
1555	S<381>	-4217.06	191.22
1556	S<380>	-4229.06	291.22
1557	SX<225>	-4241.06	191.22
1558	S<379>	-4253.05	291.22
1559	SX<224>	-4265.05	191.22
1560	S<378>	-4277.05	291.22
1561	S<377>	-4289.05	191.22
1562	VSSA	-4301.04	291.22
1563	S<376>	-4313.04	191.22
1564	SX<223>	-4325.04	291.22

458	GPIO<2>	5419.8	-325
459	GPIO<1>	5458.79	-325
460	GPIO<1>	5497.78	-325
461	GPIO<0>	5536.77	-325
462	GPIO<0>	5575.76	-325
463	VSSD	5614.75	-325
464	VSSD	5653.74	-325
465	VSSD	5692.73	-325
466	VSSD	5731.73	-325
467	VSSD	5770.72	-325
468	VSSD	5809.71	-325
469	VSSD	5848.7	-325
470	VSSD	5887.69	-325
471	VDDI_TP	5926.68	-325
472	VDDI_TP	5965.67	-325
473	VDDI_TP	6004.67	-325
474	VDDI_TP	6043.66	-325
475	VDD_TP	6082.65	-325
476	VDD_TP	6121.64	-325
477	VSSD	6160.63	-325
478	VSSD	6199.62	-325
479	VSSD	6238.61	-325
480	VSSD	6277.6	-325
481	VDD	6316.6	-325
482	VDD	6355.59	-325
483	VDD	6394.58	-325
484	VDD	6433.57	-325
485	ATEST6_PV	6472.56	-325
486	VSP	6511.55	-325
487	VSP	6550.54	-325
488	VSP	6589.54	-325
489	VSSA	6628.53	-325
490	VSSA	6667.52	-325
491	VSSA	6706.51	-325
492	VDN	6745.5	-325
493	VDN	6784.49	-325
494	VDN	6823.48	-325
495	VSN	6862.47	-325
496	VSN	6901.47	-325
497	VSN	6940.46	-325
498	VCL	6979.45	-325
499	VCL	7018.44	-325
500	VDDA_VCOM	7057.43	-325
501	VDDA_VCOM	7096.42	-325
502	VCOM	7135.41	-325
503	VCOM	7174.41	-325

1565	S<375>	-4337.04	191.22
1566	S<374>	-4349.03	291.22
1567	VSSA	-4361.03	191.22
1568	S<373>	-4373.03	291.22
1569	SX<222>	-4385.03	191.22
1570	S<372>	-4397.02	291.22
1571	S<371>	-4409.02	191.22
1572	VSSA	-4421.02	291.22
1573	S<370>	-4433.01	191.22
1574	SX<221>	-4445.01	291.22
1575	S<369>	-4457.01	191.22
1576	S<368>	-4469.01	291.22
1577	VSSA	-4481	191.22
1578	S<367>	-4493	291.22
1579	SX<220>	-4505	191.22
1580	S<366>	-4517	291.22
1581	S<365>	-4528.99	191.22
1582	SX<219>	-4540.99	291.22
1583	S<364>	-4552.99	191.22
1584	SX<218>	-4564.99	291.22
1585	S<363>	-4576.98	191.22
1586	S<362>	-4588.98	291.22
1587	SX<217>	-4600.98	191.22
1588	S<361>	-4612.97	291.22
1589	SX<216>	-4624.97	191.22
1590	S<360>	-4636.97	291.22
1591	S<359>	-4648.97	191.22
1592	SX<215>	-4660.96	291.22
1593	S<358>	-4672.96	191.22
1594	SX<214>	-4684.96	291.22
1595	S<357>	-4696.96	191.22
1596	S<356>	-4708.95	291.22
1597	SX<213>	-4720.95	191.22
1598	S<355>	-4732.95	291.22
1599	SX<212>	-4744.95	191.22
1600	S<354>	-4756.94	291.22
1601	S<353>	-4768.94	191.22
1602	SX<211>	-4780.94	291.22
1603	S<352>	-4792.93	191.22
1604	SX<210>	-4804.93	291.22
1605	S<351>	-4816.93	191.22
1606	S<350>	-4828.93	291.22
1607	SX<209>	-4840.92	191.22
1608	S<349>	-4852.92	291.22
1609	SX<208>	-4864.92	191.22
1610	S<348>	-4876.92	291.22

504	VCOM	7213.4	-325
505	VCOM	7252.39	-325
506	VCOM	7291.38	-325
507	VCOM	7330.37	-325
508	VCOM	7369.36	-325
509	VCOM	7408.35	-325
510	ATEST7_NV	7447.34	-325
511	VREF_TP	7486.34	-325
512	VREF_TP	7525.33	-325
513	VCG_TP	7564.32	-325
514	VCG_TP	7603.31	-325
515	VSSA	7642.3	-325
516	VSSA	7681.29	-325
517	VSSA	7720.28	-325
518	VSSA	7759.28	-325
519	VSSA	7798.27	-325
520	VSSA	7837.26	-325
521	VSNOUT	7876.25	-325
522	VSNOUT	7915.24	-325
523	VSNOUT	7954.23	-325
524	VSNOUT	7993.22	-325
525	VSNOUT	8032.21	-325
526	C21N	8071.21	-325
527	C21N	8110.2	-325
528	C21N	8149.19	-325
529	C21N	8188.18	-325
530	C21N	8227.17	-325
531	C21P	8266.16	-325
532	C21P	8305.15	-325
533	C21P	8344.15	-325
534	C21P	8383.14	-325
535	C21P	8422.13	-325
536	VSPOUT	8461.12	-325
537	VSPOUT	8500.11	-325
538	VSPOUT	8539.1	-325
539	VSPOUT	8578.09	-325
540	VSPOUT	8617.08	-325
541	C12N	8656.08	-325
542	C12N	8695.07	-325
543	C12N	8734.06	-325
544	C12N	8773.05	-325
545	C12N	8812.04	-325
546	C12P	8851.03	-325
547	C12P	8890.02	-325
548	C12P	8929.02	-325
549	C12P	8968.01	-325

1611	S<347>	-4888.91	191.22
1612	SX<207>	-4900.91	291.22
1613	S<346>	-4912.91	191.22
1614	SX<206>	-4924.91	291.22
1615	S<345>	-4936.9	191.22
1616	S<344>	-4948.9	291.22
1617	SX<205>	-4960.9	191.22
1618	S<343>	-4972.89	291.22
1619	SX<204>	-4984.89	191.22
1620	S<342>	-4996.89	291.22
1621	S<341>	-5008.89	191.22
1622	SX<203>	-5020.88	291.22
1623	S<340>	-5032.88	191.22
1624	SX<202>	-5044.88	291.22
1625	S<339>	-5056.88	191.22
1626	S<338>	-5068.87	291.22
1627	SX<201>	-5080.87	191.22
1628	S<337>	-5092.87	291.22
1629	SX<200>	-5104.87	191.22
1630	S<336>	-5116.86	291.22
1631	S<335>	-5128.86	191.22
1632	SX<199>	-5140.86	291.22
1633	S<334>	-5152.85	191.22
1634	SX<198>	-5164.85	291.22
1635	S<333>	-5176.85	191.22
1636	S<332>	-5188.85	291.22
1637	SX<197>	-5200.84	191.22
1638	S<331>	-5212.84	291.22
1639	SX<196>	-5224.84	191.22
1640	S<330>	-5236.84	291.22
1641	S<329>	-5248.83	191.22
1642	SX<195>	-5260.83	291.22
1643	S<328>	-5272.83	191.22
1644	SX<194>	-5284.83	291.22
1645	S<327>	-5296.82	191.22
1646	S<326>	-5308.82	291.22
1647	SX<193>	-5320.82	191.22
1648	S<325>	-5332.81	291.22
1649	SX<192>	-5344.81	191.22
1650	S<324>	-5356.81	291.22
1651	S<323>	-5368.81	191.22
1652	VSSA	-5380.8	291.22
1653	S<322>	-5392.8	191.22
1654	SX<191>	-5404.8	291.22
1655	S<321>	-5416.8	191.22
1656	S<320>	-5428.79	291.22

550	C12P	9007	-325
551	VCI	9045.99	-325
552	VCI	9084.98	-325
553	VCI	9123.97	-325
554	VCI	9162.96	-325
555	VCI	9201.95	-325
556	VSSA	9240.95	-325
557	VSSA	9279.94	-325
558	VSSA	9318.93	-325
559	VSSA	9357.92	-325
560	VSSA	9396.91	-325
561	C11N	9435.9	-325
562	C11N	9474.89	-325
563	C11N	9513.89	-325
564	C11N	9552.88	-325
565	C11N	9591.87	-325
566	C11P	9630.86	-325
567	C11P	9669.85	-325
568	C11P	9708.84	-325
569	C11P	9747.83	-325
570	C11P	9786.82	-325
571	VDD_TP	9825.82	-325
572	VDD_TP	9864.81	-325
573	VDD_TP	9903.8	-325
574	VDD_TP	9942.79	-325
575	VDDI_TP	9981.78	-325
576	VDDI_TP	10020.77	-325
577	VDDI_TP	10059.76	-325
578	VDDI_TP	10098.76	-325
579	VSSD	10137.75	-325
580	VSSD	10176.74	-325
581	VDD	10215.73	-325
582	VDD	10254.72	-325
583	VGL	10293.71	-325
584	VGL	10332.7	-325
585	VGH	10371.69	-325
586	VGH	10410.69	-325
587	CGOUT_R<17>	10449.68	-325
588	CGOUT_R<16>	10488.67	-325
589	CGOUT_R<15>	10527.66	-325
590	CGOUT_R<14>	10566.65	-325
591	CGOUT_R<13>	10605.64	-325
592	CGOUT_R<12>	10644.63	-325
593	CGOUT_R<11>	10683.63	-325
594	CGOUT_R<10>	10722.62	-325
595	CGOUT_R<9>	10761.61	-325

1657	VSSA	-5440.79	191.22
1658	S<319>	-5452.79	291.22
1659	SX<190>	-5464.79	191.22
1660	S<318>	-5476.78	291.22
1661	S<317>	-5488.78	191.22
1662	VSSA	-5500.78	291.22
1663	S<316>	-5512.77	191.22
1664	SX<189>	-5524.77	291.22
1665	S<315>	-5536.77	191.22
1666	S<314>	-5548.77	291.22
1667	VSSA	-5560.76	191.22
1668	S<313>	-5572.76	291.22
1669	SX<188>	-5584.76	191.22
1670	S<312>	-5596.76	291.22
1671	S<311>	-5608.75	191.22
1672	SX<187>	-5620.75	291.22
1673	S<310>	-5632.75	191.22
1674	SX<186>	-5644.75	291.22
1675	S<309>	-5656.74	191.22
1676	S<308>	-5668.74	291.22
1677	SX<185>	-5680.74	191.22
1678	S<307>	-5692.73	291.22
1679	SX<184>	-5704.73	191.22
1680	S<306>	-5716.73	291.22
1681	S<305>	-5728.73	191.22
1682	SX<183>	-5740.72	291.22
1683	S<304>	-5752.72	191.22
1684	SX<182>	-5764.72	291.22
1685	S<303>	-5776.72	191.22
1686	S<302>	-5788.71	291.22
1687	SX<181>	-5800.71	191.22
1688	S<301>	-5812.71	291.22
1689	SX<180>	-5824.71	191.22
1690	S<300>	-5836.7	291.22
1691	S<299>	-5848.7	191.22
1692	SX<179>	-5860.7	291.22
1693	S<298>	-5872.69	191.22
1694	SX<178>	-5884.69	291.22
1695	S<297>	-5896.69	191.22
1696	S<296>	-5908.69	291.22
1697	SX<177>	-5920.68	191.22
1698	S<295>	-5932.68	291.22
1699	SX<176>	-5944.68	191.22
1700	S<294>	-5956.68	291.22
1701	S<293>	-5968.67	191.22
1702	SX<175>	-5980.67	291.22

596	CGOUT_R<8>	10800.6	-325
597	CGOUT_R<7>	10839.59	-325
598	CGOUT_R<6>	10878.58	-325
599	CGOUT_R<5>	10917.57	-325
600	CGOUT_R<4>	10956.56	-325
601	CGOUT_R<3>	10995.56	-325
602	CGOUT_R<2>	11034.55	-325
603	CGOUT_R<1>	11073.54	-325
604	VGHO_REF	11112.53	-325
605	VGHO_REF	11151.52	-325
606	VGHO_REF	11190.51	-325
607	VGHO_R	11229.5	-325
608	VGHO_R	11268.5	-325
609	VGHO_R	11307.49	-325
610	VGHO_R	11346.48	-325
611	VGHO_R	11385.47	-325
612	VGLO_R	11424.46	-325
613	VGLO_R	11463.45	-325
614	VGLO_R	11502.44	-325
615	VGLO_R	11541.43	-325
616	VGLO_R	11580.43	-325
617	VGLO_REF	11619.42	-325
618	VGLO_REF	11658.41	-325
619	VCOM_PASS_R	11697.4	-325
620	VSN	11736.39	-325
621	VSN	11775.38	-325
622	VSP	11814.37	-325
623	VSP	11853.37	-325
624	VSSA	11892.36	-325
625	VSSA	11931.35	-325
626	VSSA	11970.34	-325
627	VSSA	12009.33	-325
628	VSSA	12048.32	-325
629	VGHOUT2	12087.31	-325
630	VGHOUT2	12126.3	-325
631	VGHOUT2	12165.3	-325
632	VGH	12204.29	-325
633	VGH	12243.28	-325
634	VGH	12282.27	-325
635	VGHOUT1	12321.26	-325
636	VGHOUT1	12360.25	-325
637	VGHOUT1	12399.24	-325
638	VSSA	12111.31	291.22
639	VSSA	12099.31	191.22
640	VSSA	12087.31	291.22
641	VSSA	12075.32	191.22
1703	S<292>	-5992.67	191.22
1704	SX<174>	-6004.67	291.22
1705	S<291>	-6016.66	191.22
1706	S<290>	-6028.66	291.22
1707	SX<173>	-6040.66	191.22
1708	S<289>	-6052.65	291.22
1709	SX<172>	-6064.65	191.22
1710	S<288>	-6076.65	291.22
1711	S<287>	-6088.65	191.22
1712	SX<171>	-6100.64	291.22
1713	S<286>	-6112.64	191.22
1714	SX<170>	-6124.64	291.22
1715	S<285>	-6136.64	191.22
1716	S<284>	-6148.63	291.22
1717	SX<169>	-6160.63	191.22
1718	S<283>	-6172.63	291.22
1719	SX<168>	-6184.63	191.22
1720	S<282>	-6196.62	291.22
1721	S<281>	-6208.62	191.22
1722	SX<167>	-6220.62	291.22
1723	S<280>	-6232.61	191.22
1724	SX<166>	-6244.61	291.22
1725	S<279>	-6256.61	191.22
1726	S<278>	-6268.61	291.22
1727	SX<165>	-6280.6	191.22
1728	S<277>	-6292.6	291.22
1729	SX<164>	-6304.6	191.22
1730	S<276>	-6316.6	291.22
1731	S<275>	-6328.59	191.22
1732	SX<163>	-6340.59	291.22
1733	S<274>	-6352.59	191.22
1734	SX<162>	-6364.59	291.22
1735	S<273>	-6376.58	191.22
1736	S<272>	-6388.58	291.22
1737	SX<161>	-6400.58	191.22
1738	S<271>	-6412.57	291.22
1739	VSSA	-6424.57	191.22
1740	VSSA	-6436.57	291.22
1741	VSSA	-6448.57	191.22
1742	VSSA	-6460.56	291.22
1743	VSSA	-6472.56	191.22
1744	VSSA	-6484.56	291.22
1745	VSSA	-6496.56	191.22
1746	VSSA	-6508.55	291.22
1747	VSSA	-6520.55	191.22
1748	VSSA	-6532.55	291.22

642	VSSA	12063.32	291.22
643	VSSA	12051.32	191.22
644	VSSA	12039.32	291.22
645	VCOM_PASS_R	12027.33	191.22
646	VCOM_PASS_R	12015.33	291.22
647	SDUM2	12003.33	191.22
648	SX<480>	11991.33	291.22
649	S<810>	11979.34	191.22
650	S<809>	11967.34	291.22
651	VSSA	11955.34	191.22
652	S<808>	11943.35	291.22
653	SX<479>	11931.35	191.22
654	S<807>	11919.35	291.22
655	S<806>	11907.35	191.22
656	VSSA	11895.36	291.22
657	S<805>	11883.36	191.22
658	SX<478>	11871.36	291.22
659	S<804>	11859.36	191.22
660	S<803>	11847.37	291.22
661	VSSA	11835.37	191.22
662	S<802>	11823.37	291.22
663	SX<477>	11811.37	191.22
664	S<801>	11799.38	291.22
665	S<800>	11787.38	191.22
666	VSSA	11775.38	291.22
667	S<799>	11763.39	191.22
668	SX<476>	11751.39	291.22
669	S<798>	11739.39	191.22
670	S<797>	11727.39	291.22
671	SX<475>	11715.4	191.22
672	S<796>	11703.4	291.22
673	SX<474>	11691.4	191.22
674	S<795>	11679.4	291.22
675	S<794>	11667.41	191.22
676	SX<473>	11655.41	291.22
677	S<793>	11643.41	191.22
678	SX<472>	11631.41	291.22
679	S<792>	11619.42	191.22
680	S<791>	11607.42	291.22
681	SX<471>	11595.42	191.22
682	S<790>	11583.43	291.22
683	SX<470>	11571.43	191.22
684	S<789>	11559.43	291.22
685	S<788>	11547.43	191.22
686	SX<469>	11535.44	291.22
687	S<787>	11523.44	191.22

1749	VSSA	-6544.55	191.22
1750	VSSA	-6556.54	291.22
1751	VSSA	-6568.54	191.22
1752	VSSA	-6580.54	291.22
1753	VSSA	-6592.53	191.22
1754	SX<160>	-6604.53	291.22
1755	S<270>	-6616.53	191.22
1756	S<269>	-6628.53	291.22
1757	VSSA	-6640.52	191.22
1758	S<268>	-6652.52	291.22
1759	SX<159>	-6664.52	191.22
1760	S<267>	-6676.52	291.22
1761	S<266>	-6688.51	191.22
1762	VSSA	-6700.51	291.22
1763	S<265>	-6712.51	191.22
1764	SX<158>	-6724.51	291.22
1765	S<264>	-6736.5	191.22
1766	S<263>	-6748.5	291.22
1767	VSSA	-6760.5	191.22
1768	S<262>	-6772.49	291.22
1769	SX<157>	-6784.49	191.22
1770	S<261>	-6796.49	291.22
1771	S<260>	-6808.49	191.22
1772	VSSA	-6820.48	291.22
1773	S<259>	-6832.48	191.22
1774	SX<156>	-6844.48	291.22
1775	S<258>	-6856.48	191.22
1776	S<257>	-6868.47	291.22
1777	SX<155>	-6880.47	191.22
1778	S<256>	-6892.47	291.22
1779	SX<154>	-6904.47	191.22
1780	S<255>	-6916.46	291.22
1781	S<254>	-6928.46	191.22
1782	SX<153>	-6940.46	291.22
1783	S<253>	-6952.45	191.22
1784	SX<152>	-6964.45	291.22
1785	S<252>	-6976.45	191.22
1786	S<251>	-6988.45	291.22
1787	SX<151>	-7000.44	191.22
1788	S<250>	-7012.44	291.22
1789	SX<150>	-7024.44	191.22
1790	S<249>	-7036.44	291.22
1791	S<248>	-7048.43	191.22
1792	SX<149>	-7060.43	291.22
1793	S<247>	-7072.43	191.22
1794	SX<148>	-7084.43	291.22

688	SX<468>	11511.44	291.22
689	S<786>	11499.44	191.22
690	S<785>	11487.45	291.22
691	SX<467>	11475.45	191.22
692	S<784>	11463.45	291.22
693	SX<466>	11451.45	191.22
694	S<783>	11439.46	291.22
695	S<782>	11427.46	191.22
696	SX<465>	11415.46	291.22
697	S<781>	11403.47	191.22
698	SX<464>	11391.47	291.22
699	S<780>	11379.47	191.22
700	S<779>	11367.47	291.22
701	SX<463>	11355.48	191.22
702	S<778>	11343.48	291.22
703	SX<462>	11331.48	191.22
704	S<777>	11319.48	291.22
705	S<776>	11307.49	191.22
706	SX<461>	11295.49	291.22
707	S<775>	11283.49	191.22
708	SX<460>	11271.49	291.22
709	S<774>	11259.5	191.22
710	S<773>	11247.5	291.22
711	SX<459>	11235.5	191.22
712	S<772>	11223.51	291.22
713	SX<458>	11211.51	191.22
714	S<771>	11199.51	291.22
715	S<770>	11187.51	191.22
716	SX<457>	11175.52	291.22
717	S<769>	11163.52	191.22
718	SX<456>	11151.52	291.22
719	S<768>	11139.52	191.22
720	S<767>	11127.53	291.22
721	SX<455>	11115.53	191.22
722	S<766>	11103.53	291.22
723	SX<454>	11091.53	191.22
724	S<765>	11079.54	291.22
725	S<764>	11067.54	191.22
726	SX<453>	11055.54	291.22
727	S<763>	11043.55	191.22
728	SX<452>	11031.55	291.22
729	S<762>	11019.55	191.22
730	S<761>	11007.55	291.22
731	SX<451>	10995.56	191.22
732	S<760>	10983.56	291.22
733	SX<450>	10971.56	191.22

1795	S<246>	-7096.42	191.22
1796	S<245>	-7108.42	291.22
1797	SX<147>	-7120.42	191.22
1798	S<244>	-7132.41	291.22
1799	SX<146>	-7144.41	191.22
1800	S<243>	-7156.41	291.22
1801	S<242>	-7168.41	191.22
1802	SX<145>	-7180.4	291.22
1803	S<241>	-7192.4	191.22
1804	SX<144>	-7204.4	291.22
1805	S<240>	-7216.4	191.22
1806	S<239>	-7228.39	291.22
1807	SX<143>	-7240.39	191.22
1808	S<238>	-7252.39	291.22
1809	SX<142>	-7264.39	191.22
1810	S<237>	-7276.38	291.22
1811	S<236>	-7288.38	191.22
1812	SX<141>	-7300.38	291.22
1813	S<235>	-7312.37	191.22
1814	SX<140>	-7324.37	291.22
1815	S<234>	-7336.37	191.22
1816	S<233>	-7348.37	291.22
1817	SX<139>	-7360.36	191.22
1818	S<232>	-7372.36	291.22
1819	SX<138>	-7384.36	191.22
1820	S<231>	-7396.36	291.22
1821	S<230>	-7408.35	191.22
1822	SX<137>	-7420.35	291.22
1823	S<229>	-7432.35	191.22
1824	SX<136>	-7444.35	291.22
1825	S<228>	-7456.34	191.22
1826	S<227>	-7468.34	291.22
1827	SX<135>	-7480.34	191.22
1828	S<226>	-7492.33	291.22
1829	SX<134>	-7504.33	191.22
1830	S<225>	-7516.33	291.22
1831	S<224>	-7528.33	191.22
1832	SX<133>	-7540.32	291.22
1833	S<223>	-7552.32	191.22
1834	SX<132>	-7564.32	291.22
1835	S<222>	-7576.32	191.22
1836	S<221>	-7588.31	291.22
1837	SX<131>	-7600.31	191.22
1838	S<220>	-7612.31	291.22
1839	SX<130>	-7624.31	191.22
1840	S<219>	-7636.3	291.22

734	S<759>	10959.56	291.22
735	S<758>	10947.57	191.22
736	SX<449>	10935.57	291.22
737	S<757>	10923.57	191.22
738	SX<448>	10911.57	291.22
739	S<756>	10899.58	191.22
740	S<755>	10887.58	291.22
741	VSSA	10875.58	191.22
742	S<754>	10863.59	291.22
743	SX<447>	10851.59	191.22
744	S<753>	10839.59	291.22
745	S<752>	10827.59	191.22
746	VSSA	10815.6	291.22
747	S<751>	10803.6	191.22
748	SX<446>	10791.6	291.22
749	S<750>	10779.6	191.22
750	S<749>	10767.61	291.22
751	VSSA	10755.61	191.22
752	S<748>	10743.61	291.22
753	SX<445>	10731.61	191.22
754	S<747>	10719.62	291.22
755	S<746>	10707.62	191.22
756	VSSA	10695.62	291.22
757	S<745>	10683.63	191.22
758	SX<444>	10671.63	291.22
759	S<744>	10659.63	191.22
760	S<743>	10647.63	291.22
761	SX<443>	10635.64	191.22
762	S<742>	10623.64	291.22
763	SX<442>	10611.64	191.22
764	S<741>	10599.64	291.22
765	S<740>	10587.65	191.22
766	SX<441>	10575.65	291.22
767	S<739>	10563.65	191.22
768	SX<440>	10551.65	291.22
769	S<738>	10539.66	191.22
770	S<737>	10527.66	291.22
771	SX<439>	10515.66	191.22
772	S<736>	10503.67	291.22
773	SX<438>	10491.67	191.22
774	S<735>	10479.67	291.22
775	S<734>	10467.67	191.22
776	SX<437>	10455.68	291.22
777	S<733>	10443.68	191.22
778	SX<436>	10431.68	291.22
779	S<732>	10419.68	191.22

1841	S<218>	-7648.3	191.22
1842	SX<129>	-7660.3	291.22
1843	S<217>	-7672.29	191.22
1844	SX<128>	-7684.29	291.22
1845	S<216>	-7696.29	191.22
1846	S<215>	-7708.29	291.22
1847	VSSA	-7720.28	191.22
1848	S<214>	-7732.28	291.22
1849	SX<127>	-7744.28	191.22
1850	S<213>	-7756.28	291.22
1851	S<212>	-7768.27	191.22
1852	VSSA	-7780.27	291.22
1853	S<211>	-7792.27	191.22
1854	SX<126>	-7804.27	291.22
1855	S<210>	-7816.26	191.22
1856	S<209>	-7828.26	291.22
1857	VSSA	-7840.26	191.22
1858	S<208>	-7852.25	291.22
1859	SX<125>	-7864.25	191.22
1860	S<207>	-7876.25	291.22
1861	S<206>	-7888.25	191.22
1862	VSSA	-7900.24	291.22
1863	S<205>	-7912.24	191.22
1864	SX<124>	-7924.24	291.22
1865	S<204>	-7936.24	191.22
1866	S<203>	-7948.23	291.22
1867	SX<123>	-7960.23	191.22
1868	S<202>	-7972.23	291.22
1869	SX<122>	-7984.23	191.22
1870	S<201>	-7996.22	291.22
1871	S<200>	-8008.22	191.22
1872	SX<121>	-8020.22	291.22
1873	S<199>	-8032.21	191.22
1874	SX<120>	-8044.21	291.22
1875	S<198>	-8056.21	191.22
1876	S<197>	-8068.21	291.22
1877	SX<119>	-8080.2	191.22
1878	S<196>	-8092.2	291.22
1879	SX<118>	-8104.2	191.22
1880	S<195>	-8116.2	291.22
1881	S<194>	-8128.19	191.22
1882	SX<117>	-8140.19	291.22
1883	S<193>	-8152.19	191.22
1884	SX<116>	-8164.19	291.22
1885	S<192>	-8176.18	191.22
1886	S<191>	-8188.18	291.22

780	S<731>	10407.69	291.22
781	SX<435>	10395.69	191.22
782	S<730>	10383.69	291.22
783	SX<434>	10371.69	191.22
784	S<729>	10359.7	291.22
785	S<728>	10347.7	191.22
786	SX<433>	10335.7	291.22
787	S<727>	10323.71	191.22
788	SX<432>	10311.71	291.22
789	S<726>	10299.71	191.22
790	S<725>	10287.71	291.22
791	SX<431>	10275.72	191.22
792	S<724>	10263.72	291.22
793	SX<430>	10251.72	191.22
794	S<723>	10239.72	291.22
795	S<722>	10227.73	191.22
796	SX<429>	10215.73	291.22
797	S<721>	10203.73	191.22
798	SX<428>	10191.73	291.22
799	S<720>	10179.74	191.22
800	S<719>	10167.74	291.22
801	SX<427>	10155.74	191.22
802	S<718>	10143.75	291.22
803	SX<426>	10131.75	191.22
804	S<717>	10119.75	291.22
805	S<716>	10107.75	191.22
806	SX<425>	10095.76	291.22
807	S<715>	10083.76	191.22
808	SX<424>	10071.76	291.22
809	S<714>	10059.76	191.22
810	S<713>	10047.77	291.22
811	SX<423>	10035.77	191.22
812	S<712>	10023.77	291.22
813	SX<422>	10011.77	191.22
814	S<711>	9999.78	291.22
815	S<710>	9987.78	191.22
816	SX<421>	9975.78	291.22
817	S<709>	9963.79	191.22
818	SX<420>	9951.79	291.22
819	S<708>	9939.79	191.22
820	S<707>	9927.79	291.22
821	SX<419>	9915.8	191.22
822	S<706>	9903.8	291.22
823	SX<418>	9891.8	191.22
824	S<705>	9879.8	291.22
825	S<704>	9867.81	191.22

1887	SX<115>	-8200.18	191.22
1888	S<190>	-8212.17	291.22
1889	SX<114>	-8224.17	191.22
1890	S<189>	-8236.17	291.22
1891	S<188>	-8248.17	191.22
1892	SX<113>	-8260.16	291.22
1893	S<187>	-8272.16	191.22
1894	SX<112>	-8284.16	291.22
1895	S<186>	-8296.16	191.22
1896	S<185>	-8308.15	291.22
1897	SX<111>	-8320.15	191.22
1898	S<184>	-8332.15	291.22
1899	SX<110>	-8344.15	191.22
1900	S<183>	-8356.14	291.22
1901	S<182>	-8368.14	191.22
1902	SX<109>	-8380.14	291.22
1903	S<181>	-8392.13	191.22
1904	SX<108>	-8404.13	291.22
1905	S<180>	-8416.13	191.22
1906	S<179>	-8428.13	291.22
1907	SX<107>	-8440.12	191.22
1908	S<178>	-8452.12	291.22
1909	SX<106>	-8464.12	191.22
1910	S<177>	-8476.12	291.22
1911	S<176>	-8488.11	191.22
1912	SX<105>	-8500.11	291.22
1913	S<175>	-8512.11	191.22
1914	SX<104>	-8524.11	291.22
1915	S<174>	-8536.1	191.22
1916	S<173>	-8548.1	291.22
1917	SX<103>	-8560.1	191.22
1918	S<172>	-8572.09	291.22
1919	SX<102>	-8584.09	191.22
1920	S<171>	-8596.09	291.22
1921	S<170>	-8608.09	191.22
1922	SX<101>	-8620.08	291.22
1923	S<169>	-8632.08	191.22
1924	SX<100>	-8644.08	291.22
1925	S<168>	-8656.08	191.22
1926	S<167>	-8668.07	291.22
1927	SX<99>	-8680.07	191.22
1928	S<166>	-8692.07	291.22
1929	SX<98>	-8704.07	191.22
1930	S<165>	-8716.06	291.22
1931	S<164>	-8728.06	191.22
1932	SX<97>	-8740.06	291.22

826	SX<417>	9855.81	291.22
827	S<703>	9843.81	191.22
828	SX<416>	9831.81	291.22
829	S<702>	9819.82	191.22
830	S<701>	9807.82	291.22
831	VSSA	9795.82	191.22
832	S<700>	9783.83	291.22
833	SX<415>	9771.83	191.22
834	S<699>	9759.83	291.22
835	S<698>	9747.83	191.22
836	VSSA	9735.84	291.22
837	S<697>	9723.84	191.22
838	SX<414>	9711.84	291.22
839	S<696>	9699.84	191.22
840	S<695>	9687.85	291.22
841	VSSA	9675.85	191.22
842	S<694>	9663.85	291.22
843	SX<413>	9651.85	191.22
844	S<693>	9639.86	291.22
845	S<692>	9627.86	191.22
846	VSSA	9615.86	291.22
847	S<691>	9603.87	191.22
848	SX<412>	9591.87	291.22
849	S<690>	9579.87	191.22
850	S<689>	9567.87	291.22
851	SX<411>	9555.88	191.22
852	S<688>	9543.88	291.22
853	SX<410>	9531.88	191.22
854	S<687>	9519.88	291.22
855	S<686>	9507.89	191.22
856	SX<409>	9495.89	291.22
857	S<685>	9483.89	191.22
858	SX<408>	9471.89	291.22
859	S<684>	9459.9	191.22
860	S<683>	9447.9	291.22
861	SX<407>	9435.9	191.22
862	S<682>	9423.91	291.22
863	SX<406>	9411.91	191.22
864	S<681>	9399.91	291.22
865	S<680>	9387.91	191.22
866	SX<405>	9375.92	291.22
867	S<679>	9363.92	191.22
868	SX<404>	9351.92	291.22
869	S<678>	9339.92	191.22
870	S<677>	9327.93	291.22
871	SX<403>	9315.93	191.22

1933	S<163>	-8752.05	191.22
1934	SX<96>	-8764.05	291.22
1935	S<162>	-8776.05	191.22
1936	S<161>	-8788.05	291.22
1937	VSSA	-8800.04	191.22
1938	S<160>	-8812.04	291.22
1939	SX<95>	-8824.04	191.22
1940	S<159>	-8836.04	291.22
1941	S<158>	-8848.03	191.22
1942	VSSA	-8860.03	291.22
1943	S<157>	-8872.03	191.22
1944	SX<94>	-8884.03	291.22
1945	S<156>	-8896.02	191.22
1946	S<155>	-8908.02	291.22
1947	VSSA	-8920.02	191.22
1948	S<154>	-8932.01	291.22
1949	SX<93>	-8944.01	191.22
1950	S<153>	-8956.01	291.22
1951	S<152>	-8968.01	191.22
1952	VSSA	-8980	291.22
1953	S<151>	-8992	191.22
1954	SX<92>	-9004	291.22
1955	S<150>	-9016	191.22
1956	S<149>	-9027.99	291.22
1957	SX<91>	-9039.99	191.22
1958	S<148>	-9051.99	291.22
1959	SX<90>	-9063.99	191.22
1960	S<147>	-9075.98	291.22
1961	S<146>	-9087.98	191.22
1962	SX<89>	-9099.98	291.22
1963	S<145>	-9111.97	191.22
1964	SX<88>	-9123.97	291.22
1965	S<144>	-9135.97	191.22
1966	S<143>	-9147.97	291.22
1967	SX<87>	-9159.96	191.22
1968	S<142>	-9171.96	291.22
1969	SX<86>	-9183.96	191.22
1970	S<141>	-9195.96	291.22
1971	S<140>	-9207.95	191.22
1972	SX<85>	-9219.95	291.22
1973	S<139>	-9231.95	191.22
1974	SX<84>	-9243.95	291.22
1975	S<138>	-9255.94	191.22
1976	S<137>	-9267.94	291.22
1977	SX<83>	-9279.94	191.22
1978	S<136>	-9291.93	291.22

872	S<676>	9303.93	291.22
873	SX<402>	9291.93	191.22
874	S<675>	9279.94	291.22
875	S<674>	9267.94	191.22
876	SX<401>	9255.94	291.22
877	S<673>	9243.95	191.22
878	SX<400>	9231.95	291.22
879	S<672>	9219.95	191.22
880	S<671>	9207.95	291.22
881	SX<399>	9195.96	191.22
882	S<670>	9183.96	291.22
883	SX<398>	9171.96	191.22
884	S<669>	9159.96	291.22
885	S<668>	9147.97	191.22
886	SX<397>	9135.97	291.22
887	S<667>	9123.97	191.22
888	SX<396>	9111.97	291.22
889	S<666>	9099.98	191.22
890	S<665>	9087.98	291.22
891	SX<395>	9075.98	191.22
892	S<664>	9063.99	291.22
893	SX<394>	9051.99	191.22
894	S<663>	9039.99	291.22
895	S<662>	9027.99	191.22
896	SX<393>	9016	291.22
897	S<661>	9004	191.22
898	SX<392>	8992	291.22
899	S<660>	8980	191.22
900	S<659>	8968.01	291.22
901	SX<391>	8956.01	191.22
902	S<658>	8944.01	291.22
903	SX<390>	8932.01	191.22
904	S<657>	8920.02	291.22
905	S<656>	8908.02	191.22
906	SX<389>	8896.02	291.22
907	S<655>	8884.03	191.22
908	SX<388>	8872.03	291.22
909	S<654>	8860.03	191.22
910	S<653>	8848.03	291.22
911	SX<387>	8836.04	191.22
912	S<652>	8824.04	291.22
913	SX<386>	8812.04	191.22
914	S<651>	8800.04	291.22
915	S<650>	8788.05	191.22
916	SX<385>	8776.05	291.22
917	S<649>	8764.05	191.22

1979	SX<82>	-9303.93	191.22
1980	S<135>	-9315.93	291.22
1981	S<134>	-9327.93	191.22
1982	SX<81>	-9339.92	291.22
1983	S<133>	-9351.92	191.22
1984	SX<80>	-9363.92	291.22
1985	S<132>	-9375.92	191.22
1986	S<131>	-9387.91	291.22
1987	SX<79>	-9399.91	191.22
1988	S<130>	-9411.91	291.22
1989	SX<78>	-9423.91	191.22
1990	S<129>	-9435.9	291.22
1991	S<128>	-9447.9	191.22
1992	SX<77>	-9459.9	291.22
1993	S<127>	-9471.89	191.22
1994	SX<76>	-9483.89	291.22
1995	S<126>	-9495.89	191.22
1996	S<125>	-9507.89	291.22
1997	SX<75>	-9519.88	191.22
1998	S<124>	-9531.88	291.22
1999	SX<74>	-9543.88	191.22
2000	S<123>	-9555.88	291.22
2001	S<122>	-9567.87	191.22
2002	SX<73>	-9579.87	291.22
2003	S<121>	-9591.87	191.22
2004	SX<72>	-9603.87	291.22
2005	S<120>	-9615.86	191.22
2006	S<119>	-9627.86	291.22
2007	SX<71>	-9639.86	191.22
2008	S<118>	-9651.85	291.22
2009	SX<70>	-9663.85	191.22
2010	S<117>	-9675.85	291.22
2011	S<116>	-9687.85	191.22
2012	SX<69>	-9699.84	291.22
2013	S<115>	-9711.84	191.22
2014	SX<68>	-9723.84	291.22
2015	S<114>	-9735.84	191.22
2016	S<113>	-9747.83	291.22
2017	SX<67>	-9759.83	191.22
2018	S<112>	-9771.83	291.22
2019	SX<66>	-9783.83	191.22
2020	S<111>	-9795.82	291.22
2021	S<110>	-9807.82	191.22
2022	SX<65>	-9819.82	291.22
2023	S<109>	-9831.81	191.22
2024	SX<64>	-9843.81	291.22

918	SX<384>	8752.05	291.22
919	S<648>	8740.06	191.22
920	S<647>	8728.06	291.22
921	VSSA	8716.06	191.22
922	S<646>	8704.07	291.22
923	SX<383>	8692.07	191.22
924	S<645>	8680.07	291.22
925	S<644>	8668.07	191.22
926	VSSA	8656.08	291.22
927	S<643>	8644.08	191.22
928	SX<382>	8632.08	291.22
929	S<642>	8620.08	191.22
930	S<641>	8608.09	291.22
931	VSSA	8596.09	191.22
932	S<640>	8584.09	291.22
933	SX<381>	8572.09	191.22
934	S<639>	8560.1	291.22
935	S<638>	8548.1	191.22
936	VSSA	8536.1	291.22
937	S<637>	8524.11	191.22
938	SX<380>	8512.11	291.22
939	S<636>	8500.11	191.22
940	S<635>	8488.11	291.22
941	SX<379>	8476.12	191.22
942	S<634>	8464.12	291.22
943	SX<378>	8452.12	191.22
944	S<633>	8440.12	291.22
945	S<632>	8428.13	191.22
946	SX<377>	8416.13	291.22
947	S<631>	8404.13	191.22
948	SX<376>	8392.13	291.22
949	S<630>	8380.14	191.22
950	S<629>	8368.14	291.22
951	SX<375>	8356.14	191.22
952	S<628>	8344.15	291.22
953	SX<374>	8332.15	191.22
954	S<627>	8320.15	291.22
955	S<626>	8308.15	191.22
956	SX<373>	8296.16	291.22
957	S<625>	8284.16	191.22
958	SX<372>	8272.16	291.22
959	S<624>	8260.16	191.22
960	S<623>	8248.17	291.22
961	SX<371>	8236.17	191.22
962	S<622>	8224.17	291.22
963	SX<370>	8212.17	191.22

2025	S<108>	-9855.81	191.22
2026	S<107>	-9867.81	291.22
2027	VSSA	-9879.8	191.22
2028	S<106>	-9891.8	291.22
2029	SX<63>	-9903.8	191.22
2030	S<105>	-9915.8	291.22
2031	S<104>	-9927.79	191.22
2032	VSSA	-9939.79	291.22
2033	S<103>	-9951.79	191.22
2034	SX<62>	-9963.79	291.22
2035	S<102>	-9975.78	191.22
2036	S<101>	-9987.78	291.22
2037	VSSA	-9999.78	191.22
2038	S<100>	-10011.77	291.22
2039	SX<61>	-10023.77	191.22
2040	S<99>	-10035.77	291.22
2041	S<98>	-10047.77	191.22
2042	VSSA	-10059.76	291.22
2043	S<97>	-10071.76	191.22
2044	SX<60>	-10083.76	291.22
2045	S<96>	-10095.76	191.22
2046	S<95>	-10107.75	291.22
2047	SX<59>	-10119.75	191.22
2048	S<94>	-10131.75	291.22
2049	SX<58>	-10143.75	191.22
2050	S<93>	-10155.74	291.22
2051	S<92>	-10167.74	191.22
2052	SX<57>	-10179.74	291.22
2053	S<91>	-10191.73	191.22
2054	SX<56>	-10203.73	291.22
2055	S<90>	-10215.73	191.22
2056	S<89>	-10227.73	291.22
2057	SX<55>	-10239.72	191.22
2058	S<88>	-10251.72	291.22
2059	SX<54>	-10263.72	191.22
2060	S<87>	-10275.72	291.22
2061	S<86>	-10287.71	191.22
2062	SX<53>	-10299.71	291.22
2063	S<85>	-10311.71	191.22
2064	SX<52>	-10323.71	291.22
2065	S<84>	-10335.7	191.22
2066	S<83>	-10347.7	291.22
2067	SX<51>	-10359.7	191.22
2068	S<82>	-10371.69	291.22
2069	SX<50>	-10383.69	191.22
2070	S<81>	-10395.69	291.22

964	S<621>	8200.18	291.22
965	S<620>	8188.18	191.22
966	SX<369>	8176.18	291.22
967	S<619>	8164.19	191.22
968	SX<368>	8152.19	291.22
969	S<618>	8140.19	191.22
970	S<617>	8128.19	291.22
971	SX<367>	8116.2	191.22
972	S<616>	8104.2	291.22
973	SX<366>	8092.2	191.22
974	S<615>	8080.2	291.22
975	S<614>	8068.21	191.22
976	SX<365>	8056.21	291.22
977	S<613>	8044.21	191.22
978	SX<364>	8032.21	291.22
979	S<612>	8020.22	191.22
980	S<611>	8008.22	291.22
981	SX<363>	7996.22	191.22
982	S<610>	7984.23	291.22
983	SX<362>	7972.23	191.22
984	S<609>	7960.23	291.22
985	S<608>	7948.23	191.22
986	SX<361>	7936.24	291.22
987	S<607>	7924.24	191.22
988	SX<360>	7912.24	291.22
989	S<606>	7900.24	191.22
990	S<605>	7888.25	291.22
991	SX<359>	7876.25	191.22
992	S<604>	7864.25	291.22
993	SX<358>	7852.25	191.22
994	S<603>	7840.26	291.22
995	S<602>	7828.26	191.22
996	SX<357>	7816.26	291.22
997	S<601>	7804.27	191.22
998	SX<356>	7792.27	291.22
999	S<600>	7780.27	191.22
1000	S<599>	7768.27	291.22
1001	SX<355>	7756.28	191.22
1002	S<598>	7744.28	291.22
1003	SX<354>	7732.28	191.22
1004	S<597>	7720.28	291.22
1005	S<596>	7708.29	191.22
1006	SX<353>	7696.29	291.22
1007	S<595>	7684.29	191.22
1008	SX<352>	7672.29	291.22
1009	S<594>	7660.3	191.22

2071	S<80>	-10407.69	191.22
2072	SX<49>	-10419.68	291.22
2073	S<79>	-10431.68	191.22
2074	SX<48>	-10443.68	291.22
2075	S<78>	-10455.68	191.22
2076	S<77>	-10467.67	291.22
2077	SX<47>	-10479.67	191.22
2078	S<76>	-10491.67	291.22
2079	SX<46>	-10503.67	191.22
2080	S<75>	-10515.66	291.22
2081	S<74>	-10527.66	191.22
2082	SX<45>	-10539.66	291.22
2083	S<73>	-10551.65	191.22
2084	SX<44>	-10563.65	291.22
2085	S<72>	-10575.65	191.22
2086	S<71>	-10587.65	291.22
2087	SX<43>	-10599.64	191.22
2088	S<70>	-10611.64	291.22
2089	SX<42>	-10623.64	191.22
2090	S<69>	-10635.64	291.22
2091	S<68>	-10647.63	191.22
2092	SX<41>	-10659.63	291.22
2093	S<67>	-10671.63	191.22
2094	SX<40>	-10683.63	291.22
2095	S<66>	-10695.62	191.22
2096	S<65>	-10707.62	291.22
2097	SX<39>	-10719.62	191.22
2098	S<64>	-10731.61	291.22
2099	SX<38>	-10743.61	191.22
2100	S<63>	-10755.61	291.22
2101	S<62>	-10767.61	191.22
2102	SX<37>	-10779.6	291.22
2103	S<61>	-10791.6	191.22
2104	SX<36>	-10803.6	291.22
2105	S<60>	-10815.6	191.22
2106	S<59>	-10827.59	291.22
2107	SX<35>	-10839.59	191.22
2108	S<58>	-10851.59	291.22
2109	SX<34>	-10863.59	191.22
2110	S<57>	-10875.58	291.22
2111	S<56>	-10887.58	191.22
2112	SX<33>	-10899.58	291.22
2113	S<55>	-10911.57	191.22
2114	SX<32>	-10923.57	291.22
2115	S<54>	-10935.57	191.22
2116	S<53>	-10947.57	291.22

1010	S<593>	7648.3	291.22
1011	VSSA	7636.3	191.22
1012	S<592>	7624.31	291.22
1013	SX<351>	7612.31	191.22
1014	S<591>	7600.31	291.22
1015	S<590>	7588.31	191.22
1016	VSSA	7576.32	291.22
1017	S<589>	7564.32	191.22
1018	SX<350>	7552.32	291.22
1019	S<588>	7540.32	191.22
1020	S<587>	7528.33	291.22
1021	VSSA	7516.33	191.22
1022	S<586>	7504.33	291.22
1023	SX<349>	7492.33	191.22
1024	S<585>	7480.34	291.22
1025	S<584>	7468.34	191.22
1026	VSSA	7456.34	291.22
1027	S<583>	7444.35	191.22
1028	SX<348>	7432.35	291.22
1029	S<582>	7420.35	191.22
1030	S<581>	7408.35	291.22
1031	SX<347>	7396.36	191.22
1032	S<580>	7384.36	291.22
1033	SX<346>	7372.36	191.22
1034	S<579>	7360.36	291.22
1035	S<578>	7348.37	191.22
1036	SX<345>	7336.37	291.22
1037	S<577>	7324.37	191.22
1038	SX<344>	7312.37	291.22
1039	S<576>	7300.38	191.22
1040	S<575>	7288.38	291.22
1041	SX<343>	7276.38	191.22
1042	S<574>	7264.39	291.22
1043	SX<342>	7252.39	191.22
1044	S<573>	7240.39	291.22
1045	S<572>	7228.39	191.22
1046	SX<341>	7216.4	291.22
1047	S<571>	7204.4	191.22
1048	SX<340>	7192.4	291.22
1049	S<570>	7180.4	191.22
1050	S<569>	7168.41	291.22
1051	SX<339>	7156.41	191.22
1052	S<568>	7144.41	291.22
1053	SX<338>	7132.41	191.22
1054	S<567>	7120.42	291.22
1055	S<566>	7108.42	191.22
2117	VSSA	-10959.56	191.22
2118	S<52>	-10971.56	291.22
2119	SX<31>	-10983.56	191.22
2120	S<51>	-10995.56	291.22
2121	S<50>	-11007.55	191.22
2122	VSSA	-11019.55	291.22
2123	S<49>	-11031.55	191.22
2124	SX<30>	-11043.55	291.22
2125	S<48>	-11055.54	191.22
2126	S<47>	-11067.54	291.22
2127	VSSA	-11079.54	191.22
2128	S<46>	-11091.53	291.22
2129	SX<29>	-11103.53	191.22
2130	S<45>	-11115.53	291.22
2131	S<44>	-11127.53	191.22
2132	VSSA	-11139.52	291.22
2133	S<43>	-11151.52	191.22
2134	SX<28>	-11163.52	291.22
2135	S<42>	-11175.52	191.22
2136	S<41>	-11187.51	291.22
2137	SX<27>	-11199.51	191.22
2138	S<40>	-11211.51	291.22
2139	SX<26>	-11223.51	191.22
2140	S<39>	-11235.5	291.22
2141	S<38>	-11247.5	191.22
2142	SX<25>	-11259.5	291.22
2143	S<37>	-11271.49	191.22
2144	SX<24>	-11283.49	291.22
2145	S<36>	-11295.49	191.22
2146	S<35>	-11307.49	291.22
2147	SX<23>	-11319.48	191.22
2148	S<34>	-11331.48	291.22
2149	SX<22>	-11343.48	191.22
2150	S<33>	-11355.48	291.22
2151	S<32>	-11367.47	191.22
2152	SX<21>	-11379.47	291.22
2153	S<31>	-11391.47	191.22
2154	SX<20>	-11403.47	291.22
2155	S<30>	-11415.46	191.22
2156	S<29>	-11427.46	291.22
2157	SX<19>	-11439.46	191.22
2158	S<28>	-11451.45	291.22
2159	SX<18>	-11463.45	191.22
2160	S<27>	-11475.45	291.22
2161	S<26>	-11487.45	191.22
2162	SX<17>	-11499.44	291.22

1056	SX<337>	7096.42	291.22
1057	S<565>	7084.43	191.22
1058	SX<336>	7072.43	291.22
1059	S<564>	7060.43	191.22
1060	S<563>	7048.43	291.22
1061	SX<335>	7036.44	191.22
1062	S<562>	7024.44	291.22
1063	SX<334>	7012.44	191.22
1064	S<561>	7000.44	291.22
1065	S<560>	6988.45	191.22
1066	SX<333>	6976.45	291.22
1067	S<559>	6964.45	191.22
1068	SX<332>	6952.45	291.22
1069	S<558>	6940.46	191.22
1070	S<557>	6928.46	291.22
1071	SX<331>	6916.46	191.22
1072	S<556>	6904.47	291.22
1073	SX<330>	6892.47	191.22
1074	S<555>	6880.47	291.22
1075	S<554>	6868.47	191.22
1076	SX<329>	6856.48	291.22
1077	S<553>	6844.48	191.22
1078	SX<328>	6832.48	291.22
1079	S<552>	6820.48	191.22
1080	S<551>	6808.49	291.22
1081	SX<327>	6796.49	191.22
1082	S<550>	6784.49	291.22
1083	SX<326>	6772.49	191.22
1084	S<549>	6760.5	291.22
1085	S<548>	6748.5	191.22
1086	SX<325>	6736.5	291.22
1087	S<547>	6724.51	191.22
1088	SX<324>	6712.51	291.22
1089	S<546>	6700.51	191.22
1090	S<545>	6688.51	291.22
1091	SX<323>	6676.52	191.22
1092	S<544>	6664.52	291.22
1093	SX<322>	6652.52	191.22
1094	S<543>	6640.52	291.22
1095	S<542>	6628.53	191.22
1096	SX<321>	6616.53	291.22
1097	S<541>	6604.53	191.22
1098	VSSA	6592.53	291.22
1099	VSSA	6580.54	191.22
1100	VSSA	6568.54	291.22
1101	VSSA	6556.54	191.22

2163	S<25>	-11511.44	191.22
2164	SX<16>	-11523.44	291.22
2165	S<24>	-11535.44	191.22
2166	S<23>	-11547.43	291.22
2167	SX<15>	-11559.43	191.22
2168	S<22>	-11571.43	291.22
2169	SX<14>	-11583.43	191.22
2170	S<21>	-11595.42	291.22
2171	S<20>	-11607.42	191.22
2172	SX<13>	-11619.42	291.22
2173	S<19>	-11631.41	191.22
2174	SX<12>	-11643.41	291.22
2175	S<18>	-11655.41	191.22
2176	S<17>	-11667.41	291.22
2177	SX<11>	-11679.4	191.22
2178	S<16>	-11691.4	291.22
2179	SX<10>	-11703.4	191.22
2180	S<15>	-11715.4	291.22
2181	S<14>	-11727.39	191.22
2182	SX<9>	-11739.39	291.22
2183	S<13>	-11751.39	191.22
2184	SX<8>	-11763.39	291.22
2185	S<12>	-11775.38	191.22
2186	S<11>	-11787.38	291.22
2187	SX<7>	-11799.38	191.22
2188	S<10>	-11811.37	291.22
2189	SX<6>	-11823.37	191.22
2190	S<9>	-11835.37	291.22
2191	S<8>	-11847.37	191.22
2192	SX<5>	-11859.36	291.22
2193	S<7>	-11871.36	191.22
2194	SX<4>	-11883.36	291.22
2195	S<6>	-11895.36	191.22
2196	S<5>	-11907.35	291.22
2197	SX<3>	-11919.35	191.22
2198	S<4>	-11931.35	291.22
2199	SX<2>	-11943.35	191.22
2200	S<3>	-11955.34	291.22
2201	S<2>	-11967.34	191.22
2202	SX<1>	-11979.34	291.22
2203	S<1>	-11991.33	191.22
2204	SDUM1	-12003.33	291.22
2205	VCOM_PASS_L	-12015.33	191.22
2206	VCOM_PASS_L	-12027.33	291.22
2207	VSSA	-12039.32	191.22
2208	VSSA	-12051.32	291.22

1102	VSSA	6544.55	291.22
1103	VSSA	6532.55	191.22
1104	VSSA	6520.55	291.22
1105	VSSA	6508.55	191.22
1106	VSSA	6496.56	291.22
1107	VSSA	6484.56	191.22

2209	VSSA	-12063.32	191.22
2210	VSSA	-12075.32	291.22
2211	VSSA	-12087.31	191.22
2212	VSSA	-12099.31	291.22
2213	VSSA	-12111.31	191.22

9 DISCLAIMER

The information appearing in this publication is believed to be accurate.Integrated circuits sold by AIXIESHENG covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. AIXIESHENG Technology makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. Furthermore, AIXIESHENG Technology makes no warranty of merchant ability or fitness for any purpose. AIXIESHENG Technology reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by AIXIESHENG Technology for such applications. Please note that application circuits illustrated in this document are for reference purposes only.